MC20002

FPGA Bridge IC

for

MIPI D-PHY Systems
and
LVDS to SLVS Conversion

PRELIMINARY DATASHEET

Version 1.07

April 2014

Meticom GmbH

Revision History

MC20002		
Version	**Date of Issue**	**Change**
1.01	April 25, 2012	• First Draft
1.02	May 10, 2012	• Updated maximum speed • Added Application Diagram • Added AC and DC Characteristics • Added application examples
1.03	August 10, 2012	• Updated AC characteristics
1.04	October 09, 2012	• Table 5, pin numbers corrected: pin 9 (VDD); pin 12 (VDDIO) • Table 5, Thermal Pad description added
1.05	November 22, 2012	• Added thermal pad dimensions • Added RoHS statement
1.06	December 20, 2012	• Clarified use of GPIO pins in section 6.5
1.07	April 4, 2014	• Package drawing update • Application note added - input to output signal diagram

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1 General Description

The MC20002 is a high performance FPGA bridge IC, which converts incoming LVDS high speed and incoming CMOS low speed data streams into a single lane MIPI D-PHY compliant output stream. The MC20002 can also convert an LVDS signal into an SLVS signal.

The MC20002 can be connected to any signal source, for example FPGAs or DSPs.

Data rates can be from 0 Mbps to 2.5 Gbps in HS (High Speed) mode and up to 20 Mbps in LPDT (Low Power Data Transmission) mode.

In MIPI D-PHY mode the $T_{HS\text{-}PREPARE}$ timing can be controlled by the host device.

2 Key Features

- Output is compliant to MIPI D-PHY interfaces using the DSI, CSI-1 and CSI-2 standards
  - HS mode data rate: up to a maximum of 2.5 Gbps
  - LPDT mode data rate: up to 20 Mbps
- Flexible $T_{HS\text{-}PREPARE}$ timing in MIPI D-PHY mode
- Conversion of LVDS input to SLVS output
  - LVDS data rate: up to a maximum of 2.5 Gbps
- No additional level shifters needed
- Arbitrary power up sequence
- Available as a bare die
  - RoHS compliant, Pb-free
- Available in a TQLMP-16 package
  - 3mm * 3mm * 0.75mm
  - 0.5mm pitch
  - RoHS compliant, Pb-free

3 Block Diagram

3.1 Block Diagram

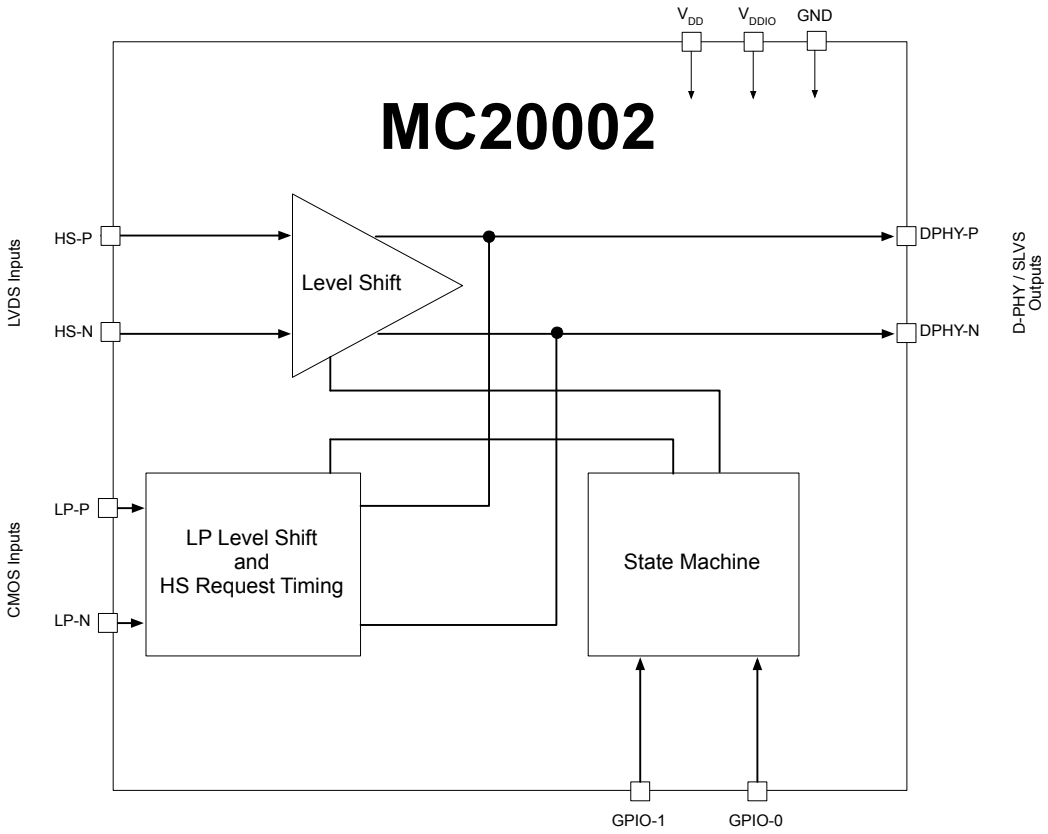


Figure 1: Functional Block Diagram of the MC20002

4 Parametrics

4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{DDIO}	Supply voltage		-0.5	3.6	V
V_{DD}	Supply voltage		-0.5	2.0	V
T_{STG}	Storage temperature		-55	125	°C
T_J	Junction temperature		-55	125	°C
V_{ESD}	Electrostatic discharge voltage capability	(HBM; 100 pF, 1.5 kΩ)	2.0		kV
$V_{ESD\text{-}Dout}$	Electrostatic discharge voltage capability at differential I/Os	(HBM; 100 pF, 1.5 kΩ)	500 (target 2000)		V

Table 1: Absolute Maximum Ratings

Notes:

Absolute Maximum Ratings may not be exceeded to the device without causing permanent damage or degradation. Exposures to these values for extended periods may affect device reliability. If the device is operated beyond the range of Operating Conditions functionality is not guaranteed.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDIO}	Supply voltage		2.3	2.5	2.7	V
V_{DD}	Supply voltage		1.1	1.2	1.3	V
GND	Ground			0		V
$V_{noise,VDD}$	Maximum allowed supply noise on V_{DD}	see Figure 2			100	mV_{pp}
T_A	Ambient temperature		-40	25	100	°C

Table 2: Operating Conditions

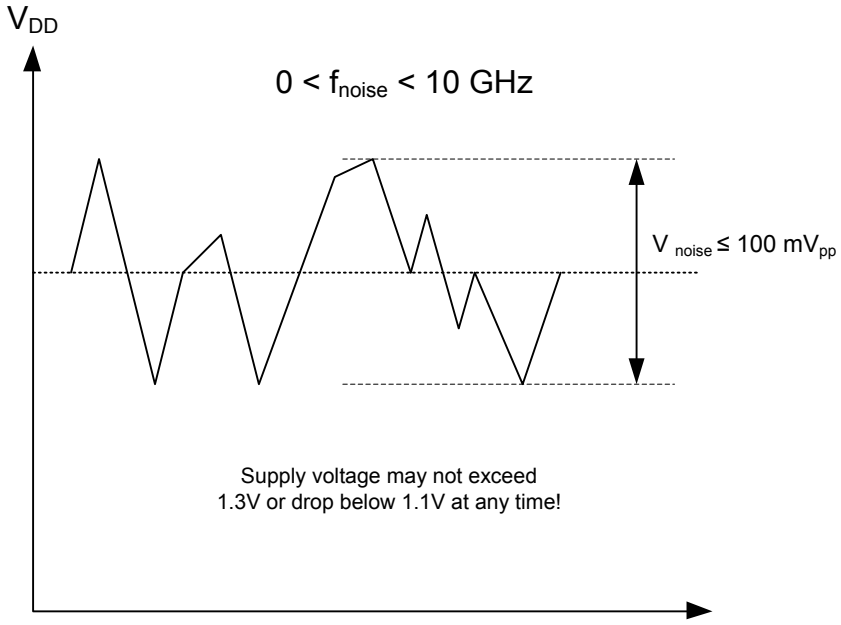


Figure 2: Maximum Allowed Supply Noise on V_{DD}

4.3 DC Characteristics

(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	HS mode supply current including SLVS output	D-PHY HS Mode / LVDS to SLVS	2.13		2.73	mA
I_{DDIO}	HS mode supply current	D-PHY HS Mode / LVDS to SLVS	0.47		0.5	mA
Single Ended Input (LP-P, LP-N, GPIO-0, GPIO-1)						
V_{IH}	High level input voltage		0.7		V_{DDIO}	V
V_{IL}	Low level input voltage		0		0.5	V
I_{IH}	High level input current	$V_{IN} \geq V_{DDIO}$ - 0.2			100	nA
I_{IL}	Low level input voltage	$V_{IN} \leq 0.2$			100	nA
C_{IN}	Input capacitance	Including package		1	1.5	pF
HS Input (HS-P, HS-N)						
V_{CM-IN}			800	1200	1600	mV
$\|V_{IN-Diff}\|$		@ up to 1.5Gbps	70		400	mV
		@ above 1.5Gbps	140		400	mV
Z_{IN}			80	100	125	Ω
Differential Output (D_{PHY-P}, D_{PHY-N})						
V_{CM-OUT}	Output common mode voltage	@V_{DD}=1.2V	150	200	250	mV
$\|V_{DO_DIFF}\|$	Differential output voltage	$\|V_{DPHY-P} - V_{DPHY-N}\|$ @ V_{DD}=1.2V	150	180	250	mV_{pp}
Z_{OD}	Output impedance	Differential	80	100	125	Ω

Table 3: DC Characteristics

4.4 AC Characteristics

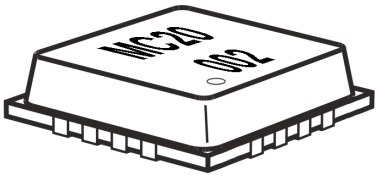
(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
HS Input (HS-P, HS-N)							
S_{11}	Input return loss	f <1.04GHz			15	dB	
t_{R,HS_Tx} , $t_{F_HS_Tx}$	Input data transition time	20%-80%			0.5	UI	
BR	Supported input data bit rate		0		2500	Mbps	
LP Input (LP-P, LP-N, GPIO-0, GPIO-1)							
BR_{LP}	Maximum LP input bit rate		0		20	Mbps	
D-PHY Output (DPHY-P, DPHY-N)							
BR	Maximum serial output data bit rate		2500			Mbps	
t_R, t_F	Output data transition time	20%-80%		90		ps	
S_{22}	Output return loss	f <1.04GHz			15	dB	
		f <625MHz			18	dB	
J_D	Deterministic output jitter	at D_{PHY-P} / D_{PHY-N}			30	ps	
J_R	Generated random output jitter	at D_{PHY-P} / D_{PHY-N}		0.5	0.9	ps_{rms}	
J_{PSRR}	Jitter caused by PSRR	Supply noise @ VDD		1	2	ps/mV	

Table 4: AC Characteristics

5 Package Information

5.1 TQLMP-16 Package



(drawing not to scale)

- Package Type: Thin Quad Leadless Molded Package (TQLMP)
- Package Dimensions: 3.0 x 3.0 x 0.75 mm³
- Pin Pitch: 0.5 mm

5.2 Pin Description

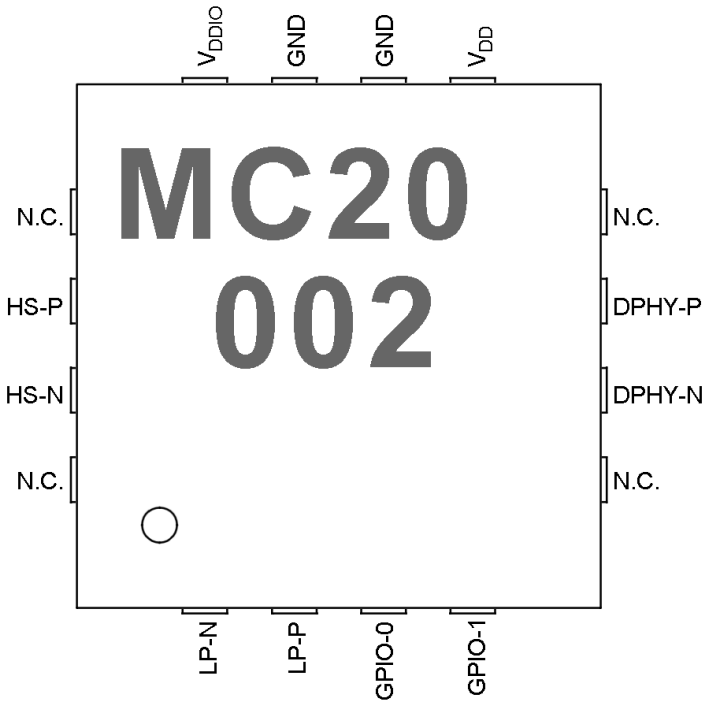
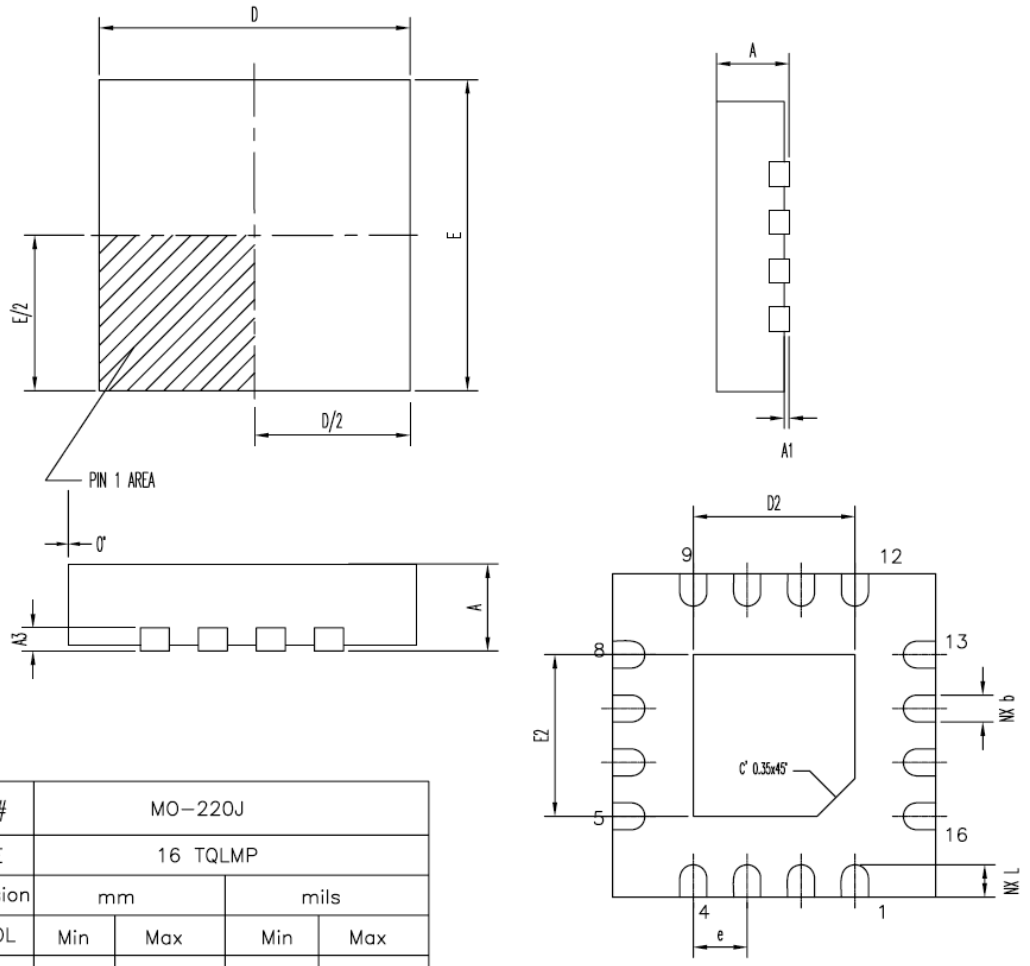


Figure 3: Pin Assignment MC20002

Pin Name	Pin No.	I/O	Type	Description
VDDIO	12	I	Supply	Supply voltage for the LVDS input stage and internal level shifters
VDD	9	I	Supply	Supply voltage for the SLVS Output Driver and internal logic
GND	10, 11	-	-	Global ground
HS-P	14	I	LVDS	Positive LVDS high speed input
HS-N	15	I	LVDS	Negative LVDS high speed input
LP-P	2	I	CMOS	Positive CMOS low power data input
LP-N	1	I	CMOS	Negative CMOS low power data input
GPIO-0	3	I	CMOS	General purpose configuration input 0
GPIO-1	4	I	CMOS	General purpose configuration input 1
DPHY-P	7	O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output
DPHY-N	6	O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output
N.C.	5, 8, 13, 16	-	-	Do not connect
Thermal Pad		-	-	Thermal Pad may be connected to GND or left floating (n.c.)

Table 5: Pin Description

5.3 Package Information



JEDEC#	MO-220J			
TYPE	16 TQLMP			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.7	0.8	27.56	31.50
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	2.9	3.1	114.17	122.05
E	2.9	3.1	114.17	122.05
D2	1.4	1.6	55.12	62.99
E2	1.4	1.6	55.12	62.99
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.25	0.35	9.84	13.78
θ°	0°	4°	0°	4°
ND	4			
NE	4			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

Figure 4: Mechanical Dimensions TQLMP-16

6 Application Notes

6.1 Application Overview

MC20002 can be used together with D-PHY sink (such as a display) as shown. It can take standard LVDS and CMOS signals from an FPGA and convert them into a D-PHY compliant output stream, which can then be fed directly into a D-PHY compliant display.

The diagram also shows the MC20001, which performs the reverse function of the MC20002.

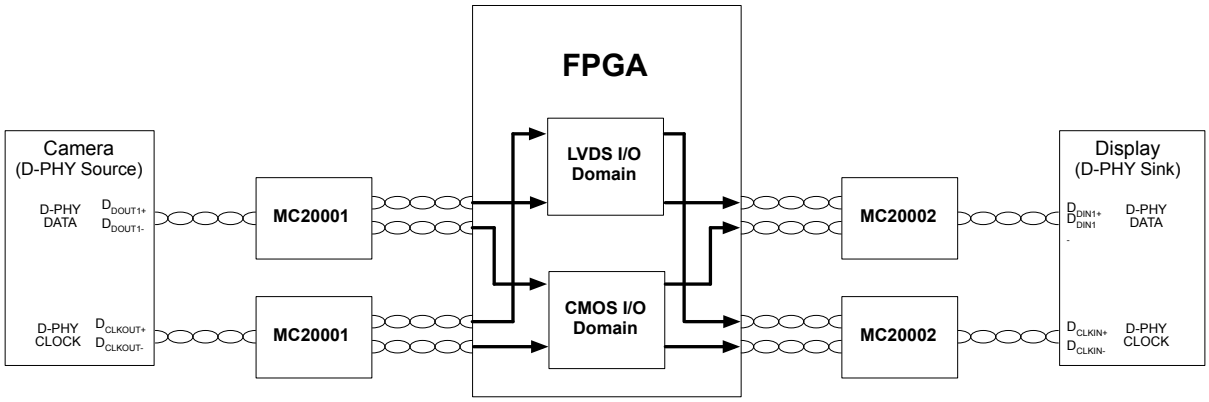


Figure 5: Application Diagram

6.2 FPGA to D-PHY Bridge Application

In this example one D-PHY clock lane and one D-PHY data lane are shown. Additional D-PHY data lanes can be implemented in the same way.

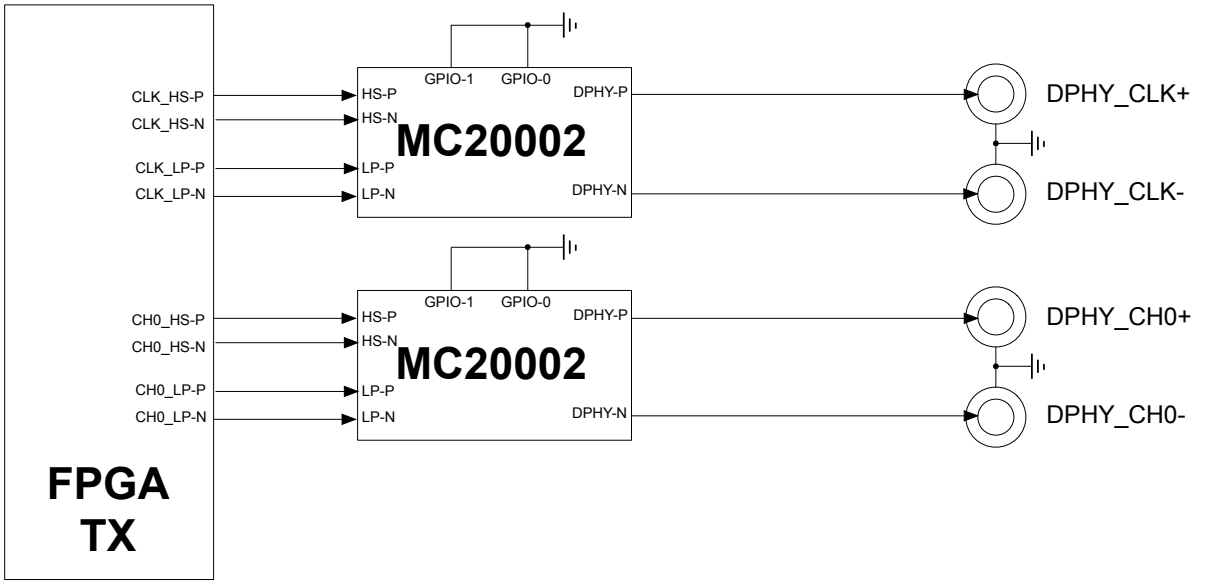


Figure 6: FPGA to D-PHY Bridge Application

6.3 FPGA to D-PHY Bridge Application with Bus Turnaround

In this example one D-PHY clock lane and one D-PHY data lane are shown. The D-PHY data lane uses an MC20001 to implement the bus turnaround (BTA) function. Additional D-PHY data lanes, which do not use BTA, can be implemented in the same way as the D-PHY clock lane.

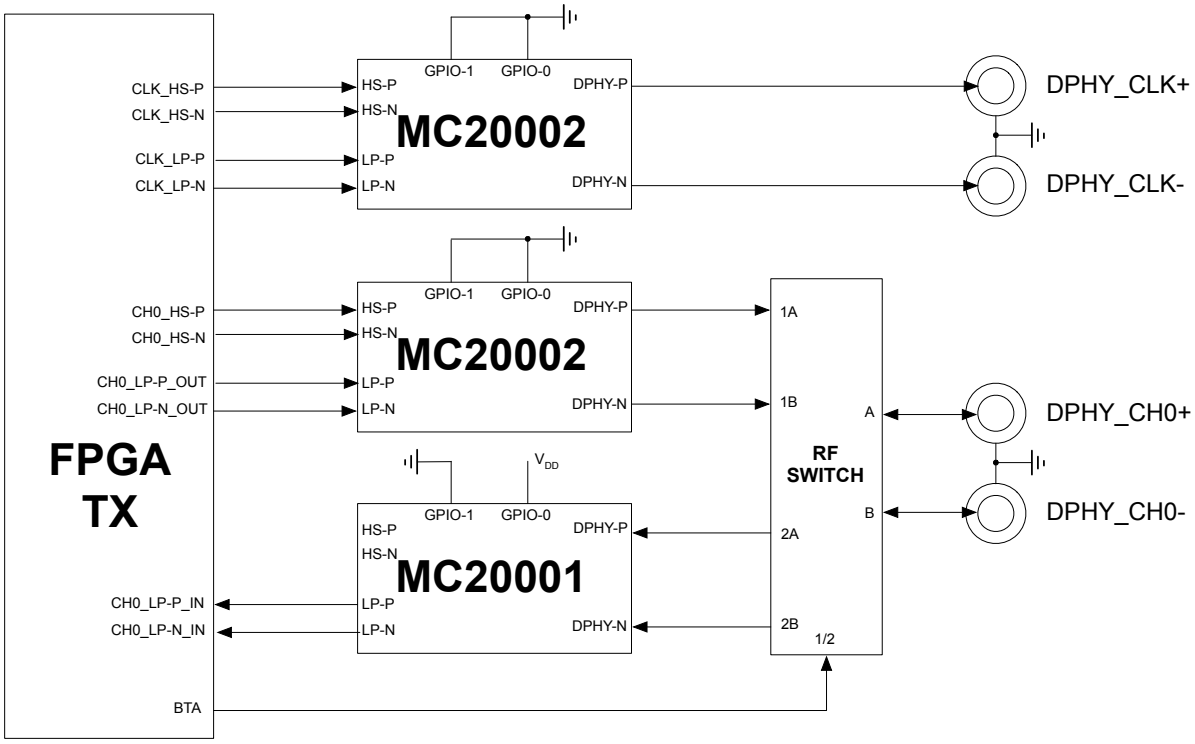


Figure 7: FPGA to D-PHY Bridge Application with Bus Turnaround

6.4 Signal Levels

6.4.1 HS-P and HS-N LVDS Inputs

The allowed common mode range is between 800mV and 1.6 Volt for DC coupling. The inputs can also be AC coupled.

6.4.2 LP-P and LP-N CMOS Inputs

MC20002 accepts logic input voltages between 0.7 Volt and 2.7 Volt for a ‘High’ Level.

No level shifters are needed in order to translate a 2.5V logic output from an FPGA to a 1.2V MIPI D-PHY compliant LP signal.

6.4.3 DPHY-P and DPHY-N Outputs

These signals are compliant with the MIPI D-PHY specification.

6.5 Configuration for MIPI D-PHY Operation Using GPIO-0 and GPIO-1

GPIO-1	GPIO-0	Description	
0	0	Fixed internal timing for $T_{HS-PREPARE}$ = 60ns	Mode 1
0	1	IC sleep mode (used together with LP-P and LP-N pins)	Mode 2
1	0	External $T_{HS-PREPARE}$ timing mode activated	Mode 3
1	1	Determines exact time for $T_{HS-PREPARE}$	Mode 4

Table 6: GPIO Selection Bits in MIPI D-PHY Mode

- Mode 1:
  As soon as a high speed request (HSR) has been detected at the LP-P and LP-N inputs, MC20002 switches through the HS inputs to the DPHY outputs after a fixed time delay of 60 ns. The HS inputs are also level shifted to the D-PHY compliant SLVS levels. During this time a $T_{HS-PREPARE}$ signal is sent to the D-PHY outputs.

- Mode 2:
  The IC can be set to sleep mode. To achieve this, the LP-P and LP-N inputs are used as control inputs and are used together with the GPIO-0 and GPIO-1 inputs as shown below.

LP-P	LP-N	GPIO-1	GPIO-0	Description
1	1	0	1	Sleep mode, outputs: DPHY-P = 1.2V, DPHY-N = 1.2V

Table 7: Configuration for Sleep Mode

- Mode 3:
  Setting GPIO-1 activates the mode which enables an external setting of $T_{HS-PREPARE}$. As soon as a high speed request (HSR) has been detected at the LP-P and LP-N inputs, MC20002 waits for an external trigger signal on GPIO-0. Until the trigger has been received MC20002 will not output the HS data on the DPHY outputs. During this time a $T_{HS-PREPARE}$ signal is sent to the D-PHY outputs.

- Mode 4:
  When MC20002 is in Mode 3 and the GPIO-0 pin goes high, MC20002 will then output the HS data on the DPHY outputs. This allows for a programmable $T_{HS-PREPARE}$ timing

6.6 Configuration for LVDS to SLVS Conversion

In this mode the LP-P and LP-N inputs are used as control inputs and are used together with the GPIO-0 and GPIO-1 inputs to define the mode of operation as shown below.

LP-P	LP-N	GPIO-1	GPIO-0	Description
0	0	0	1	LVDS to SLVS conversion mode activated

Table 8: Configuration for LVDS to SLVS Conversion Mode

6.7 Input to Output Signal Diagram

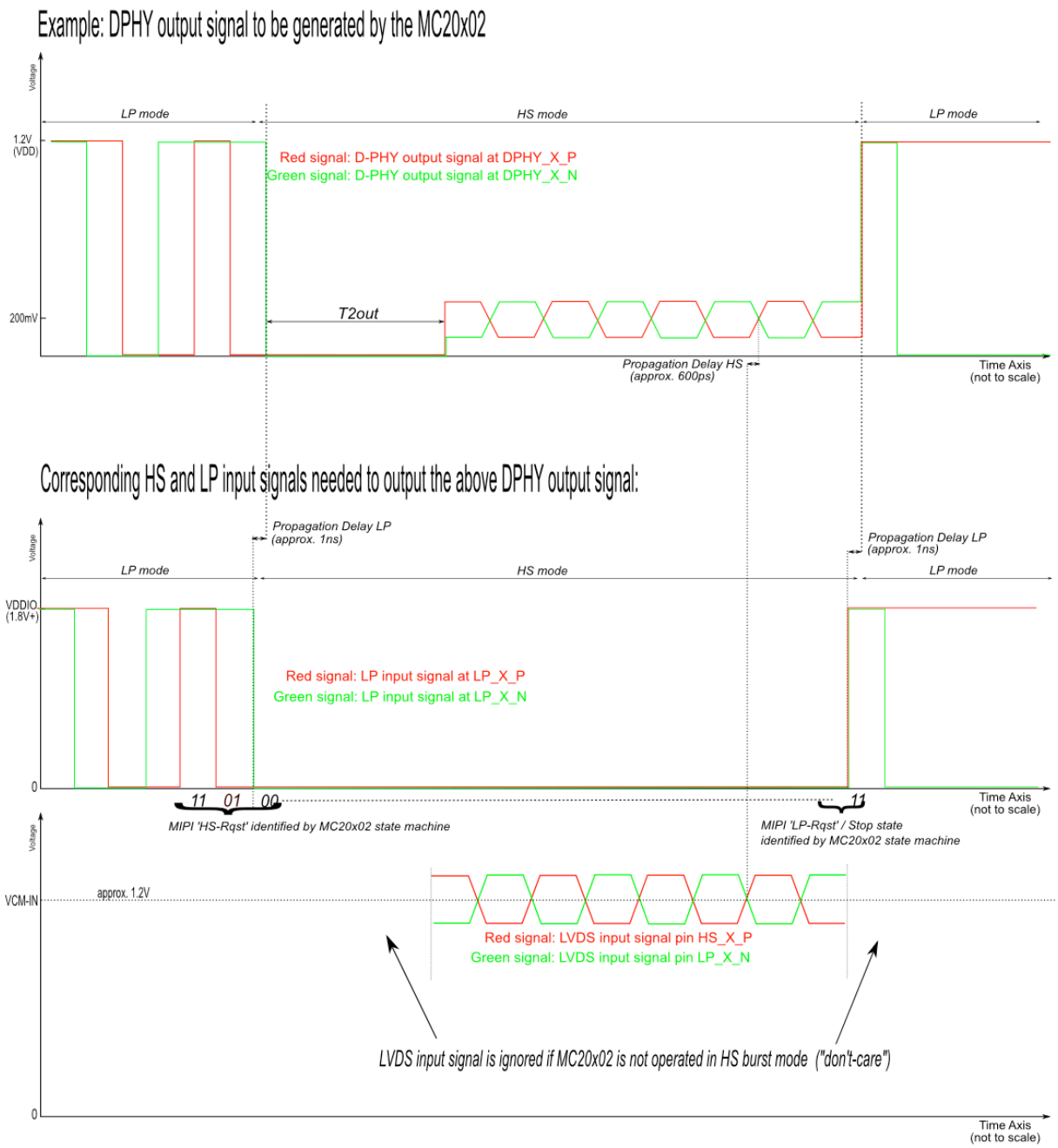


Figure 5: Input to Output Signal Diagram

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