800mA Triple Output Laser Diode Driver

ISL58303

The ISL58303 is a high-speed triple output laser diode driver designed to support color field sequential laser light source Pico projection modules. Outputs can be ganged together to achieve peak total current greater than 3.6A. Output channels are designed with independent programmable bias and threshold adjustment to support a wide range of laser diode manufacturers. The ISL58303 offers exceptional power efficiency and a high degree of system integration allowing a compact and cost effective system design.

To assist with reduction of laser speckle, this laser diode driver has a high frequency modulation input to modulate laser pulses. This can be used to achieve outputs pulses of less than 1ns.

Interface to the system is accomplished via a high-speed serial bus that is made up of SEN, SCLK and SDIO. Initialization of internal registers after power-on reset, operational setup and laser intensity data for each output channel are communicated through this bus.

For laser operational safety, a hardware enable signal (CE) is ANDed with an internal register bit. Both have to be asserted to enable the device. This prevents an accidental fault causing an unwanted laser output.

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Features

- Complete triple programmable laser diode driver
- 800mA maximum output current per channel
- 1200mA peak output current per channel
- Ganging of multiple channels as well as multiple chips can be done to meet the highest current demands
- ISL58303 has all N-MOS output channels (I_{OUT1}, I_{OUT2} and I_{OUT3}) for common anode laser diode configurations
- Independent output channel enable
- Programmable threshold DACs and color DACs for each channel
- Supports High Frequency Modulation (HFM) that switches all 3 outputs in unison producing pulse widths of less than 1ns.
- Fast SPI serial interface
- Space saving package: 24 Ld 4mmx4mm TQFN

Applications

- RGB color field sequential laser projection system
- Time of flight measurement systems
- High speed/high current laser diode systems

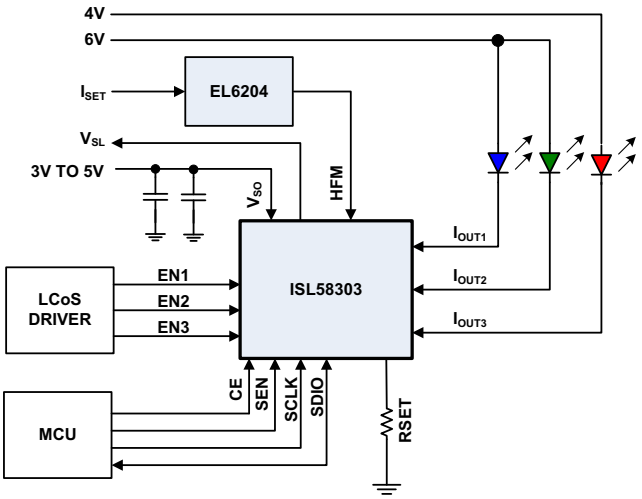

FIGURE 1. ISL58303 TYPICAL APPLICATION LCOS

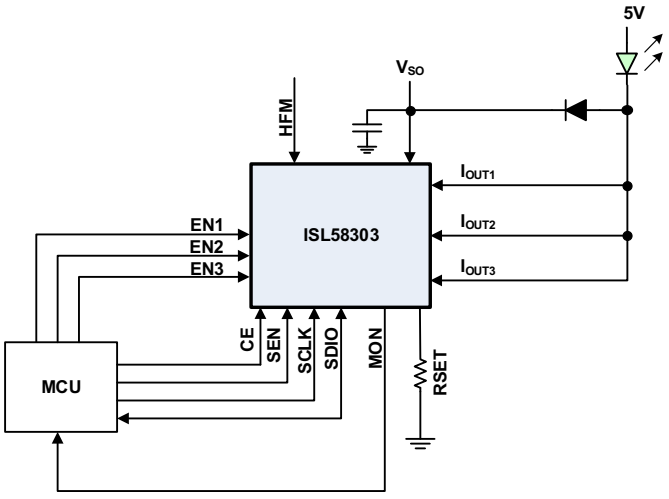

FIGURE 2. ISL58303 TYPICAL APPLICATION HIGH CURRENT

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Block Diagram

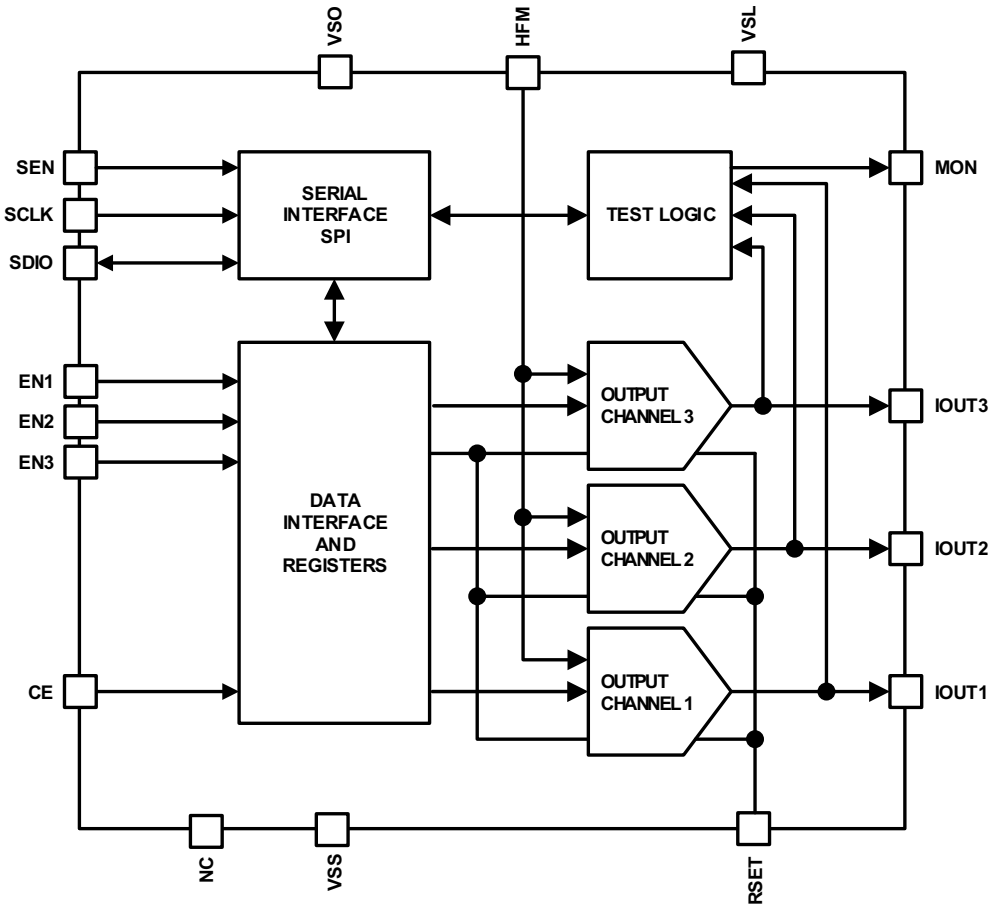


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Ordering Information

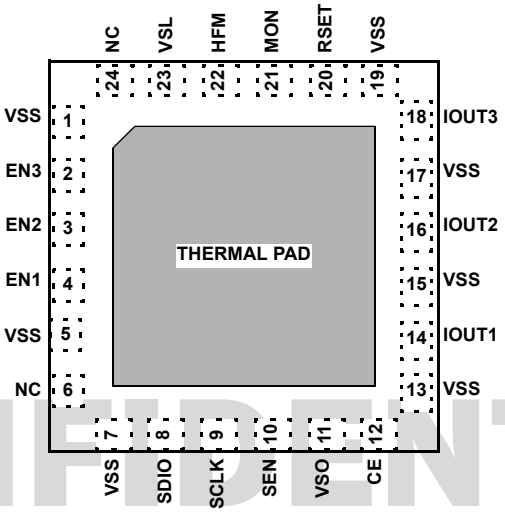
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT	PKG. DWG. #
ISL58303DRTZ	583 03DRTZ	-10 to +85	-	24 Ld TQFN	L24.4x4E
ISL58303DRTZ-T7A	583 03DRTZ	-10 to +85	250	24 Ld TQFN	L24.4x4E
ISL58303DRTZ-T13	583 03DRTZ	-10 to +85	6k	24 Ld TQFN	L24.4x4E
ISL58303DRTZ-EVAL	Evaluation Board				

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL58303 For more information on MSL please see techbrief TB363.

Pin Configuration

ISL58303
(24 LD TQFN)
TOP VIEW



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NOTE: All drawings are from the top view looking through the package as if it were transparent.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION
12	CE	Digital	CE is an active high signal. When high enables LDD's operation. 500k pull-up to VSO.
22	HFM	Digital	High frequency input that enables/disables all color DAC currents. A '0' enables the IOUT pins.
2	EN3	Digital	Enable control for IOUT3. Active high (2.75V maximum).
3	EN2	Digital	Enable control for IOUT2. Active high (2.75V maximum).
4	EN1	Digital	Enable control for IOUT1. Active high (2.75V maximum).
10	SEN	Digital	SEN is the SPI serial interface enable strobe. This is an active high signal.
9	SCLK	Digital	SCLK is the SPI serial interface clock.
8	SDIO	Digital	SDIO is the SPI serial interface bidirectional data.
18	IOUT3	Analog	Current sink from laser cathode to ground for Channel 3.
16	IOUT2	Analog	Current sink from laser cathode to ground for Channel 2.
14	IOUT1	Analog	Current sink from laser cathode to ground for Channel 1.
20	RSET	Analog	A resistor from RSET to ground sets the chip bias current level. All chip reference currents are derived from R_{SET}. Place resistor close to pin. Typical value used is 620Ω 1% tolerance.
11	VSO	Power	One VSO pin provides power to the device.
23	VSL	Power	This pin is used to provide decoupling for the internal 2.5V logic power, which also supplies all the digital pins. There is an internal regulator generating this voltage from VSO.
1, 5, 7, 13, 15, 17, 19	VSS	Power	All of the GND pins are common in the chip. GND connections should be made on the PCB to all GND pins.
21	MON	Digital	Monitor pin for factory testing. Pin must be left open.
6, 24	NC		No connect. This pin should be tied to ground pin for added thermal dissipation path.
	PAD		Thermal pad should be tied to ground and a heatsink.

Absolute Maximum Ratings T_A = +25°C

Supply Voltage VSO 6.0V
Voltage at I_{OUT1} I_{OUT2} I_{OUT3}, continuous 6.0V
Output Current, continuous 1000mA
Logic Input Voltages EN1, EN2, EN3 . . . . . 3.0V
Logic Input Voltages Other pins . . . . . -0.5V to VSO + 0.5V
Current into R_{SET} 5mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V
Charge Device Model (Tested per JESD22-C101C) 1kV
Latch-Up (Tested per JESD-78; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld TQFN (Notes 4, 5)	42	5

Operating Temperature Range . . . . . -10°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -10°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

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IMPORTANT NOTE: Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

DC Electrical Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C, all registers set to default conditions.

PARAMETER	DESCRIPTION	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{So}	Supply Voltage	3.0		5.5	V
I_{S-DIS}	Supply Currents, Disable Mode		0.4	1	mA
I_{S-OEN}	VSO Current, CE = '1', EN1 or EN2 or EN3 = '1'		14	20	mA
I_{S-ODIS}	VSO Current, CE = '1', EN1 = EN2 = EN3 = '0'		11	16	mA
V_{IH}	Input Logic High Level - All Logic Inputs Except HFM	1.8			V
V_{IL}	Input Logic Low Level - All Logic Inputs Except HFM			0.8	V
V_{Th-HFM}	Logic Threshold of the HFM Pin	1.00	1.25	1.50	V
V_{OH}	High Level, I_L = -5mA, SDIO	2.4			V
V_{OL}	Low Level, I_L = 5mA, SDIO			0.4	V
I_{INH}	Input Current High Level	-2		+2	µA
I_{INL}	Input Current Low Level (Note 6)	-2		+2	µA

ISL58303 I_{OUT1} and I_{OUT3} Color DACs DC Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C, all registers set to default conditions.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT1_{MAX}$	Maximum Output Current (Note 10)	Input code = FFh, $V_{HEADROOM}$ > 1.5V	700	800		mA
$IOUT3_{MAX}$	Maximum Output Current (Note 10)	Input code = FFh, $V_{HEADROOM}$ > 1.5V	580	665		mA
t_{RISE}	Rise Time	10% to 90% from zero to $IOUT_{MAX}$ at 1.5V headroom		1.5		ns
t_{FALL}	Fall Time	10% to 90% from $IOUT_{MAX}$ to zero at 1.5V headroom		1.5		ns
$t_{DEL-RISE}$	HFM Propagation Delay Rising Edges	HFM rising 50% point to I_{OUT1} or I_{OUT3} 50% point	2.5	3.5	5.0	ns
$t_{DELAY-FALL}$	HFM Propagation Delay Falling Edges	HFM falling 50% point to I_{OUT1} or I_{OUT3} 50% point	2.5	3.5	5.0	ns

I_{OUT2} Color DACs DC Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C, all registers set to default conditions.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
$IOUT2_{MAX}$	Maximum Output Current (Note 10)	Input code = FFh, $V_{HEADROOM}$ > 1.5V	700	765		mA
t_{RISE}	Rise Time	10% to 90% from zero to $IOUT_{MAX}$ at 1.5V headroom		1.5		ns
t_{FALL}	Fall Time	10% to 90% from $IOUT_{MAX}$ to zero at 1.5V headroom		1.5		ns
$t_{DEL-RISE}$	HFM Propagation Delay Rising Edges	HFM rising 50% point to I_{OUT2} 50% point	2.5	3.5	5.0	ns
$t_{DELAY-FALL}$	HFM Propagation Delay Falling Edges	HFM falling 50% point to I_{OUT2} 50% point	2.5	3.5	5.0	ns

HFM to I_{OUT} Delay Skew Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
t_{SKEWx}	Skew Between All I_{OUT} Pins	Default		250	1000	ps
$T_{SKEW-ALL}$	Skew Across All Parts	Longest HFM to IOUTx - Shortest HFM to IOUTx propagation delay			1.5	ns
$t_{DEL-TEMPCO}$	HFM Propagation Delay Tempco	HFM rising 50% point to I_{OUT} 50% point over the operating temperature range	3		7	ps/°C

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I_{OUT} $I_{THRESHOLD}$ DAC DC Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$IOUT_{MAX}$	Maximum Output Current	Input code = FFh, $V_{HEADROOM}$ > 500mV	335	400		mA

I_{OUT} Color and Threshold Scale DAC (8-Bit) DC Specifications

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, R_{LOAD} = 4.3Ω to 5V, Color DAC = 0xFF, T_A = +25°C.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
G_{SLOPE}	Slope Gain	Gain adjustment range over all segment	0		100	%
DNL-PMAX	Differential Nonlinearity	Worst of all adjacent codes (Note 7)		1	5	LSB

SPI Serial Interface AC Performance

Unless otherwise indicated: V_{SO} = 5V, R_{SET} = 620Ω, SCLK = 50MHz.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
F_{SER}	SCLK Maximum Operating Frequency		50			MHz
t_{EL}	SEN “L” Time		20			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Rising Edge		10			ns
t_{DS}	SDIO Set-Up Time		5			ns
t_{DH}	SDIO Hold Time		5			ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge		10			ns
t_{CC}	SCLK Cycle Time1		20			ns
t_{CH}	SCLK High Time	t_{CL} = 12ns	8			
t_{CL}	SCLK Low Time	t_{CH} = 12ns	8			

NOTES:

6. CE has a 500k pull-up to VSO.
7. Differential Nonlinearity (DNL) is the differential between the measured and ideal 1 LSB change of any two adjacent codes.
8. See timing diagrams Figures 6 and 7 for details.
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
10. Decreasing the value of RSET from the default of 620Ω will increase the output current, 800mA can always be achieved.

Block Diagram

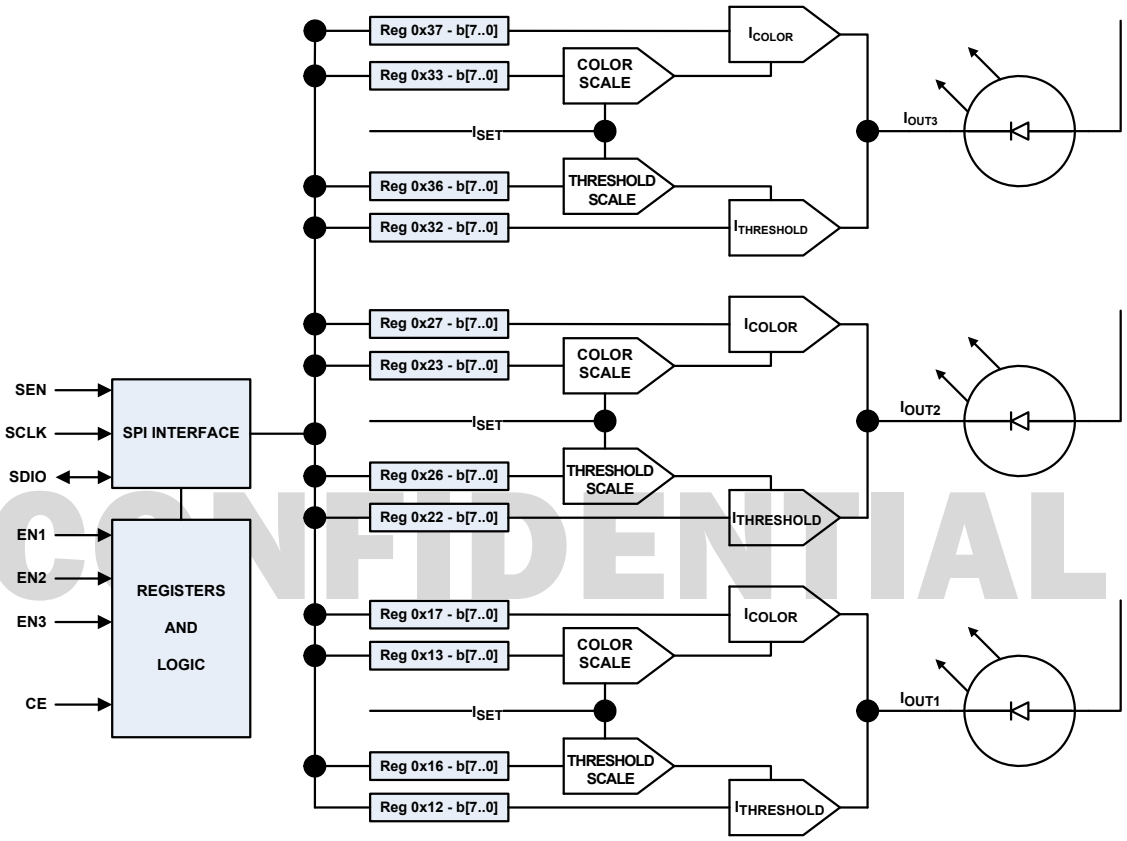

FIGURE 4. OUTPUT BLOCK DIAGRAM

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Functional Description

Figure 4 shows the major functional blocks of the ISL58303. There are output blocks that are the same at the block level with 4 DACs each with a control register. There are slight performance differences between the outputs, which are detailed in the electrical specifications.

Chip Enable (CE)

The device operates normally when CE is asserted high. When CE is deasserted the IC is disabled and enters sleep mode where the bias current for all output channels shuts down.

The CE signal is ANDed internally with a register chip enable bit (Reg. 0x07 b0). Both hardware pin and register bit must be asserted for the IOUT pins to operate normally. This adds a level of operational safety in preventing accidental hardware failure.

Output Enables

The ISL58303 has three DAC outputs (I_{OUT1}, I_{OUT2} and I_{OUT3}) to drive red, green and blue lasers. Each output has its own enable pin. EN1, EN2 and EN3 are enable pins that control I_{OUT1}, I_{OUT2} and I_{OUT3} outputs, respectively. When the EN pin is asserted high, the respective output is biased for operation.

HFM (High Frequency Modulation)

HFM is a high speed enable/disable pin, which is active ‘0’. Since a laser illumination source creates a speckling effect on non-uniform surfaces, the ISL58303 provides an electrical means to reduce laser speckle. Applying a high frequency signal to the HFM pin modulates all 3 I_{OUT} color DAC outputs simultaneously.

To execute the HFM function, an external clock oscillator must be employed.

If the HFM function is not desired in a system, this pin should be pulled to GND through a resistor (10kΩ is a good value).

Note: Threshold DAC currents are not switched by HFM.

Color DAC Outputs

The ISL58303 has 3 identical current sink outputs. This enables the system designer to place red, green and blue laser diodes in any physical order.

All Color DACs, when enabled, sink current proportional to their respective registers values.

Threshold DAC

Each output has a threshold current DAC. The I_{OUT} current is directly proportional to the product of the threshold scale and

threshold registers. This provides a means to always use the full range (8 bits) of the threshold DACs and the highest possible resolution.

Color DAC

Each output has a color (color intensity) current DAC. The reference input of the Color DACs is set by the color scale DACs. This provides a means to always use the full range (8 bits) of the color DACs and maintain the highest resolution.

Ganging of Outputs

To achieve greater current drive, 2 or all 3 IOUT pins can be ganged together allowing up to 2.4A of current from a single chip. Ganging of outputs can be extended to multiple devices making the board layout and heat dissipation the limiting factors in the maximum achievable current. When ganging multiple devices, power, ground, enable, SPI and HFM signals are shared between all chips. If the user requires independent control of each chip separate SEN signals would be required.

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Power-Up Sequence

With VSO powered and GND connected register writes and reads can be performed through the SPI interface. The Laser VDD is required for the chip-to-sync current through the IOUTx pins.

Internal Sampler

An 8-bit ADC is accessible through the SPI interface, which allows the user to sample the voltage on each of the IOUT pins as well as several internal nodes. The ADC can be multiplexed to measure the internal logic $V_{DD\ (VSL)}$, a temperature reference, the RSET voltage, VSO voltage and GND.

The sampler can be configured to perform a capture at either Color Intensity code 0x00 or 0xFF. There are 4 conversion rate settings and a peak detector. The ADC is linear between 1V and 3.5V.

VSL Decoupling

A single 0.1µF or larger capacitor must be placed as closely to the VSL pin as the board layout allows. This provides decoupling for the internal regulator that generates VSL.

RSET Scaling

The RSET pin controls an analog scaling function that adjusts the output drive current of the IOUT pins. This pin can be used to fine tune the current drive so that I_{OUT} current can be limited to safe values for the laser. RSET can also be lowered so that the LSB size of the current DACs is smaller, which raises the resolution. RSET current is adjusted up or down by changing the external resistor.

SPI Serial Interface

The device register values must be programmed into the registers after Power-On Reset (POR) has settled (25ms is enough time). A host MCU can then write operational values into the DAC registers via the SPI interface. Each channel's laser threshold, threshold scale, color intensity, color scale and chip status can be accessed independently through this interface.

When performing a register read operation, some devices will not always return the correct value. Performing two back-to-back reads will always return the correct register value. The SPI serial bus interface consists of 3 signals; SEN, SCLK and SDIO. Figures 6 and 7 show the SPI serial interface Read and Write cycle timing diagrams respectively. In the case of tying more than one ISL58303 in parallel to drive higher current, a separate SEN signal for each device is required to properly interface to each device. SCLK and SDIO can be shared between devices.

See the timing parameter definitions in "SPI Serial Interface AC Performance" on page 5.

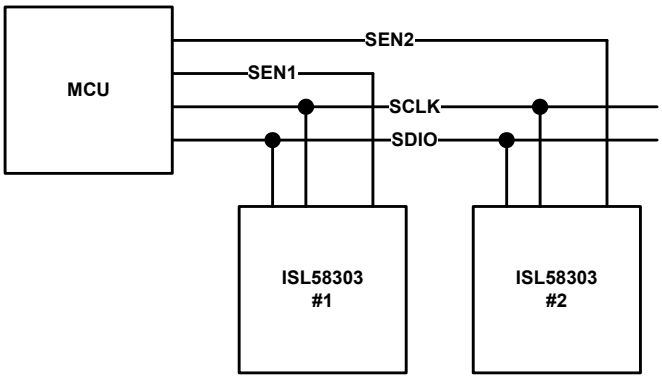

FIGURE 5. INTERFACING MULTIPLE LASER DIODE DRIVERS

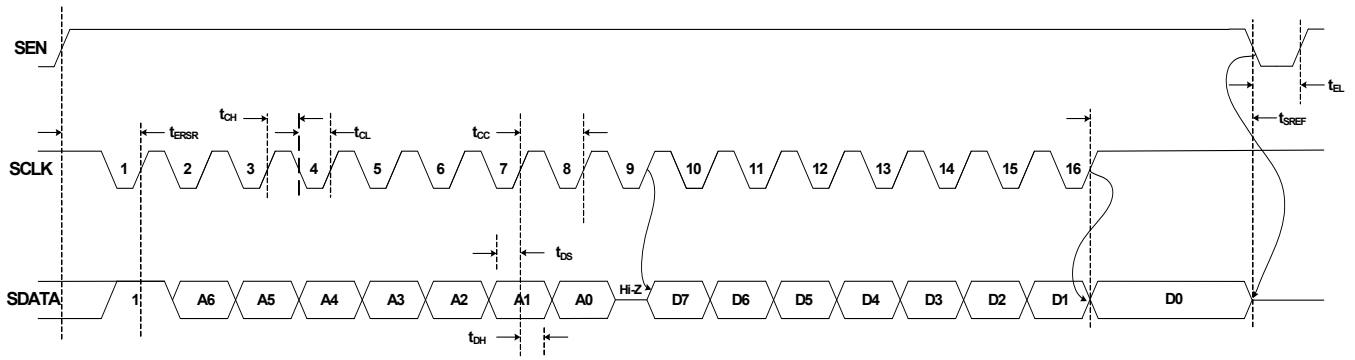

FIGURE 6. SPI SERIAL INTERFACE READ CYCLE TIMING DIAGRAM

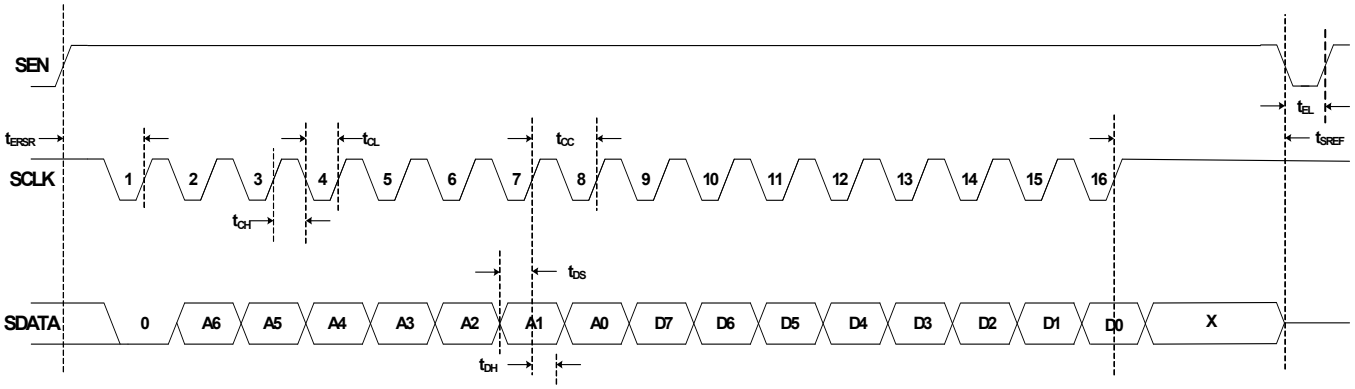

FIGURE 7. SPI SERIAL INTERFACE WRITE CYCLE TIMING DIAGRAM

Layout Recommendations

The AC performance of this circuit depends greatly on the care taken in designing the PC board. If high-speed modulation is used, it is important to control the impedance of the HFM signal traces. To insure high-speed laser performance, series inductance from the laser power supply to the ISL58303 device (both sides of the laser) and from the device to ground must be minimized. Draw the traces from VDD_{LASER} as short and wide as practical. There should be no vias in this path. A good low inductance grounding strategy is shown in Figure 8.

Thermal Considerations

With the capability of driving 2.4A of laser current, an efficient strategy for removing heat from the device is critical. Figure 8 shows the recommended footprint for extracting heat from the ISL58303 device. 9 vias should connect the thermal pad to the board ground plane. The via should be fully connected (360°) to the thermal pad and the ground plane. Use 9 vias with 0.3mm drill size filled with 1oz or more of copper.

Note: There is no built-in thermal shutdown.

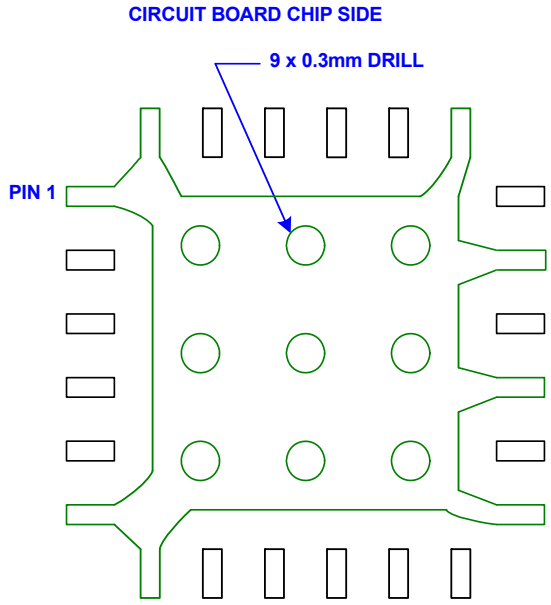

FIGURE 8. RECOMMENDED DEVICE FOOTPRINT

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Thermal Information" on page 4. The power dissipation can be calculated by using Equation 1:

$$P_D = V_{HR} \times (I_{OUTAVE} + I_{TH}) + I_{VSO} \times VSO \quad \text{(EQ. 1)}$$

V_{HR} stands for headroom voltage and is defined as the voltage on the IOUT pin or pins when sinking current. V_{HR} is the supply voltage on the load (usually a laser) minus the IR drop across the load. Larger headroom voltages will result in faster rise times and larger output current for a given code but at the expense of power dissipation. There is very little performance gains for headroom values above 2.0V.

I_{OUTAVE} is proportional to the programmed Color DAC current times the duty cycle of the HFM signal. I_{VSO} will depend on the number of enabled channels and the value programmed in the Color Scale DAC. I_{TH} is the programmed threshold current, which is not switched by HFM so it has a 100% duty cycle.

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The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 2:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 2)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 1, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The QFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane).

Register Map

ADDR	NAME	DESCRIPTION	ACCESS	DEFAULT
0x01	Chip ID	Chip revision ID	R	0xE3
0x02	Serial Control	Serial control	R/W	0x00
0x03	Status	Status bits	R	0x00
0x06	SDIO	Sets the SDIO operating voltage	R/W	0x00
0x07	Enable 0	Enable various parts of the chip	R/W	0x00
0x12	I_{OUT1} $I_{THRESHOLD}$ DAC	The I_{OUT1} threshold register	R/W	0x00
0x13	I_{OUT1} Color Scale	The I_{OUT1} color scaling register	R/W	0x00
0x16	I_{OUT1} Threshold Scale	The I_{OUT1} threshold scaling register	R/W	0x00
0x17	I_{OUT1} Color DAC	The I_{OUT1} color DAC register	R/W	0x00
0x22	I_{OUT2} $I_{THRESHOLD}$ DAC	The I_{OUT2} threshold register	R/W	0x00
0x23	I_{OUT2} Color Scale	The I_{OUT2} color scaling register	R/W	0x00
0x26	I_{OUT2} Threshold Scale	The I_{OUT2} threshold scaling register	R/W	0x00
0x27	I_{OUT2} Color DAC	The I_{OUT2} color DAC register	R/W	0x00
0x32	I_{OUT3} $I_{THRESHOLD}$ DAC	The I_{OUT3} threshold register	R/W	0x00
0x33	I_{OUT3} Color Scale	The I_{OUT3} color scaling register	R/W	0x00
0x36	I_{OUT3} Threshold Scale	The I_{OUT3} threshold scaling register	R/W	0x00
0x37	I_{OUT3} Color DAC	The I_{OUT3} color DAC register	R/W	0x00
0x40	ADC Resource Select	Selects the node to be measured	R/W	0x00
0x41	ADC Measurement Result	Contains the result of the latest ADC measurement	RO	0x00
0x42	ADC Control Register 1	ADC block configuration	R/W	0x00
0x43	ADC Control Register 2	ADC block configuration	R/W	0x00

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Register Descriptions

TABLE 1. SERIAL CONTROL REGISTER. . . . . .ADDRESS: 0x01

BIT	NAME	BIT DEFINITION
B7-B0	Chip ID	This is a read only register used for chip identification (returns E3).

TABLE 2. SERIAL CONTROL REGISTER. . . . . .ADDRESS: 0x02

BIT	NAME	BIT DEFINITION
B7-B6	Reserved	Do not modify
B5-B4	Page Select	B5: B4: (Access to reserved pages could cause adverse effect). 0:0 = the default page 0:1 = Reserved 1:0 = Reserved 1:1 = Disable serial
B3-B0	Reserved	Do not modify

TABLE 3. STATUS REGISTER . . . . . ADDRESS: 0x03

BIT	NAME	BIT DEFINITION
B7-B1	Reserved	Do not modify
B0	Power Good	1: VSO is above the shutdown trip point. 0: VSO is below the shutdown trip point.

TABLE 4. SDIO REGISTER. . . . . ADDRESS: 0x06

BIT	NAME	BIT DEFINITION
B7	SDIO Voltage	1: Sets serial interface to operate at 1.8V. 0: Sets the Serial interface to operate at 3.3V (default).
B6-B0	Reserved	Do not modify

TABLE 5. ENABLE REGISTER . . . . . ADDRESS: 0x07

BIT	NAME	BIT DEFINITION
B7,B6	Reserved	Do not modify
B5	Sampler Enable	1: Enables the analog in the sampler block. 0: Disables the analog in the sampler block and saves current.
B4-B1	Reserved	Do not modify
B0	Chip Enable	1: Enables chip. This bit is physically ANDed internally with the CE pin. Both must be enabled. 0: Disables chip (default)

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TABLE 6. I_{OUT1} THRESHOLD DAC REGISTER. . . . . ADDRESS: 0x12

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} threshold	These bits are the input data bits of the I_{OUT1} Threshold Current DAC. I_{OUT1} Threshold Current = Gain x I_{OUT1} Threshold Scale x (128B7 + 64B6 + 32B5 + ... 4B2 + 2B1 + B0)/255

TABLE 7. I_{OUT1} COLOR SCALE REGISTER. . . . . ADDRESS: 0x13

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} Color Scale	These bits are the input bits of the I_{OUT1} Color Scale DAC. I_{OUT1} Color Scale = Gain (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

TABLE 8. I_{OUT1} THRESHOLD SCALE REGISTER. . . . . ADDRESS: 0x16

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} Threshold Scale	These bits are the input for the I_{OUT1} Threshold Scale DAC. I_{OUT1} Threshold Scale = (128B7 + 64B6 +32B5 +... 4B2 + 2B1 + B0)/255

TABLE 9. I_{OUT1} COLOR DAC REGISTER . . . . . ADDRESS: 0x17

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT1} COLOR	These bits are the input for the I_{OUT1} COLOR DAC. I_{OUT1} COLOR = (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)

TABLE 10. I_{OUT2} THRESHOLD DAC REGISTER. . . . . ADDRESS: 0x22

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} $I_{THRESHOLD}$	These bits are the input data bits of the I_{OUT2} Threshold Current DAC. I_{OUT2} Threshold Current = Gain x I_{OUT2} Threshold Scale x (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

TABLE 11. I_{OUT2} COLOR SCALE REGISTER . . . . . ADDRESS: 0x23

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} Color Scale	These bits are the input bits of the I_{OUT2} Color Scale DAC. I_{OUT2} Color Scale = Gain (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

TABLE 12. I_{OUT2} THRESHOLD SCALE REGISTER. . . . . ADDRESS: 0x26

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} Threshold Scale	These bits are the input for the I_{OUT2} Threshold Scale DAC. I_{OUT2} Threshold Scale = (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

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TABLE 13. I_{OUT2} COLOR DAC REGISTER . . . . . ADDRESS: 0x27

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT2} COLOR	These bits are the input for the I_{OUT2} COLOR DAC. I_{OUT2} COLOR = (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)

TABLE 14. I_{OUT3} THRESHOLD DAC REGISTER. . . . . ADDRESS: 0x32

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} $I_{THRESHOLD}$	These bits are the input data bits of the I_{OUT3} Threshold Current DAC. I_{OUT3} Threshold Current = Gain x I_{OUT3} Threshold Scale x (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

TABLE 15. I_{OUT3} COLOR SCALE REGISTER . . . . . ADDRESS: 0x33

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} Color Scale	These bits are the input bits of the I_{OUT3} Color Scale DAC. I_{OUT3} Color Scale = Gain (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255.

TABLE 16. I_{OUT3} THRESHOLD SCALE REGISTER. . . . . ADDRESS: 0x36

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} Threshold Scale	These bits are the input for the IOUT3 Threshold Scale DAC. I_{OUT3} Threshold Scale = (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)/255

TABLE 17. I_{OUT3} COLOR DAC REGISTER. . . . . ADDRESS: 0x37

BIT	NAME	BIT DEFINITION
B7-B0	I_{OUT3} COLOR	These bits are the input for the I_{OUT3} COLOR DAC. I_{OUT3} COLOR = (128B7 + 64B6 + 32B5 +... 4B2 + 2B1 + B0)

TABLE 18. ADC RESOURCE SELECT . . . . . ADDRESS: 0x40

BIT	NAME	BIT DEFINITION
B7	Sample Code Select	This bit selects the code of the color intensity DAC that will enable I_{OUTx} sampling. 1: VOUTx will be sampled if color = 0xFF 0: VOUTx will be sampled if color = 0x00
B6, B5	IOUT Select	The bits select which of the I_{OUT} voltages to sample. :11 - I_{OUT3} :10 - I_{OUT2} :01 - I_{OUT1} :00 - No I_{OUTx} Sampled

TABLE 19. ADC MEASUREMENT RESULT . . . . . ADDRESS: 0x41

BIT	NAME	BIT DEFINITION
B7-B0	ADC Value	8-bit value captured by the ADC.

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TABLE 20. ADC CONTROL REGISTER 1 . . . . . ADDRESS: 0x42

BIT	NAME	BIT DEFINITION
B7	Start	Write to B7 a 1 to start conversion. When conversion is complete, a read will give B7 = 0.
B6	ADC Power	0: The ADC will be powered down. 1: The ADC will be powered up.
B5, B4	ADC CLK	Conversion time = 10µs (2B5 + B4)/3 + 500ns (approximately)
B3	Reserved	Do not modify
B2 - B0	ADC Input	:000 = GND :001 = RSET resistor voltage (1.07V regardless of RSET) :010 = GND :011 = Internal Logic Supply (~2.5V) :100 = Die temperature :101 = GND :110 = Monitor Pin Voltage (Diagnostics only) :111 = Laser Diode Sampled Voltage (Select IOUT pin reg 0x40 B6, B5)

TABLE 21. ADC CONTROL REGISTER 2 . . . . . ADDRESS: 0x43

BIT	NAME	BIT DEFINITION
B7	ATE Test	1: Enables ATE test 0: Means normal operation
B6 - B4	Reserved	Do not modify
B3	Attenuator Bypass	1: The attenuator preceding the ADC is bypassed (no attenuator). 0: The attenuator preceding the ADC is in the path.
B2	Sample VSO	1: VSO is sampled 0: IOUTx branch is sampled (IOUTx channel selected by reg 0x40 B6, B5).
B1, B0	Reserved	Do not modify

Performance Graphs

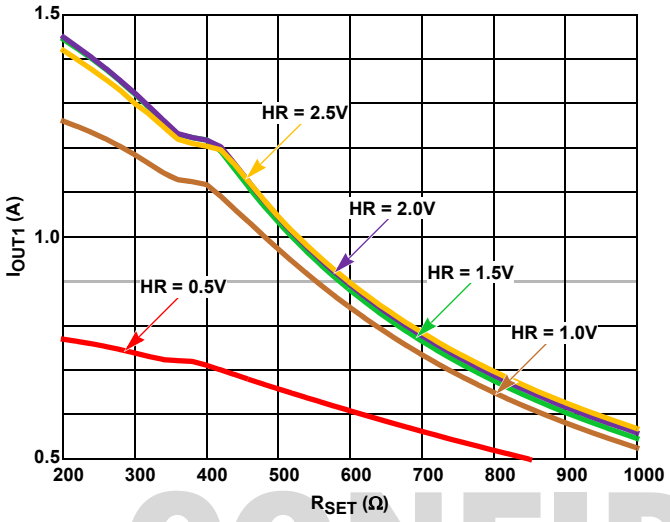

FIGURE 9. I_{OUT1} vs R_{SET} FOR DIFFERENT HEADROOM VOLTAGES

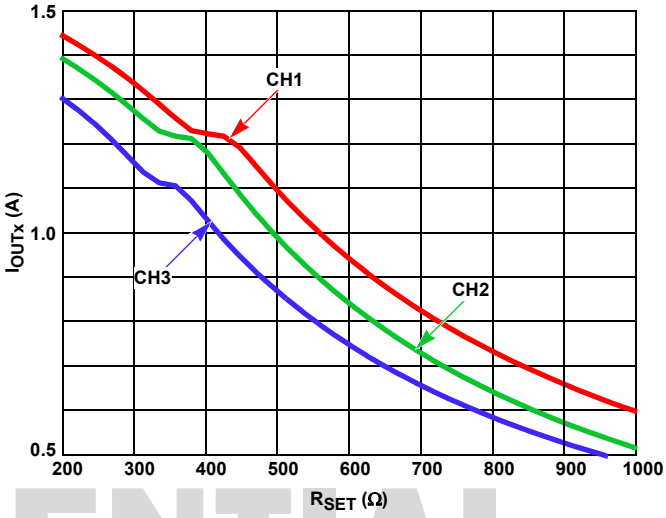

FIGURE 10. I_{OUTx} CURRENT vs R_{SET}, HEADROOM = 1.5V

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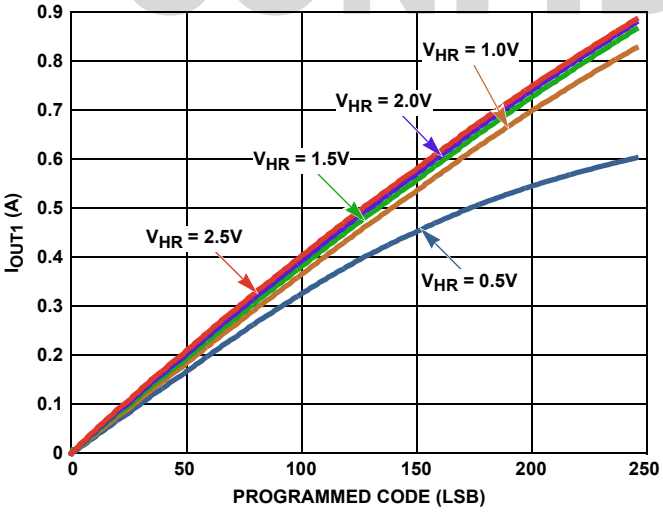

FIGURE 11. I_{OUT1} vs CODE FOR DIFFERENT HEADROOM VOLTAGES

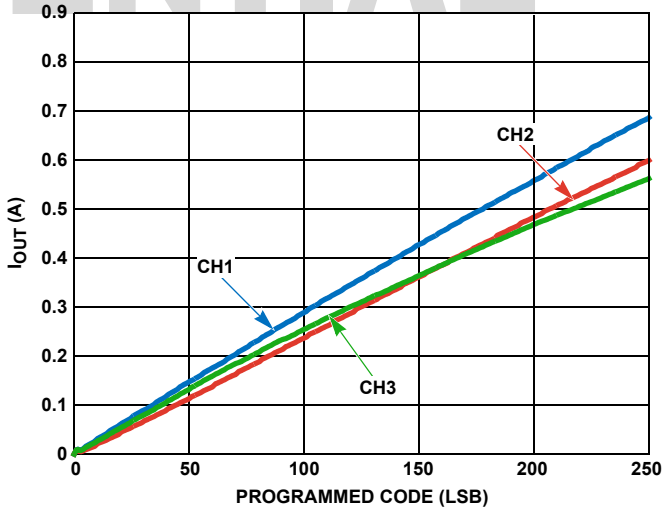

FIGURE 12. I_{OUT} vs PROGRAMMED CODE CHANNEL COMPARISON

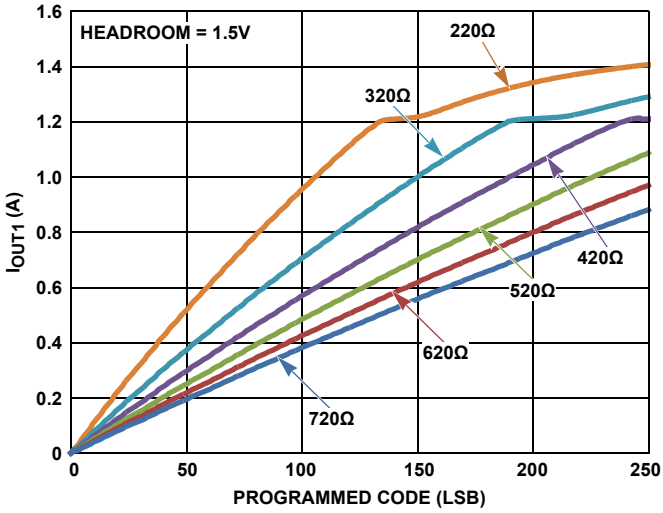

FIGURE 13. I_{OUT1} vs PROGRAMMED CODE FOR DIFFERENT R_{SETs}

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
September 1, 2016	FN7555.3	Updated Figure 1 on page 1 by replacing EL6203 with EL6204. Updated “Ordering Information” table on page 2 by changing minimum in Temperature Range from 0° to -10. “Thermal Information” on page 4 - Updated the minimum operating temperature range and minimum operating junction temperature from 0°C to -10°C.
February 16, 2016	FN7555.2	Updated the Ordering Information table on page 2. On page 5, removed t_{DE} specification and removed t_{DE} from Figure 6 on page 8.
May 9, 2014	FN7555.1	page 9- Power Dissipation, corrected Equation 1 and added descriptions for all terms Page 17- Removed PMOS output graphs page 5- Added $T_{SKEW-ALL}$ in specification page 8- Modified Figures 6 and 7, SPI Timing Diagrams Major revision touching most of the document Removed all references to the ISL58304 Added new performance graphs Added diagrams and text referring to gesture and ganged applications Updated POD to most recent revision with following changes: Bottom View - Changed Exposed paddle dimension from 2.50 to 2.60 Made correction in Typical land pattern - added 0 to 0.250 Added tolerance to Exposed DAP in Bottom view. From: 2.60 sq. To: 2.60 ± 0.10 with added square graphic in front of the 2.60
June 20, 2012	FN7555.0	Initial release.

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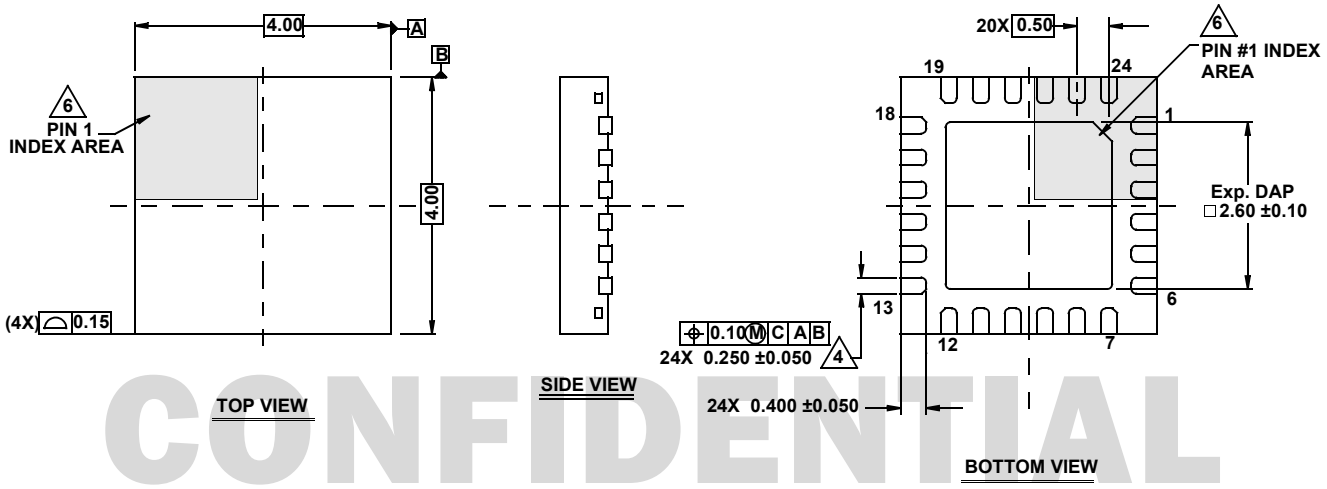
Package Outline Drawing

L24.4x4E

24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 2, 2/14



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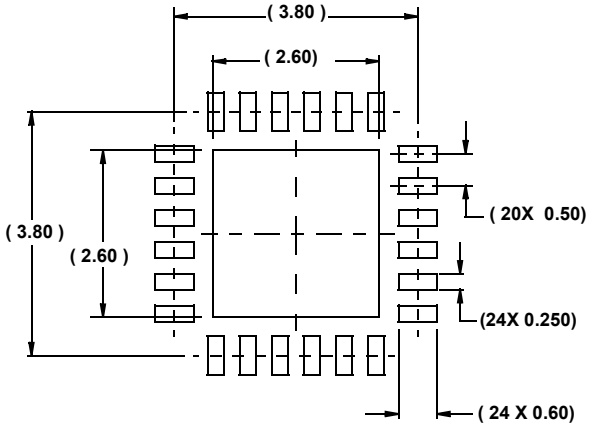
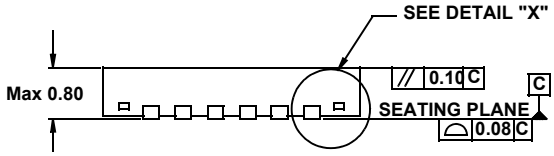
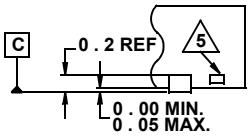


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.