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ISL58214

Programmable High Speed Single Channel Laser Diode Driver

FN6944
Rev 2.00
April 14, 2015

The ISL58214 is a highly integrated laser diode driver designed to support a laser beam scanning MEMS projector. Operating from a single 5V analog supply, it directly drives either a cathode-grounded laser, or a floating laser whose anode is connected to a high voltage supply. The ISL58214 is configured through a serial interface.

An integrated 10-bit high power DAC drives the selected laser. The desired current level can be scaled by a 10-bit DAC programmed through a serial interface or the I_{SLOPE} pin to compensate for ambient brightness, speed variation or laser sensitivity change.

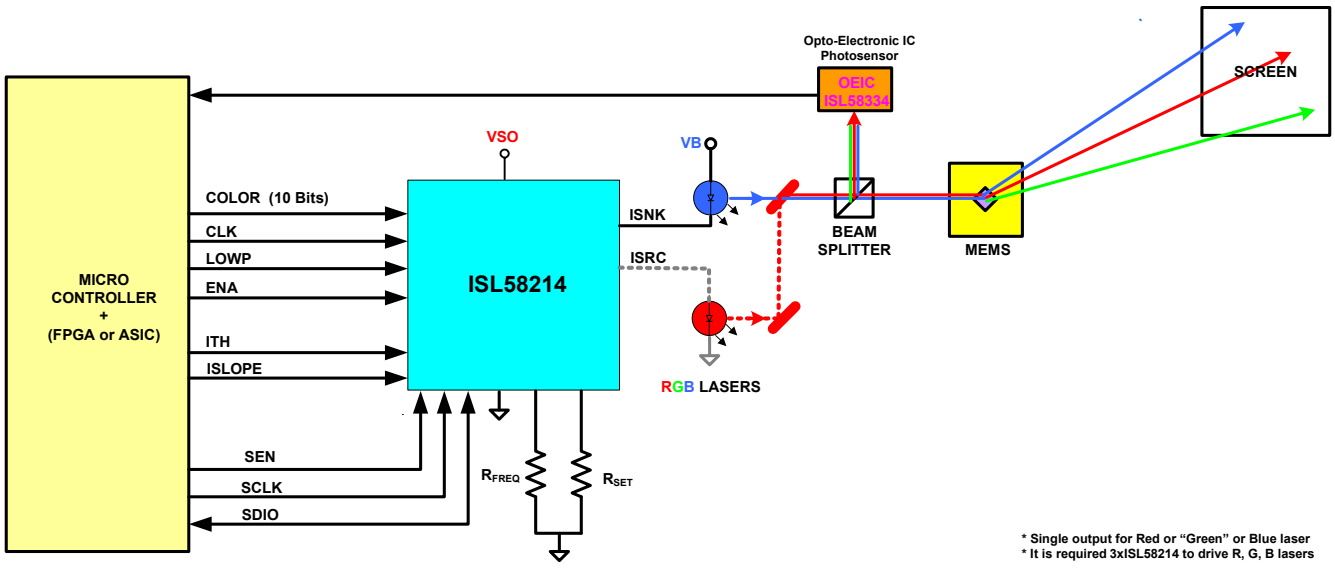
The CLK pin clocks in the data on the rising edge of CLK. The LOWP line gates the output off when HIGH.

Features

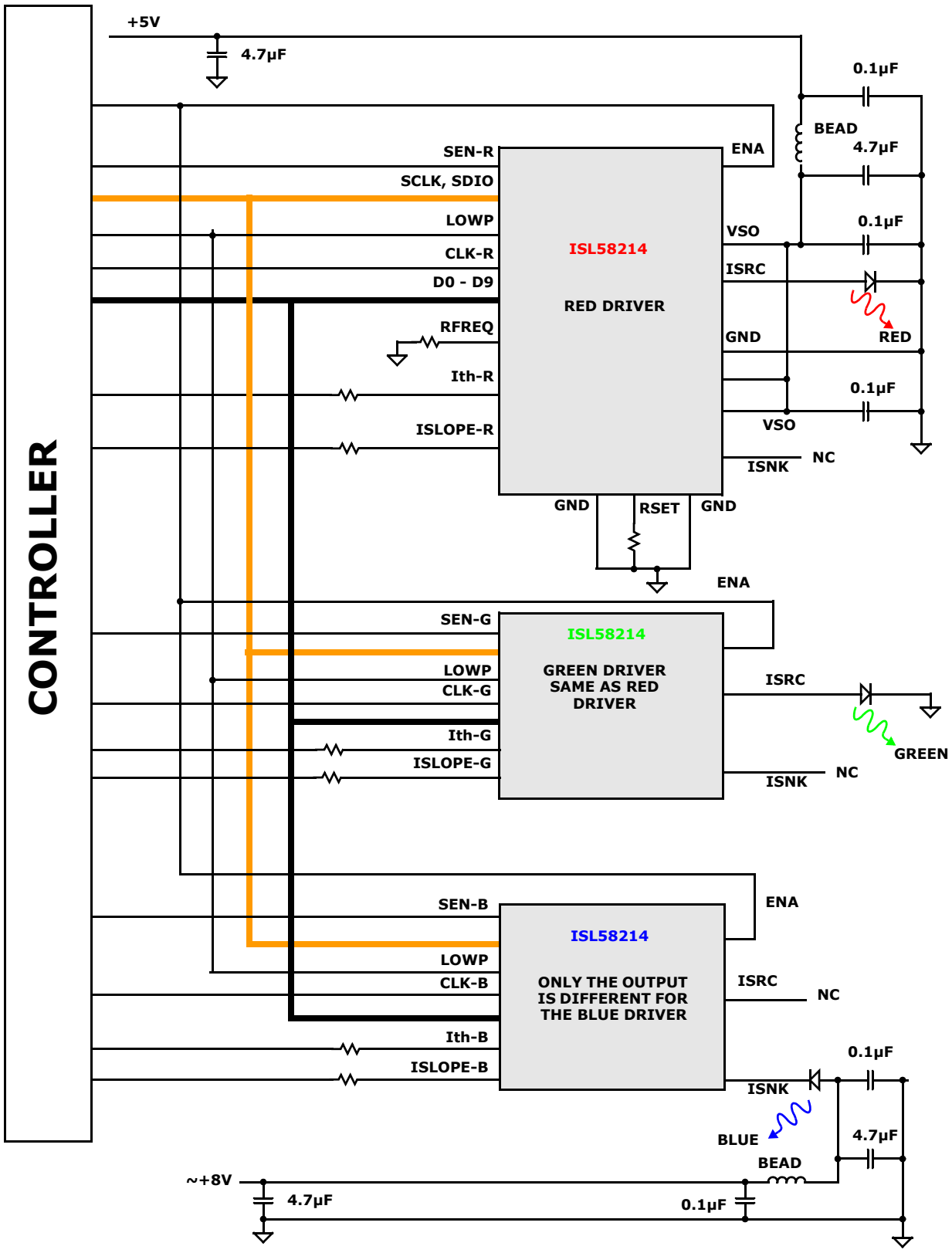
- Direct drive for floating laser, or cathode grounded. Supports Red, 'Green' or Blue laser
- Up to 1000mA maximum total output (I_{SRC}) with 1.5ns typical tr/tf
- Up to 500mA maximum total output (I_{SNK}) with 1ns typical tr/tf.
- 10-bit x 10-bit multiplying DAC output provides 10-bit full scale adjustment and 10-bit resolution at any full scale output
- I_{SLOPE} input allows compensation for laser slope, ambient light, and sweep speed variation
- High-speed SPI Serial input works up to 50MHz
- 10-bit video code capable of operating up to 100MHz pixel data rate
- Integrated programmable HFM (High Frequency Modulation) for laser stabilization and speckle reduction
- Pb-free (RoHS compliant)

Applications

- RGB laser based projector or pico projector
- Hand held projector
- General purpose laser diode driver
- General purpose high current driver/controller

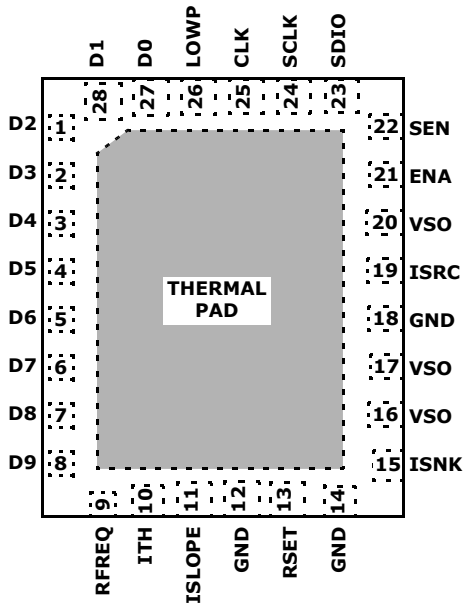


System Block Diagram



Pin Configuration

ISL58214
(28 LD QFN)
TOP VIEW



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL58214CRZ-T13	58214 CRZ	28 Ld QFN	L28.4x5A
ISL58214CRZ-EVAL	Evaluation Board		

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL58214. For more information on MSL please see techbrief TB363.

Pin Descriptions

PIN #	PIN NAME	I/O	PIN TYPE	PIN DESCRIPTION
27, 28, 1, 2, 3, 4, 5, 6, 7, 8	D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	Input	Digital	These inputs specify the color current. I_{COLOR} = Imax (512*D9 + 256*D8 + ... 4*D2 + 2*D1 + D0). Imax is set by the scale DAC register (Page 0, Addr 15h), I_{SLOPE}, and RSET.
9	RFREQ	Input	Analog	The resistor to GND sets the reference for the HFM (anti-speckle) oscillator.
10	Ith	Input	Analog	Current into this pin becomes laser Threshold current; it has a 1000Ω input impedance. The gain is programmable.
11	ISLOPE	Input	Analog	Current into this pin sets the full scale DAC amplitude
12, 14, 18	GND	GND	GND	Ground (connect all)
13	RSET	Input	Analog	RSET to GND is the reference for the current DAC.
15	ISNK	Output	Analog	Floating laser diode output. Laser anode tied to a high supply.
16, 17, 20	VSO	Power	Power	The +5V power for the output drivers (connect all)
19	ISRC	Output	Analog	The output current into a grounded anode laser diode
21	ENA	Input	Digital	When high the chip is enabled. When low, the chip is powered down and the outputs disabled.
22	SEN	Input	Digital	The enable for the serial port.
23	SDIO	I/O	Digital	The data for the serial port
24	SCLK	Input	Digital	Serial clock for SDIO data
25	CLK	Input	Digital	The Dn data is clocked in on the rising edge of CLK
26	LOWP	Input	Digital	When high the output is disable for laser safety
-	PD	Power	Analog	The thermal pad must be heavily grounded as a heat sink.

NOTE: Pins with the same name are internally connected together; however, LDD pins must not be used for connecting together external components or features.

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Absolute Maximum Ratings

V_{SO}, Supply Voltages 6V
V_{ISNK}, Voltage at I_{SNK} 7V
I_{SRC}, Output Current. 1000mApk
I_{SNK}, Output Current 600mApk
V_{IH_DATA}, Logic Input Voltages . . . . . -0.5V to Lesser of . . . . . V_{SO} + 0.5V or 3V
V_{IH}, Logic Input Voltages . . . . . -0.5V to V_{SO} + 0.5V
I_{IN}, Current into R_{SET}, R_{FREQ}, I_{APC} 5mA
ESD Rating
Human Body Model (Tested per JESD22-A114E). 2kV
Machine Model (Tested per JESD22-A115-A). 100V
Charged Device Model. 1500V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld QFN Package (Notes 4, 5)	37	2.9

T_S, Storage Temperature Range. . . . . -60°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

T_A, Temperature Range . . . . . -5°C to +85°C
T_J, Junction Temperature. . . . . -5°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

Unless otherwise indicated, all of the following tables are: $V_{SO} = V_{HI} = 5V$, $R_{SET} = 620\Omega$, $R_{FREQ} = 4700\Omega$, CLK = 100MHZ, $R_{LOAD\text{-}ISRC} = 8\Omega$ to GND, $R_{LOAD\text{-}ISNK} = 10\Omega$ to V_{HI}, Scale DAC = 0x3FF, Reg 1-21 = 0x88, $T_A = +25°C$.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
DC ELECTRICAL SPECIFICATIONS					
V_{SO}	(Notes 6, 7)	4.5		5.5	V
I_{VSO}	Supply Current (No Current Output)		25	40	mA
I_S, dis	Supply Currents, Disable Mode		10	15	mA
V_{ISNK}	Allowable Operating Range of ISNK Pin (see Figure 2)			5.8	V
V_{IH_DATA}	Input Logic High Level for Data lines (D0-D9)	1.5		3	V
V_{IH}	Input Logic High Level	2.4			V
V_{IL}	Input Logic Low Level			0.8	V
V_{OH}	SDIO, Monitor Output High Level, I_L = -5mA	2.4			V
V_{OL}	SDIO, Monitor Output Low Level, I_L = 5mA			0.4	V
I_{INH}	Input Current High Level	-1		+1	µA
I_{INL}	Input Current High Level, except ENA pin	-1		+1	µA
I_{INL_ENA}	Input Current Low Level for ENA pin	-15		-5	µA

NOTES:

6. Required voltage at the device pins. Allowance must be made for any voltage drop between the power supply and the device.
7. Required voltage also depends on laser diode manufacturer and pickup optical efficiency.

Scale DAC (10-bit) DC Specifications

Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL-P_{SCALE}	Differential Non-Linearity	(Note 8)	-3.5		+2.5	LSB
INL-P_{SCALE}	Integral Non-Linearity	At 200h Resistive Load ~0V to ~3V		+40		LSB
ZS-P_{SCALE}	Zero-Scale Error	(Note 9)	-2	0	+2	LSB
V_{RSET}	RSET Pin Voltage		1.03	1.06	1.11	V

NOTE:

8. Differential non-linearity (DNL) is the differential between the measured and ideal 1 LSB change of any two adjacent codes.

I_{SLOPE} DC Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
R_{IN}	I_{SLOPE} Input Impedance to GND			570		Ω
$I_{GAIN\ SRC}$	I_{SLOPE} Current Gain to I_{SRC}	P_{SCALE} = 0x3FF, Input Code = 0x3FF		450		mA/mA
$I_{GAIN\ SNK}$	I_{SLOPE} Current Gain to I_{SNK}	P_{SCALE} = 0x3FF, Input Code = 0x3FF		135		mA/mA

I_{SRC} Color Power DAC (10-bit) DC Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL_{COLR_SRC}	Differential Non-Linearity		-2		+0.5	LSB
INL_{COLR_SRC}	Integral Non-Linearity			21		LSB
FS_{OUT}-H1.1	Input code Full-Scale Output Current Headroom = 1.1V	Input Code = 0x3FF, V_{ISRC} = 3.9V, VSO = 5.0V, R_{SET} = 620Ω	625			mA
$SFS_{OUT-COLR_SRC}$	Full-Scale Current Power Supply Rejection	vs V_{SO} (Note 10)		40		dB
$TFS_{OUT-COLR_SRC}$	Full-Scale Current Temperature Coefficient	(Note 11)		600		ppm/°C
ZS_{COLR_SRC}	Zero-Scale error	V_{ISRC} = 2V (Note 9)	-2	0	+2	LSB

I_{SNK} Color Power DAC (10-bit) DC Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL_{COLR_SNK}	Differential Non-Linearity		-4.9		+2.0	LSB
INL_{COLR_SNK}	Integral Non-Linearity			60		LSB
FS_{OUT}-620	Input code Full-Scale Output Current R_{SET} = 620Ω, Reg 1-21 = 0x88	Input code = 0x3FF	200	250		mA
$SFS_{OUT-COLR_SNK}$	Full-Scale Current Power Supply Rejection	vs V_{SO} (Note 10)		20		dB
$TFS_{OUT-COLR_SNK}$	Full-Scale Current Temperature Coefficient	(Note 11)		600		ppm/°C
ZS_{COLR_SNK}	Zero-Scale Error	V_{ISNK} = 2V (Note 9)	-8	0	+8	LSB

NOTES:

9. Zero-scale error (ZS) is the deviation from zero current output when the digital input code is zero.
10. Full-scale output current power supply sensitivity (SFS) is measured by varying the V_{SO} from 4.5V to 5.5V DC and measuring the effect of this signal on the full-scale output current.
11. Full-scale output current temperature coefficient (TFS) is given by delta (full-scale output current)/Δ(T).

I_{SNK} Threshold Amplifier DC Specifications Standard condition unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{th_MIN-GAIN}$	Current Gain at Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	8	17	25	mA/mA
$I_{th_MAX-GAIN}$	Current Gain at Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	180	240	295	mA/mA
I_{th_GAIN}	Current Gain	I_{th} = 0µA, 500µA	80	135	170	mA/mA
I_{th_OS}	Current Offset	I_{th} = 0µA	-2	1	3	mA
LIN_{th}	Output Current Linearity	I_{th} = 0µA, 500µA, 1.0mA	-2		4	%
I_{SNK}-th	I_{SNK} Threshold Output Current, Using I_{th} Input	I_{th} = 1.5mA	120			mA
R_{IN}	I_{th} Input Impedance to GND		800		1300	Ω
$PSRR_{th}$	I_{th} Current Power Supply Rejection	I_{th-IN} = 0.45mA, varying V_{SO}		20		dB

I_{SRC} Threshold Amplifier DC Specifications Standard condition unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{th_MIN-GAIN}$	Current Gain At Min Gain	Reg1-21h = 1X, I_{APC} = 0µA, 500µA	9	13	18	mA/mA
$I_{th_MAX-GAIN}$	Current Gain At Max Gain	Reg1-21h = FX, I_{APC} = 0µA, 500µA	150	170	195	mA/mA
I_{th_GAIN}	Current Gain	I_{th} = 0µA, 500µA	80	95	115	mA/mA
I_{th_OS}	Current Offset	I_{th} = 0µA	-2	1	3	mA
LIN_{th}	Output Current Linearity	I_{th} = 0µA, 500µA, 1.0mA	-2		4	%
I_{SRC}-th	I_{SRC} Threshold Output Current, Using I_{th} Input	I_{th} = 1.5mA	120			mA
R_{IN}	I_{th} Input Impedance to GND	Same amplifier as for I_{SNK}	800		1300	Ω
$PSRR_{th}$	I_{th} Current Power Supply Rejection	I_{th-IN} = 0.45mA, varying V_{SO}		20		dB

Threshold DAC (12-bit) DC Specifications Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DNL-T	Threshold DAC Differential Non-Linearity	$P_{th:}$ Reg 0-19 + Reg 1-09	-2		+2	LSB
INL-T	Threshold DAC Integral Non-Linearity	At 900h on Resistive Load. 0V to ~3V		+90		LSB
I_{SRC}-T-DAC	Threshold Output Current, Threshold DAC at Full-Scale, I_{SRC}	P_{th} = 0xFFF, I_{APC} = 0, Reg 1-21 = 8F	110	130	170	mA
I_{SNK}-T-DAC	Threshold Output Current, Threshold DAC at Full-Scale, I_{SNK}	P_{th} = 0xFFF, I_{APC} = 0, Reg 1-21 = 8F	160	200	240	mA
$PSRR_{-FS}$	Power Supply Rejection - Full-Scale Current	Varying the V_{SO} (Note 10)		-42		dB
TC_{-FS-T}	Temperature Coefficient - Full-Scale Current	Not including the R_{SET} tempco (Note 11) 0°C to +85°C		-48		ppm/°C
ZS-R	Zero-Scale Error	V_{IOUT} = 2V (Note 9)	-80	0	80	LSB

HFM (High Frequency Modulator) Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{MAX-ISRC-OFF}$	Max HFM Off DC Output, I_{SRC}	HFMOFF = 0x7FF	90	120	160	mA
$I_{MAX-SNK-OFF}$	Max HFM Off DC Output, I_{SNK}	HFMOFF = 0x7FF	45	62	80	mA
$I_{MIN-SRC-OFF}$	Min HFM Off DC Output, I_{SRC}	HFMOFF = 0x000	-3	0	3	mA
$I_{MIN-SNK-OFF}$	Min HFM Off DC Output, I_{SNK}	HFMOFF = 0x000	-3	0	3	mA
$I_{MAX-SRC-ON}$	Max HFM Oscillator Output, I_{SRC}	HFMON = Reg 0-17h = 0xFF		118		mA_{P-P}
$I_{MAX-SNK-ON}$	Max HFM Oscillator Output, I_{SNK}	HFMON = 0xFF Reg 1-21 = x8h		60		mA_{P-P}
$F_{OSC-MAX}$	Max HFM Frequency	Reg 0-16 = 0xFF; R_{FREQ} = 4.7kΩ	850	980	1150	MHz
$F_{OSC-MIN}$	Min HFM Frequency	Reg 0-16 = 0x01; R_{FREQ} = 4.7kΩ	275	345	400	MHz
$PSRR_{OSC-AMP-ISNK}$	PSRR - HFM Amplitude	700MHz; HFMON = 0xFF		1.2		%/V
$TF_{OSC400MAX}$	HFM Frequency Temperature Coefficient	Range from 200MHz to 400MHz		0 - 900		ppm/°C
$TF_{OSC900MAX}$	HFM Frequency Temperature Coefficient	Range from 400MHz to 900MHz		±250		ppm/°C
VR_{FREQ}	R_{FREQ} Pin Voltage	R_{FREQ} = 4.7kΩ	0.85	1.01	1.1	V
$SS_{-WIDTH-RANGE}$	Spread Spectrum Spreading Width Adjustment Range	R_{FREQ} = 4.7kΩ, Reg 1-18 = 10h, Reg 0-16 = 0x26	0.1	0.293	1.1	%
SS_Shift	Shift of Center Frequency when SS is Enabled vs when it's Disabled	R_{FREQ} = 4.7kΩ, Reg 1-18-00h to 30h, Reg 0-16 = 26h		0.4		%
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 0	30	53	80	kHz
SS_Mod	Spread Spectrum Modulation Frequency	REG 1-18h Bit 7 = 1	15	37	55	kHz

Serial Interface AC Performance Standard conditions unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
F_{SER}	SCLK Operating Range	Static logic not limited at low frequency	0		50	MHz
t_{EH}	SEN "H" Time	At 50MHz	320			ns
t_{EL}	SEN "L" Time	At 50MHz	160			ns
t_{ERSR}	SEN Rising Edge to the First SCLK Rising Edge	At 50MHz	10			ns
t_{CDS}	SDIO Set-Up Time	At 50MHz		10		ns
t_{CDH}	SDIO Hold Time	At 50MHz		10		ns
t_{SREF}	Last SCLK Rising Edge to SEN Falling Edge	At 50MHz	10			ns
t_{CC}	SCLK Cycle Time1	At 50MHz	20			ns
Duty	SCLK "H" Duty Cycle	At 50MHz	40	50	60	%
t_{CDD}	SDIO Output Delay	At 50MHz			4	ns
t_{EDH}	SDIO Output Hold Time	At 50MHz	2			ns

Laser Driver AC Performance

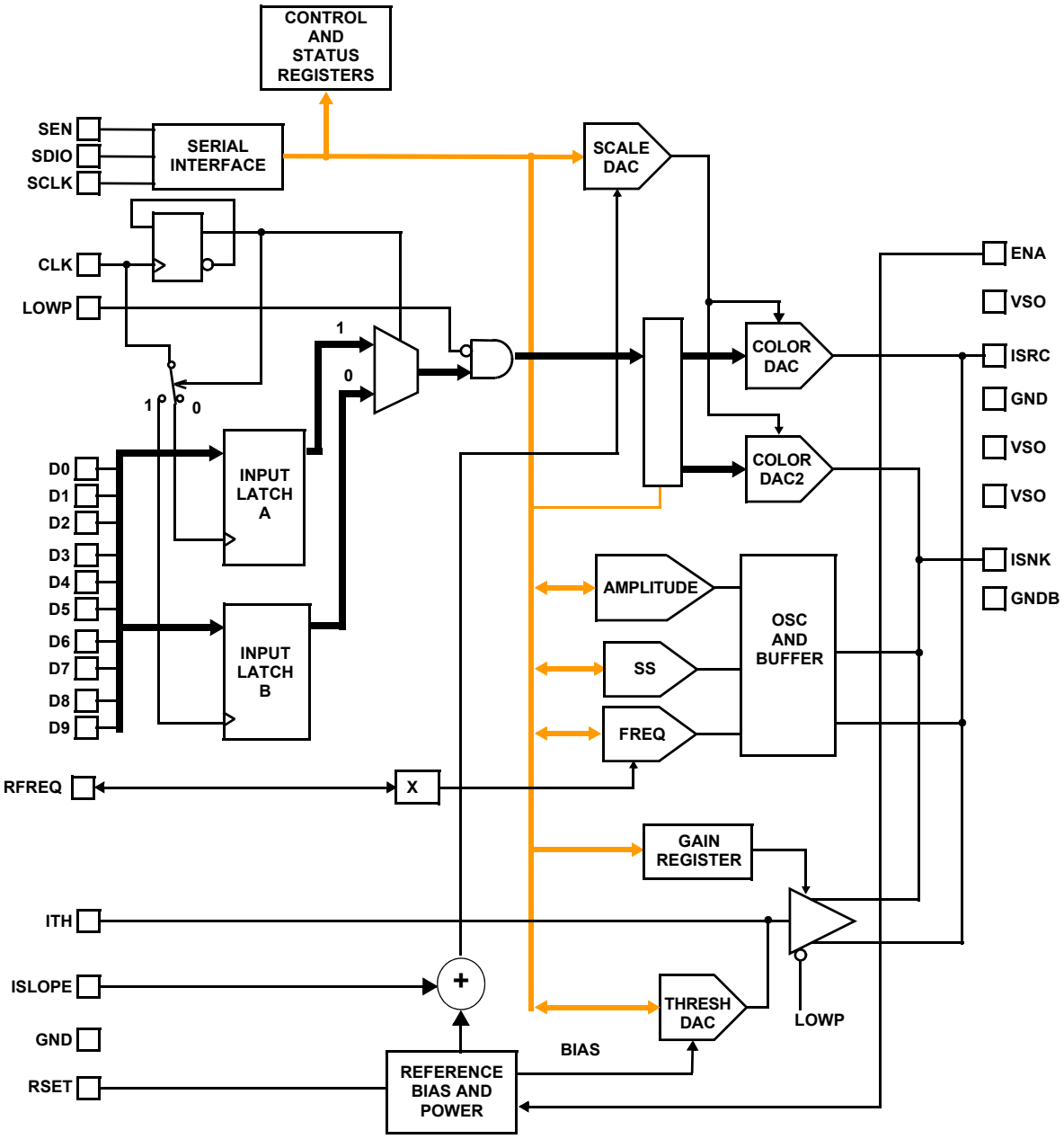
Demoboard test, 10% duty cycle pulse, load = equivalent circuitry to [laser + flex cable] and/or as noted. V_{SO} = 5V. T_A = +25°C.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R\text{-}ISRCx}$	I_{SRC} Write Rise Time (10% to 90%)	Note 12		1.0	2.0	ns
$t_{F\text{-}ISRCx}$	I_{SRC} Write Fall Time (10% to 90%)	Note 12		1.0	2.0	ns
$O/S_{\text{-}ISRCx}$	I_{SRC} Write Fast Overshoot	Note 12		10		%
$t_{R\text{-}ISNK}$	I_{SNK} Write Rise Time (10% to 90%)	Note 12		0.8	1.5	ns
$t_{F\text{-}ISNK}$	I_{SNK} Write Fall Time (10% to 90%)	Note 12		0.5	1.0	ns
t_{DELAY}	From CLK at 50% to OUTPUT at 10%	Note 12		4.5		ns
$t_{OFF\text{-}DELAY}$	From LOWP at 50% to OUTPUT at 10%	Note 12		7		ns
t_{SETUP}	DATA to CLK				700	ps
t_{HOLD}	DATA to CLK				1500	ps
$O/S_{\text{-}ISNK}$	ISNK Write Fast Overshoot	Note 12		10		%
BW_{Ith}	I_{th} Amplifier 3dB Bandwidth	Note 12		0.3		MHz
BW_{ISLOPE}	I_{SLOPE} Amplifier 3dB Bandwidth	Note 12		3		MHz

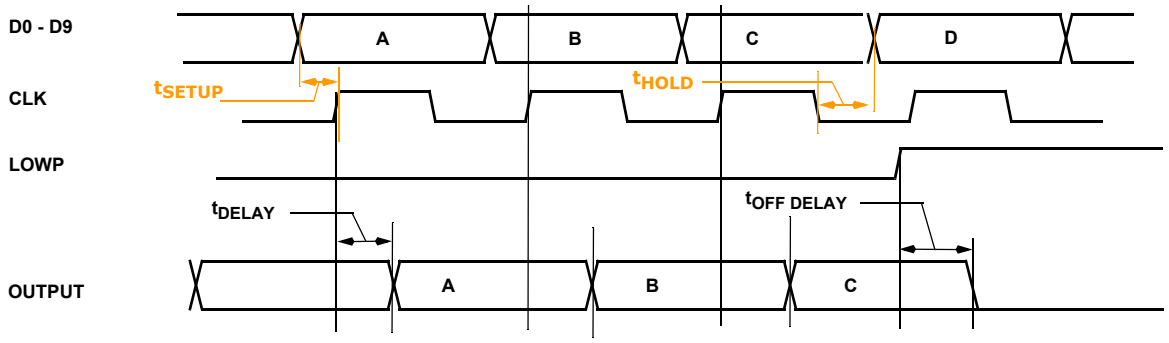
NOTE:

12. Limits established by characterization and are not production tested.

Application Block Diagram



Timing Diagram



Typical Performance Curves

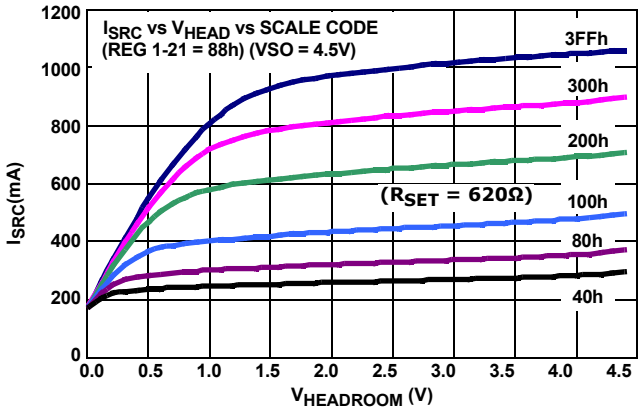


FIGURE 1. I_{SRC} CURRENT vs V_{SD} vs I_{SCALE_BIAS}

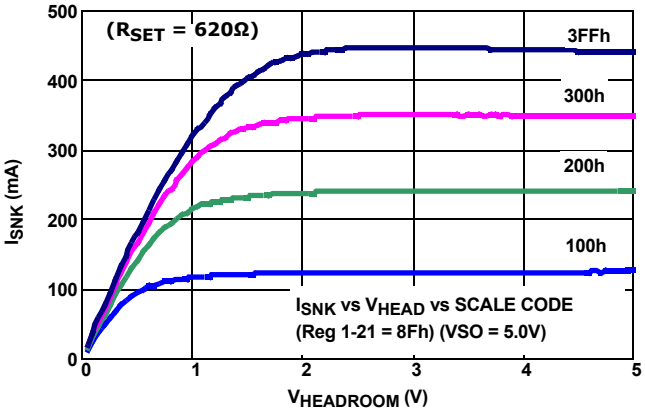


FIGURE 2. I_{SNK} CURRENT vs V_{DS} vs I_{SCALE_BIAS}

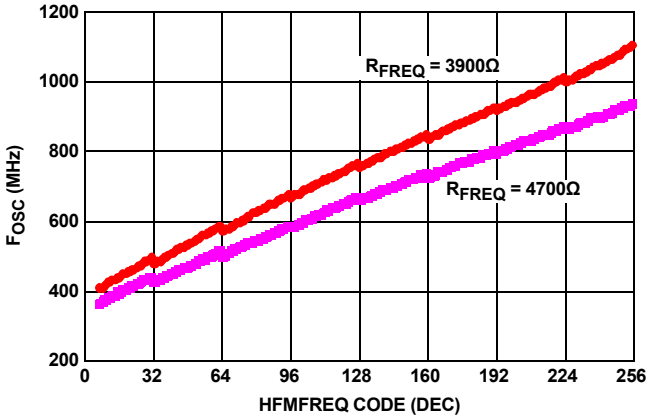


FIGURE 3. HFM CONTROL

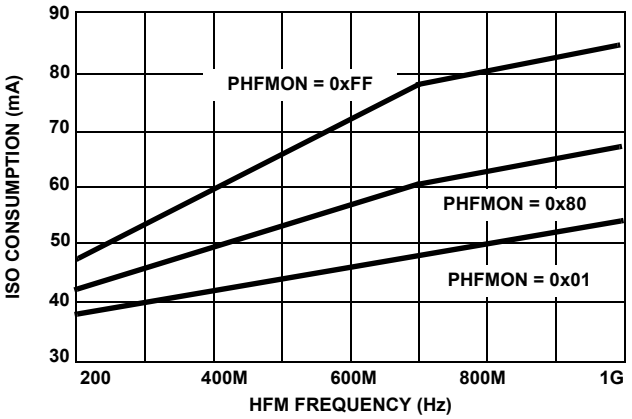


FIGURE 4. HFM OSCILLATOR CURRENT CONSUMPTION

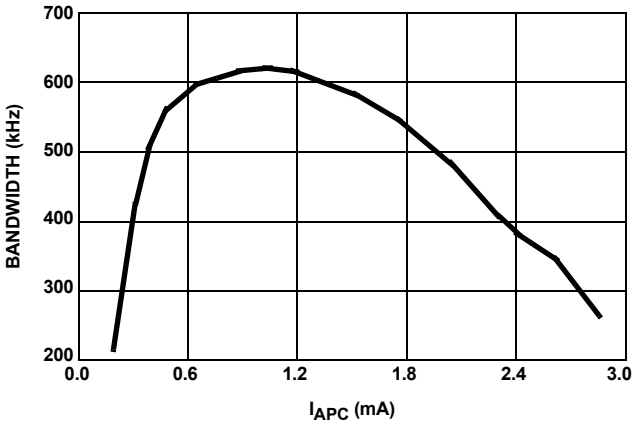


FIGURE 5. I_{OUT}/I_{TH} BANDWIDTH vs I_{TH}

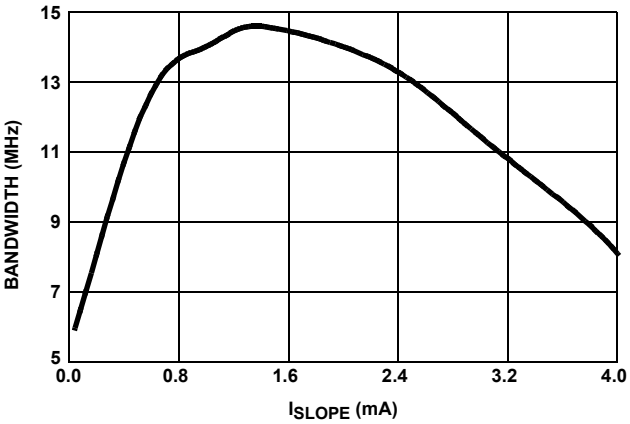


FIGURE 6. I_{OUT}/I_{SLOPE} BANDWIDTH vs I_{SLOPE}

Applications Information

R_{SET} Scaling

The datasheet values for threshold current, and fast current are based on an R_{SET} of 620Ω when scaling DAC and input code are both set to full scale. The user may choose R_{SET} to match the output current needs of the application.

Scaling DAC and I_{SLOPE} Scaling

The scale DAC is biased equivalently by either I_{SLOPE} or I_{RSET} (= V_{RSET}/R_{SET}). That is, 1mA of either bias current results in the same I_{SRC}. In the figures of this section, Scaling DAC output current is used to represent current either into I_{SLOPE} or out of RSET pins.

Color Output Current

The color output current capability for a typical part is shown in Figures 1 and 2. In addition to scaling DAC output, the amount of I_{SRC} will be limited by the available headroom voltage at the ISRC pin.

Color Output Operation

On the rising edge of CLK, the data on the Dn lines is captured. A single data bus can be shared by the three different ISL58214 chips. A separate CLK line is needed for each chip. After the data is loaded in all three colors, the rising edge of LOWP will clock the data from the first flip-flop and into the output flip-flop. Then the output current will be applied to the respective lasers at the same time.

HFM Operation

The HFM oscillator is provided to reduce speckle. The frequency range is determined by RFREQ. The actual frequency is controlled by a register. The HFM includes a spread spectrum function. The frequency of the spread spectrum oscillator and the amplitude of the frequency shift can be programmed.

Threshold Current

Threshold current may be controlled by either the Threshold DAC or the I_{th} input. When set by PTHRESH register (Page 0, Addr 19h, Page 1, Addr 09h), I_{th} is limited to the data sheet value, whereas the I_{TH} input will allow a significantly higher value to be obtained. The threshold DAC and I_{TH} currents sum together producing an input voltage on the net resistance at the ITH pin.

Power Consumption

The primary power consumption is caused by the headroom voltage across the output stage (V_{SO} - V_{ISRC}) x I_{SRC}. In a power sensitive application, the V_{SO} can be reduced below 5.0V (but above VSOgood), so long as sufficient headroom is available to obtain the desired output current. The chip power dissipation depends on the size of the heat sink because the die is attached to a metal plate that is exposed under the package.

Register Usage

Upon power-up all registers are initialized to zero. All registers are read/writable unless otherwise specified.

Bit settings marked as "*Reserved*" or blank must not be used. They may be wired to legacy circuitry.

Memory Map

The address space is organized into three pages with 128 bytes each. Registers CR0, CR1, CR2, and STATUS, can be accessed from any page at the same addresses. The active page is selected via the PAGESEL bits in CR2.

Register List

Control Register 0 . . . . . RegX-00
Control Register 1 . . . . . RegX-01
Control Register 2 . . . . . RegX-02
Status Register RegX-03

Scale DAC High Order Bits Reg0-15
HFM Frequency Setting Reg0-16
HFM Amplitude Setting Reg0-17
Threshold Current High Order Bits Reg0-19
Unlink Control Reg0-21
Control Register 3 . . . . . Reg1-08
Threshold Current Low Order Bits Reg1-09
Slow Damping Reg1-0A
HFM Frequency Counter Reg1-0E
Device ID Reg1-15
Revision ID Reg1-16
Q Damping Reg1-17
Spread Spectrum Control Reg1-18
Threshold & Scale DAC Gain Select Reg1-21
Scale DAC Low Order Bits Reg2-15
I_{OUT} Select Reg2-27

Register Bit Description

TABLE 1. CR0: CONTROL REGISTER 0 (REG X-00)

BIT	NAME	BIT DEFINITION
B7	SELECT I_{SNK}	Use in conjunction with Reg 2-27 Bit 1 If B7 = 0 and Reg 2-27[1] = 0, I_{SRC} is selected. If B7 = 1 and Reg 2-27[1] = 1, I_{SNK} is selected.
B6-B2	Reserved	Leave as 00000
B1	OE	Laser Output Enable 1: Enable laser output stage. 0: Disable laser output stage.
B0	CE	Chip Enable 1: Enable device. 0: Deep sleep, analog portion of the chip is powered down. SDIO still active. The ENA pin is ANDed with CE bit to generate internal Chip Enable.

TABLE 2. CR1: CONTROL REGISTER 1 (REG X-01)

BIT	NAME	BIT DEFINITION
B7	HFMCNTEN	HFM Counter Enable for measuring HFM frequency 1: Enable HFM counter. 0: Disable HFM counter (conserve power).
B6-B4	Reserved	Leave 000
B3	HFMOSCEN	HFM Oscillator Enable 1: Enable. 0: Disable.
B2-B0	Reserved	Leave 000

TABLE 3. CR2: CONTROL REGISTER 2 (Reg X-02)

BIT	NAME	BIT DEFINITION
B7	Reserved	Leave 0
B6	PAGEAUTO	B6 = 0 means that the memory page will not auto toggle. B6 = 1 means that the Memory Page will Auto-toggle between Page0 and Page2.
B5 B4	PAGESEL1 PAGESEL0	Memory Page Select 00: Set accessed page to Page 0 01: Set accessed page to Page 1 10: Set accessed page to Page 2 11: Reserved
B3-B0	Reserved	Leave 0000

TABLE 4. SR1: STATUS REGISTER (REG X-03)

BIT	NAME	BIT DEFINITION
B7, B3	Reserved	
B2	Color Enabled	1 means color current is enabled. 0 means color current is not enabled.
B1	reserved	
B0	PWR OK	1 means that both the 5V and internal 2.5V supplies are above the detection levels. 0 means that one or both supplies are below the detection levels. The detection levels are below the minimum specified.

TABLE 5. SCALE-H: POWER MAX HIGH (REG 0-15)

BIT	NAME	BIT DEFINITION
B7-B0	SCALE-H	SCALE-H - High Order Bits Iw = k(512B7 +256B6 + ... +8B1 +4B0 + Reg 2-15)

TABLE 6. HFMFREQ: HFM FREQUENCY SETTING (REG 0-16)

BIT	NAME	BIT DEFINITION
B7-B0	HFMFREQ	HFMFREQ = F_{MIN} + F_{STEP}(128B7 +64B6 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0) Note: If HFMFREQ = 00h, the HFM output is DC

TABLE 7. HFMON: HFM ON-AMPLITUDE (REG 0-17)

BIT	NAME	BIT DEFINITION
B7-B0	HFMON	HFMON = k(128B7 +64B6 + 32B5 + 16B4 + 8B3 + 4B2 + 2B1 + B0) See "Oscillator Block Diagram" on page 20 for more details on the HFM amplitude.

TABLE 8. THRESHH: THRESHOLD CURRENT HIGH ORDER BITS (REG 0-19)

BIT	NAME	BIT DEFINITION
B7-B0	THRESHH	THRESH = k(2048B7 +1024B6 + ... + 32B1 + 16B0 + THRESHL) THRESHL bits are in Reg 1-0A

TABLE 9. UNLINK: UNLINK CONTROL (REG 0-21)

BIT	NAME	BIT DEFINITION
B7	Unlink	If unlink = 1, the SCALE DAC gets its reference from the ISLOPE pin only. If unlink = 0, the SCALE DAC gets its reference from the RSET pin and the ISLOPE pin.
B6-B0	Reserved	Leave 0000000

TABLE 10. CR3: CONTROL REGISTER 3 (REG 1-08)

BIT	NAME	BIT DEFINITION
B7	REGRST	Resets all registers. 1: Reset. Safety interlock allows reset bit to have effect only when lower three bits of CR0 are cleared (CE = OE = WE = 0). 0: Normal operation.
B6-B0	Reserved	

TABLE 11. THRESHL: THRESHOLD CURRENT LOW ORDER BITS (REG 1-09)

BIT	NAME	BIT DEFINITION
B7-B4	Reserved	Leave 0000
B3-B0	THRESH-L	THRESH-L = k(THRESH-H + 8B3 + 4B2 + 2B1 + B0), THRESH-H is Reg 0-19

TABLE 12. SLOW DAMPING CONTROL (REG 1-0A)

BIT	NAME	BIT DEFINITION
B7-B3	Reserved	Leave 0000
B2-B0	SDAMP1	I_{SRC} Write Waveform Damping

TABLE 13. HFM FREQUENCY COUNT REGISTER (READ MODE) (REG 1-0E)

BIT	NAME	BIT DEFINITION
B7 - B0	HFMCNT	HFM cycles when SEN is high when HFM counting is enabled. B7 is the MSB. The counter will rollover if the count exceeds 255. Reg X-01, bit 7 = 1 enables the HFM counter. Reg 1-0E bit 1 enables the serial HFM counter.

TABLE 14. HFM FREQUENCY COUNT REGISTER (WRITE MODE) (REG 1-0E)

BIT	NAME	BIT DEFINITION
B7 - B2	Reserved	
B1	Enable Serial HFM Count	If B1 = 1, the HFM counter will count when SCLK is high. If B1 = 0, the HFM counter will not count.
B0	SCLK Mode	IF B1 above = 1, and B0 = 0, SCLK is the interval for the HFM frequency count. If B1 above = 1, and B0 = 1, SCLK/2 is the interval for the HFM frequency count (two SCLK periods).

TABLE 15. DEVICE ID (REG 1-15)

BIT	NAME	BIT DEFINITION
B7 - B0	Device ID	Device ID = **0x77** A different number is available for each chip family.

TABLE 16. REVISION ID (REG 1-16)

BIT	NAME	BIT DEFINITION
B7 - B0	Revision ID	This Rev ID is **0xC8** A number to identify the member of the device family.

TABLE 17. WRITE Q DAMPING AND LD SAMPLE (REG 1-17)

BIT	NAME	BIT DEFINITION
B7	LD Sample Ena	B7 = 1 means that laser voltage sampling is enabled. B7 = 0 means that laser voltage sampling is disabled.
B6 - B5	Reserved	Do not use
B4 - B0	QD4 - QD0	Write “Q” Damping for Iout1 is related to (16 QD4 + 8 QD3 + 4 QD2 + 2 QD1 + QD0). A larger number provides more damping.

TABLE 18. SPREAD SPECTRUM CONTROL (REG 1-18)

BIT	NAME	BIT DEFINITION
B7	SS Frequency and Disable	If bits B7, B6, B5, and B4 are all 0, the SS is disabled. If SS width is non zero, this bit selects about 34kHz when 1, and about 53kHz when 0.
B6 - B4	SS Width	Width ≅ k (24B6 + 2 B5 + B4)
B3 - B0	Reserved	Do not use

TABLE 19. THRESHOLD AND SCALE DAC GAIN SELECT (REG 1-21)

BIT	NAME	BIT DEFINITION
B7 - B4	$I_{THRESHOLD}$ GAIN	The Gain of the threshold amplifier is = K(8B7 + 4B6 + 2B5 + B4). The power-up register value is 1000. A setting of 0000 defaults to a setting of 0001 to prevent zero gain.
B3 - B0	I_{SNK_MAX}	If I_{SNK} output is selected, these 4 bits multiply by the existing SCALE output to determine the I_{SNK} fast current. The power-up register value is 1000. A setting of 0000 defaults to a setting of 0001 to prevent zero gain. If I_{SRC} is selected, these bits should be 0000.

TABLE 20. SCALE-L: POWER MAX LOW (REG 2-15)

BIT	NAME	BIT DEFINITION
B7, B6	SCALE-L	Read Only, these are the register bits.
B5, B4	Reserved	Do not use
B3, B2	SCALE-L	SCALE-L - Low Order Bits Iw = k(Reg 0-15 + 2B3 +B2) see SCALE-H in Table 5. When written these bits go the SCALE-L register. When read back, these are the SCALE DAC register bits.
B1, B0	Reserved	Do not use

NOTE: The lower SCALE bits and the high SCALE bits are both written from their register to the SCALE DAC at the same time that the SCALE high bits are written to their register.

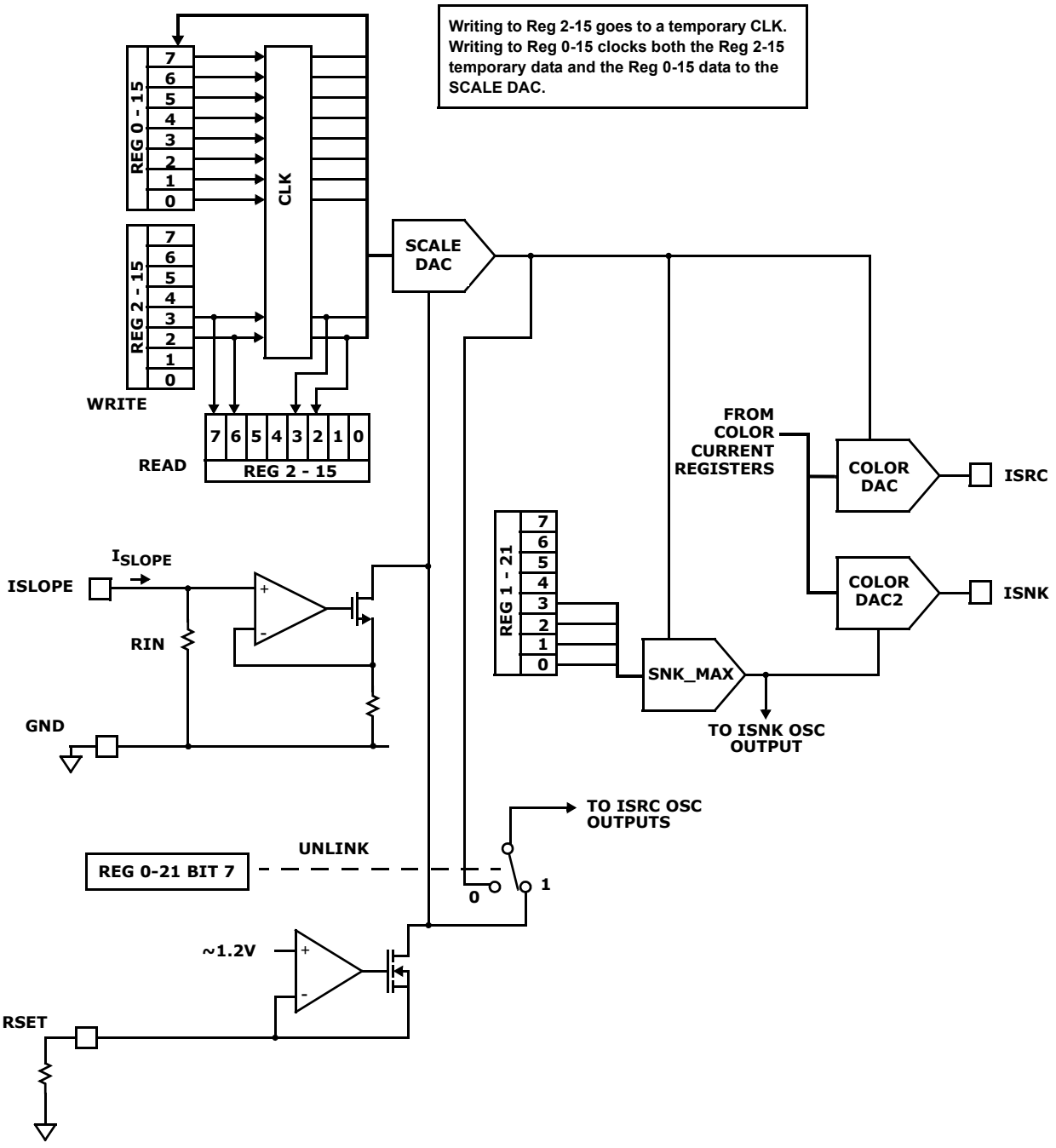
TABLE 21. I_{OUT} SELECT (REG 2-27)

BIT	NAME	BIT DEFINITION
B7 - B2	Reserved	Do not use
B1	Select I_{SNK}	Use in conjunction with Reg X-00 Bit 7 If B0 = 0 and Reg X-00[7] = 0, I_{SRC} is selected. If B1 = 1 and Reg X-00[7] = 1, I_{SNK} is selected.
B0	Reserved	Leave 0

TABLE 22. THRESHOLD CURRENT DAC REPRESENTATION

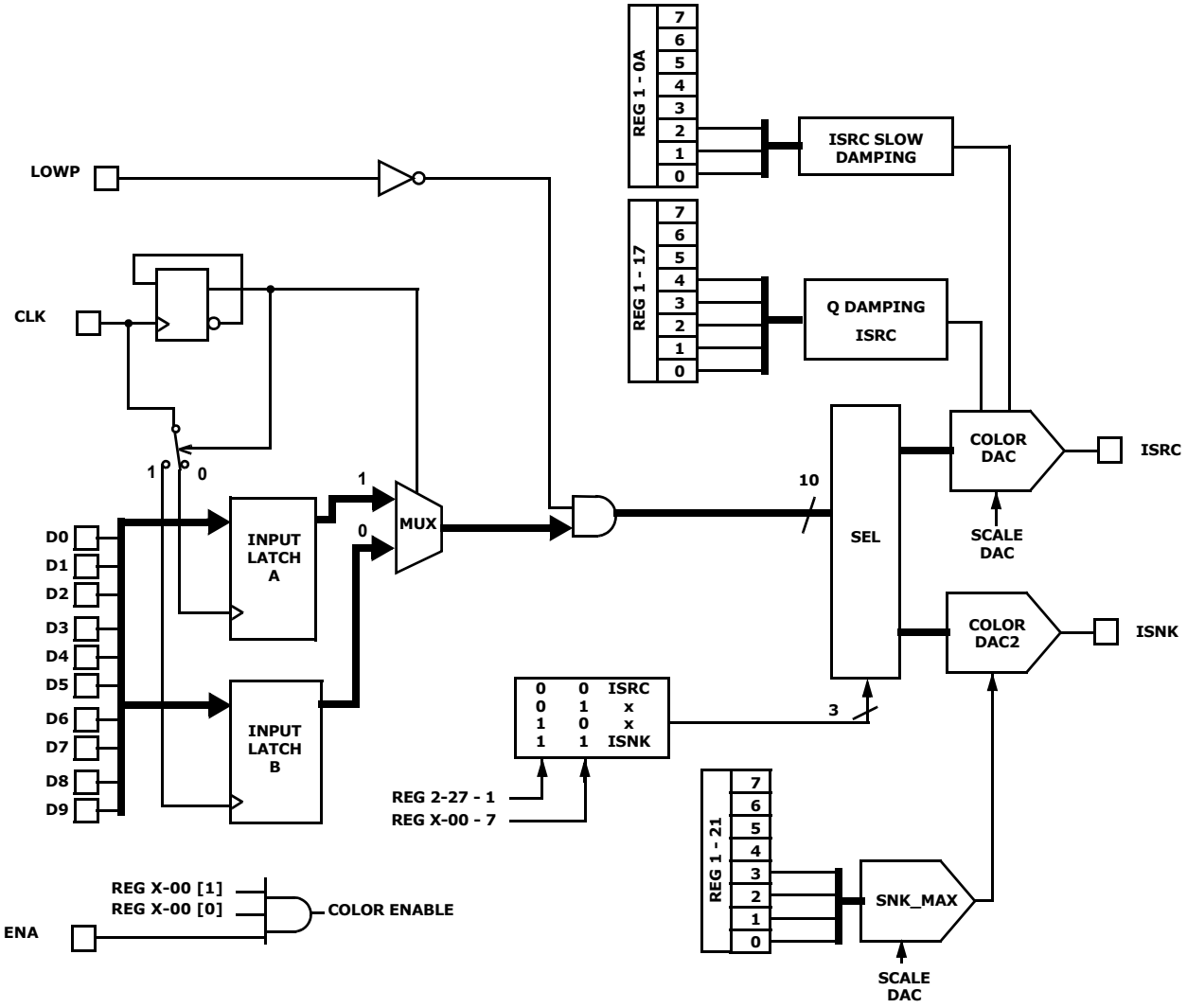
Register bits	THRESHH								THRESHL			
	B7	B6	B5	B4	B3	B2	B1	B0	B3	B2	B1	B0
Representation	Unsigned 12-bit											
	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Scale DAC Block Diagram

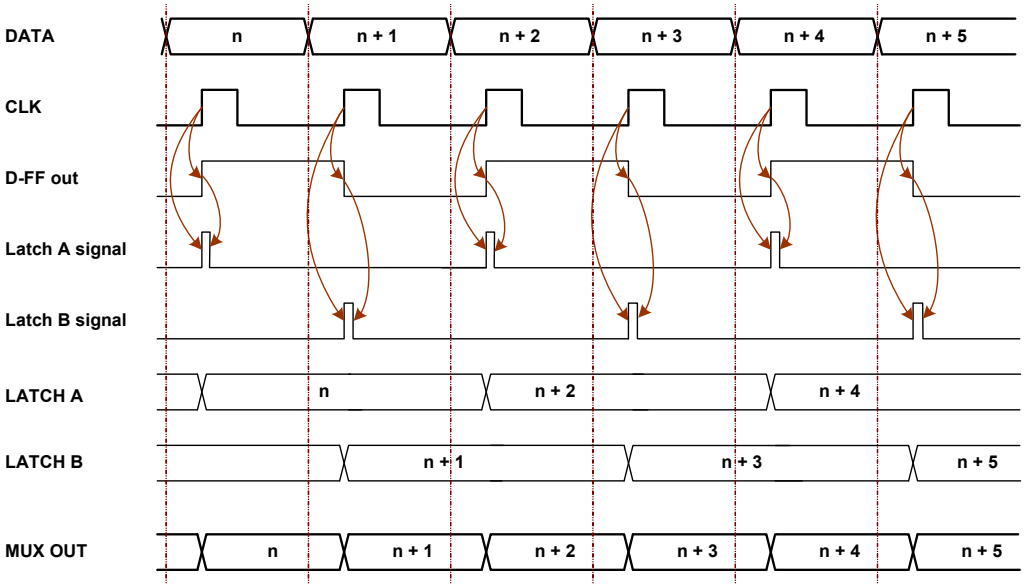


- All of the DAC's are multiplying DAC's, where the output is the product of the input code, and the applied reference signal.

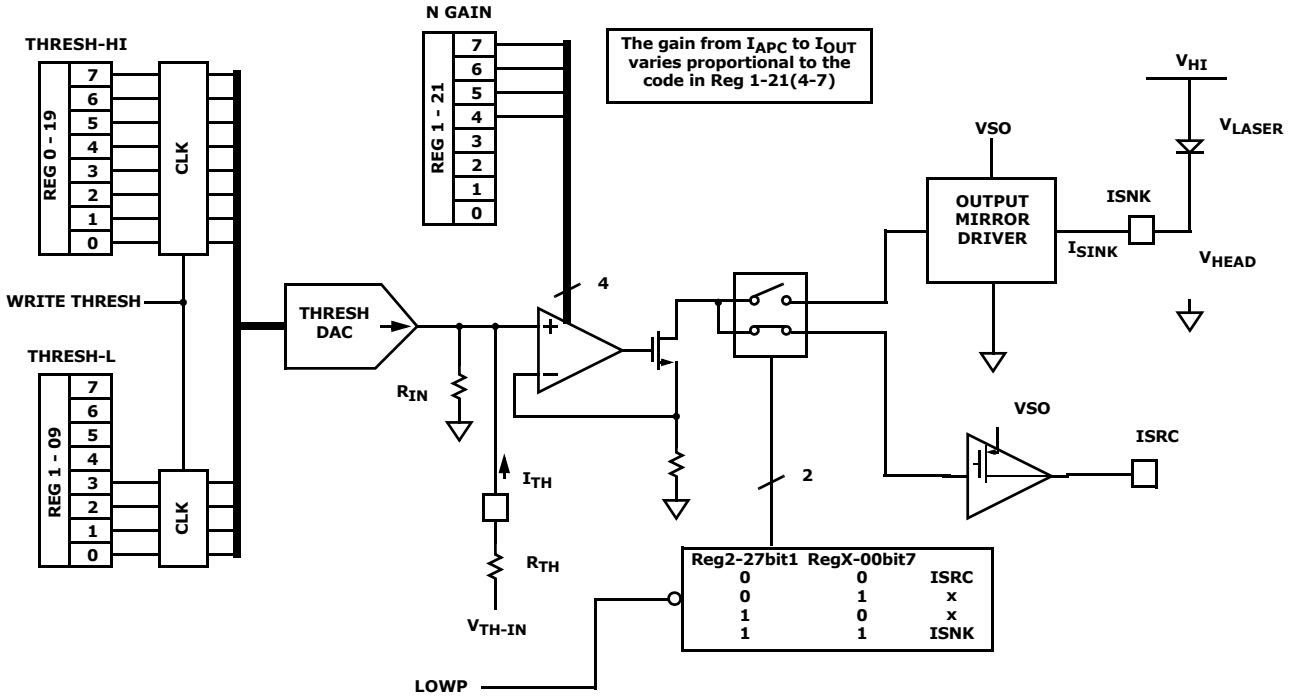
Color Block Diagram



Detailed Timing Diagram



Threshold Block Diagram



Threshold DAC

The THRESH DAC outputs a positive current into the net resistance at the input of the I_{TH} voltage-to-current converter amplifier. The external V_{TH} independently creates a voltage at the input of the I_{APC} amplifier. The net voltage at the input of the I_{APC} amplifier divided by R_{IN} is defined as the APC amplifier input current, even though the current is to ground. This input current multiplied by the specified gain ITH_{GAIN} gives the output current $IOUT_{TH}$. The Threshold amplifier gain varies from 0 to full scale proportional to Reg 1-21-(4-7).

The 12-bit THRESH DAC register is CLKed when THRESH-H is loaded to prevent glitches. It is designed to be a 12-bit monotonic DAC.

When Reg 1-21 = 80h, the gain from I_{APC} to I_{OUT} is about 100mA/mA for any selected output channel.

If LOWP = 1, the threshold current is set to zero.

Threshold Current

The threshold current is approximately determined by interpolation from data specs.

$I_{OUT\text{-}THRESH} = IOUT_{THRESH\text{-}DAC} + IOUT_{THRESH\text{-}Ith}$

Where:

- $IOUT_{THRESH\text{-}DAC}$ ~= IOUT-R-DAC x $THRESH_{MULT}$ x R_{TH} / (R_{TH} + R_{IN})
- $IOUT_{THRESH\text{-}Ith}$ ~= ITH_{GAIN} x $V_{TH\text{-}IN}$ / (R_{TH} + R_{IN})

Where:

IOUT-T-DAC Gives for example: 110mA.

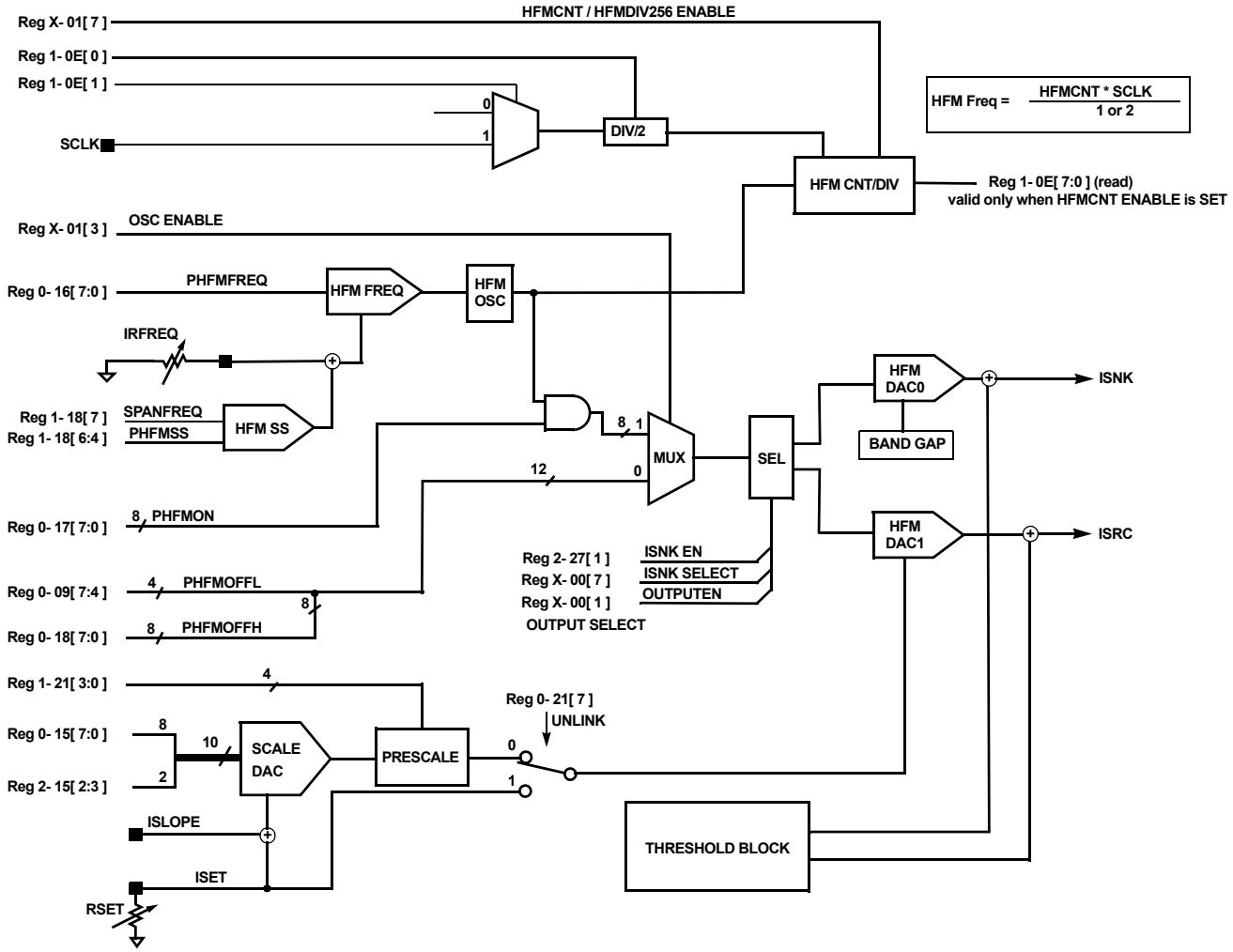
R_{IN} Gives for example: 1000 typ ohms.

ITH_GAIN Gives for example: 100 typ mA/mA.

$THRESH_{MULT}$ ~= $THRESH_{DAC}$/4095, where $THRESH_{DAC}$

The above equations assume a linear transfer function. At high currents there are saturation effects. Below 1V headroom, depending on the current, the predicted output will be less than predicted.

Oscillator Block Diagram



Oscillator Control

A high frequency component can be added to the laser current to reduce speckle.

The HFM block has two states determined by whether the oscillator is enabled or disabled. The HFM block outputs RF modulation when the oscillator is enabled and a DC level when the oscillator is disabled. The DC level is PHFMOFF in HFMOFF mode.

TABLE 23. OSCILLATOR CONTROL LOGIC

X-01-3	OSCILLATOR OUTPUT
0	Off
1	On

HFM I_{OUT} Equations

The oscillator current is approximately determined by interpolation from the datasheet.

$IOUT_{OSC-ON} \cong A_{ON,max}$ x PHFMON/255 x K_{REF} OR Zero.

Where:

- $A_{ON,max}$ = for example: 100mA (typ).
- K_{REF} = ($RSET_{SPEC}$/RSET)
- $RSET_{SPEC}$ = for example 620Ω.

When the HFM oscillator is turned on, the oscillator current reaches a peak value set by PHFMON. The relation between PHFMON and average optical power is difficult to derive deterministically. First, the AC current reaching the laser is attenuated by parasitics. The higher the HFM frequency, the larger the loss. Second, if the laser is biased near threshold, the turn-on delay reduces the optical pulse width. Third, laser relaxation oscillation further shapes the optical pulse.

An empirical procedure is to first find the best conditions for the AC current (PHFMON) and frequency (HFMFREQ) in terms of read noise reduction.

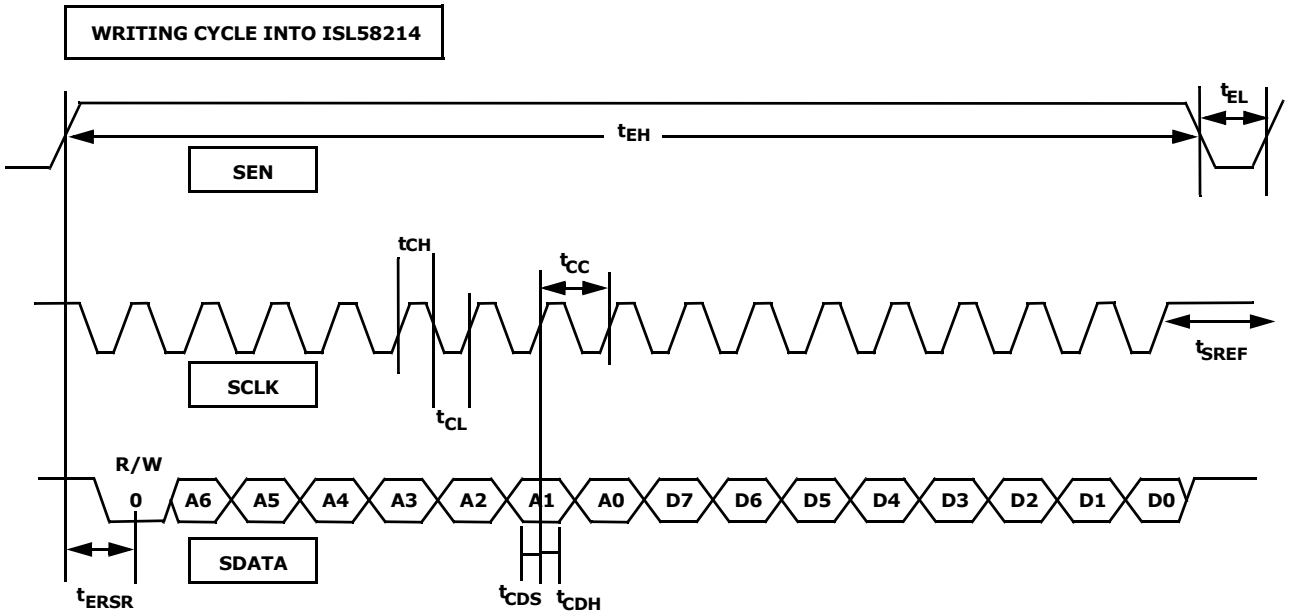
HFM Frequency Counter

HFM frequency can be monitored via internal counter. The way to monitor the HFM frequency is to measure how many cycles occur during a serial clock period. If the serial clock period is known, this enables the HFM to be measured and adjusted by the drive firmware. To enable this measurement, follow the following steps:

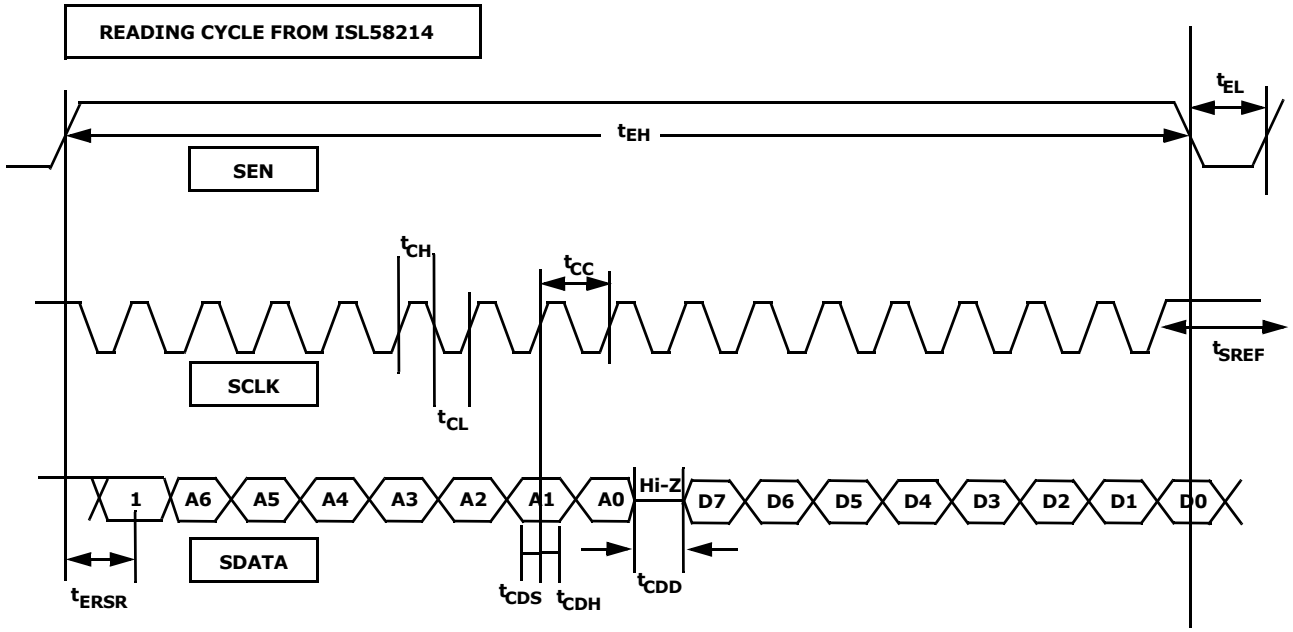
- First clear Reg X-01 Bit 7 = 0. This allows the serial port to use the control register at Reg 1-0E.
- Set Reg 1-0E bit 1 = 1. This enables the serial clock to gate the counter.
- Set Reg1-0E bit 0 = 1. This step is optional, but recommended. This would divide the serial clock by 2, hence increase the number of count of cycles by 2. Since SEN is not synchronized with the HFM, higher number of counts means lower the error.
- Set Reg X-01 bit 7 = 1. This allows the control logic to measure the burst of HFM between serial clock edges. The control logic will continue to do this on any serial transfer, either a write or a read. The measurement is done during the address portion of the serial cycle.
- By reading Reg 1-0E, the measurement is done.
- The HFM frequency then can be calculated as HFM frequency = HFMCNT(dec) x known SCLK/2.

The amount of HFM current that reaches the laser and produces light modulation is a very complex transfer function. Although the HFM circuit simply switches between zero and the specified current, the frequency is so high that the result is heavily influenced by the chip, packages and layout.

Serial Interface Protocol



R/W BIT, ADDRESS BITS, AND DATA BITS ARE CLOCKED INTO ISL58214 AT RISING EDGE OF SCLK.



R/W BIT AND ADDRESS BITS ARE CLOCKED INTO ISL58214 AT RISING EDGE OF SCLK.
DATA BITS ARE CLOCKED OUT FROM ISL58214 AT FALLING EDGE OF SCLK.
THE LAST BIT (D0) OF DATA IS CLOCKED BY THE FALLING EDGE OF SEN.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
April 1, 2015	FN6944.2	Removed Related Literature from page 1. Stamped Datasheet Not Recommended for New Designs No Recommended Replacement.
July 29, 2013	FN6944.1	Converted to New Intersil Template. Changed Products information to About Intersil.
May 13, 2010	FN6944.0	Initial Release

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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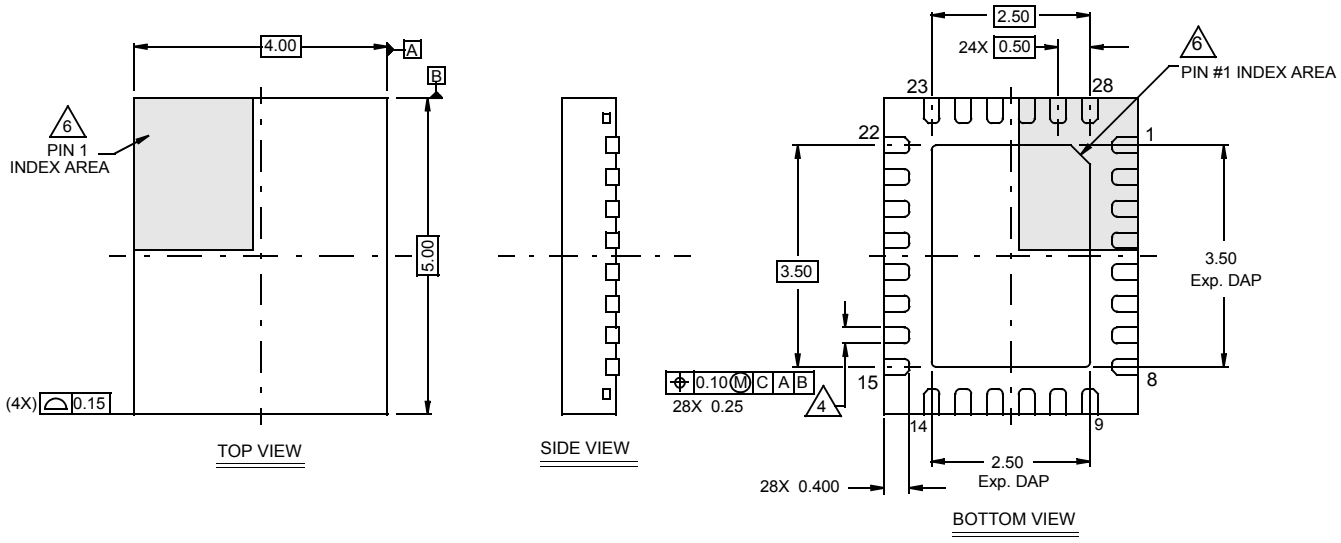
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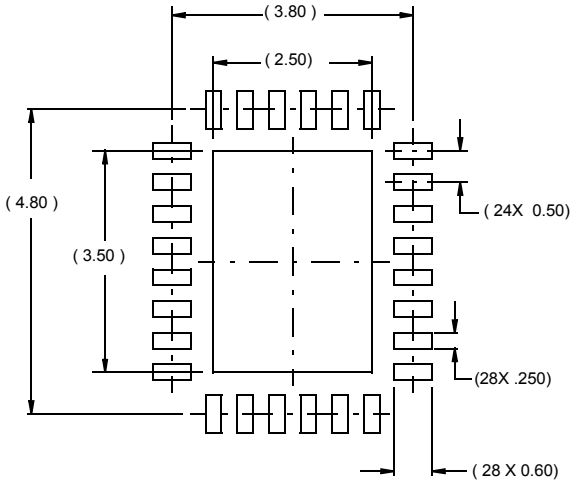
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Package Outline Drawing

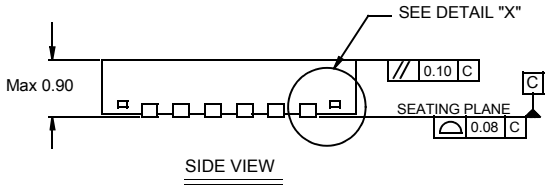
L28.4x5A

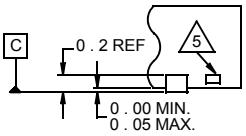
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 06/08





TYPICAL RECOMMENDED LAND PATTERN





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.