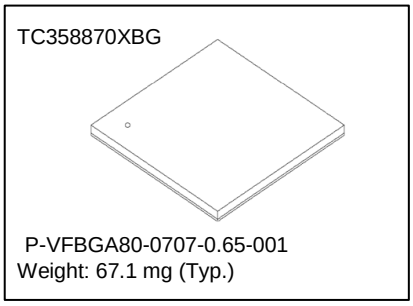
CMOS Digital Integrated Circuit Silicon Monolithic

TC358870XBG

Mobile Peripheral Devices



Overview

TC358870XBG, Ultra HD to DSI, bridge converts high resolution (higher than 4 Gbps) HDMI® stream to MIPI DSI Tx video. It is a follow up device of TC358779XBG, without scalar functionality. The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display by using its HDMI Tx output port.

Features

- **HDMI-RX Interface**
  - ✧ HDMI 1.4b
    - Video Formats Support (Up to 4K×2K / 30fps), maximum 24 bps (bit-per-pixel) no deep color support
      - ➢ RGB, YCbCr444: 24-bpp
      - ➢ YCbCr422: 24-bpp
    - Color Conversion
      - ➢ 4:2:2 to 4:4:4 is supported
      - ➢ 4:4:4: to 4:2:2 is supported
      - ➢ RGB888 to YCbCr (4:4:4 / 4:2:2) is supported
      - ➢ YCbCr (4:4:4 / 4:2:2) to RGB888/666 is supported
        - ✧ Note: for RGB666 (R=R[5:0],2'b00, G=G[5:0],2'b00, B=G[5:0],2'b00)
    - Maximum HDMI clock speed: 297 MHz
    - Audio Supports
      - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
    - 3D Support
    - Support HDCP1.4 decryptions
    - EDID Support, Release A, Revision 1 (Feb 9, 2000)
      - ➢ First 128 byte (EDID 1.3 structure)
      - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
      - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
  - ✧ Does not support Audio Return Path and HDMI Ethernet Channels

- **DSI TX Interface**
  - ✧ MIPI DSI compliant (Version 1.1 22 November 2011)
  - ✧ Dual links DSI (DSI0 and DSI1), each link supports 4 data lanes @1 Gbps/ data lane
    - DSI0 carries the left half data of HDMI Rx video stream and DSI1 carries the right one at the default configuration.
    - Left or right data can be assigned/programmed to either DSI Tx link
    - The maximum length of each half is limited to 2048-pixel plus up to full length overlap, DSI0 data length could be different from that of DSI1's
    - The maximum Hsync skew between DSI0 and DSI1 can be less than 10 ByteClk
  - ✧ Single link DSI, maximum horizontal pixel width
    - 2558 pixels (24-bit per pixel)
    - 3411 pixels (16-bit per pixel)
  - ✧ Supports video data formats
    - RGB666, RGB888, YCbCr444, YCbCr 422 16-bit and YCbCr 422 24-bit
    - YCbCr inputs can be converted into RGB before outputting

- **I^2C Interface**
  - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultrafast mode (2 MHz)
  - ✧ Slave Mode
    - To be used by an external Master to configure all TC358870XBG internal registers, including EDID_SRAM and panel control
    - Support 2 I^2C Slave Addresses (0x0F & 0x1F) selected through boot-strap pin (**INT**)

- **Audio Output Interface**
  - ✧ Up to four I2S data lines for supporting multi-Channel audio data (5.1 and 7.1)
  - ✧ Maximum audio sample frequency supported is 192 kHz @8 CH
  - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
  - ✧ Support Master Clock output only
  - ✧ Support 32 bit-wide time-slot only
  - ✧ Output Audio Over Sampling clock (256fs)
  - ✧ Either I2S or TDM Audio interface available (pins are multiplexed)
  - ✧ I2S Audio Interface
    - Support Left or Right-justify with MSB first
  - ✧ TDM (Time Division Multiplexed) Audio Interface
    - Fixed to 8 channels (depend on HDMI input stream)

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- ✧ Digital Audio Interface
  - Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz

- **InfraRed (IR)**
  - ✧ Support NEC InfraRed protocol.

- **Power supply inputs**
  - ✧ Core: 1.15V
  - ✧ MIPI D-PHY: 1.2V
  - ✧ I/O: 1.8V, 3.3V
  - ✧ HDMI: 3.3V
  - ✧ APLL: 3.3V

- **Power Consumption during typical operations**
  - ✧ 1920×1080 @60 fps: 420 mW (Dual D-PHY link)
  - ✧ 2560×1600 @60 fps: 504 mW (Dual D-PHY link)
  - ✧ 3840×2160 @30 fps: 520 mW (Dual D-PHY link)

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2. MIPI DSI, “MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.1 Revision 22 Nov 2011”
3. HDMI, “High-Definition Multimedia Interface Specification Version 1.4a March 4, 2010”
4. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

TC358870XBG, Ultra HD to DSI, bridge converts high resolution (higher than 4 Gbps) HDMI stream to MIPI DSI Tx video. It is a follow up device of TC358779XBG without scalar/de-interlace capability. The HDMI-RX runs at 297 MHz to carry up to 7.2 Gbps video stream. It requires dual link MIPI DSI Tx, 1 Gbps/data lane, to transmit out a maximum 7.2 Gbps video data.

The bridge chip is necessary for current and next generation Application Processors to drive a (dual) DSI link display directly via its HDMI Tx output port.

TC358870XBG system view block diagrams is shown in Figure 1.1, respectively.

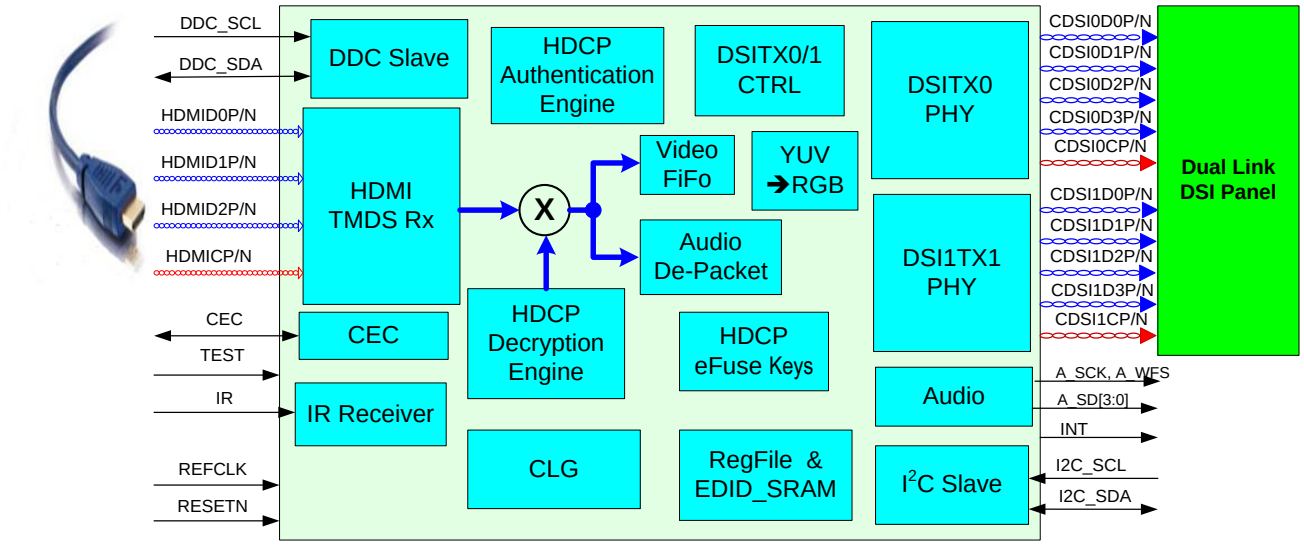


Figure 1.1 TC358870XBG System Overview

2. External Pins

TC358870XBG resides in BGA80 pin packages. The following table gives the signals of TC358870XBG and their function.

Table 2.1 TC358870XBG Functional Signal List

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
SYSTEM (4)	RESETN	K8	I		Sch	System reset input (active low)	VDDIO18
	REFCLK	K9	I		Sch	Reference clock input (40 – 50 MHz)	VDDIO18
	TEST	G5	I		N	Internal test terminal (Always must be fixed low externally)	VDDIO18
	INT	J3	O	L	N	Interrupt Output signal (active high) *1	VDDIO18
CDSI TX0 (10)	CDSI0CP	F10	O	H	MIPI-PHY	MIPI-DSI0 clock positive	VDD12_MIPI0
	CDSI0CN	F9	O	H	MIPI–PHY	MIPI-DSI0 clock negative	VDD12_MIPI0
	CDSI0D0P	H10	O	H	MIPI–PHY	MIPI-DSI0 data 0 positive	VDD12_MIPI0
	CDSI0D0N	H9	O	H	MIPI–PHY	MIPI-DSI0 data 0 negative	VDD12_MIPI0
	CDSI0D1P	G10	O	H	MIPI–PHY	MIPI-DSI0 data 1 positive	VDD12_MIPI0
	CDSI0D1N	G9	O	H	MIPI–PHY	MIPI-DSI0 data 1 negative	VDD12_MIPI0
	CDSI0D2P	E10	O	H	MIPI–PHY	MIPI-DSI0 data 2 positive	VDD12_MIPI0
	CDSI0D2N	E9	O	H	MIPI–PHY	MIPI-DSI0 data 2 negative	VDD12_MIPI0
	CDSI0D3P	D10	O	H	MIPI–PHY	MIPI-DSI0 data 3 positive	VDD12_MIPI0
	CDSI0D3N	D9	O	H	MIPI–PHY	MIPI-DSI0 data 3 negative	VDD12_MIPI0
CDSI TX1 (10)	CDSI1CP	A7	O	H	MIPI-PHY	MIPI-DSI1 clock positive	VDD12_MIPI0
	CDSI1CN	B7	O	H	MIPI–PHY	MIPI-DSI1 clock negative	VDD12_MIPI1
	CDSI1D0P	A9	O	H	MIPI–PHY	MIPI-DSI1 data 0 positive	VDD12_MIPI1
	CDSI1D0N	B9	O	H	MIPI–PHY	MIPI-DSI1 data 0 negative	VDD12_MIPI1
	CDSI1D1P	A8	O	H	MIPI–PHY	MIPI-DSI1 data 1 positive	VDD12_MIPI1
	CDSI1D1N	B8	O	H	MIPI–PHY	MIPI-DSI1 data 1 negative	VDD12_MIPI1
	CDSI1D2P	A6	O	H	MIPI–PHY	MIPI-DSI1 data 2 positive	VDD12_MIPI1
	CDSI1D2N	B6	O	H	MIPI–PHY	MIPI-DSI1 data 2 negative	VDD12_MIPI1
	CDSI1D3P	A5	O	H	MIPI–PHY	MIPI-DSI1 data 3 positive	VDD12_MIPI1
	CDSI1D3N	B5	O	H	MIPI–PHY	MIPI-DSI1 data 3 negative	VDD12_MIPI1
HDMI-RX (9)	HDMICP	C1	I		HDMI-PHY	HDMI clock channel positive	VDD33_HDMI
	HDMICN	C2	I		HDMI-PHY	HDMI clock channel negative	VDD33_HDMI
	HDMID0P	D1	I		HDMI-PHY	HDMI data 0 channel positive	VDD33_HDMI
	HDMID0N	D2	I		HDMI-PHY	HDMI data 0 channel negative	VDD33_HDMI
	HDMID1P	E1	I		HDMI-PHY	HDMI data 1 channel positive	VDD33_HDMI
	HDMID1N	E2	I		HDMI-PHY	HDMI data 1 channel negative	VDD33_HDMI
	HDMID2P	F1	I		HDMI-PHY	HDMI data 2 channel positive	VDD33_HDMI
	HDMID2N	F2	I		HDMI-PHY	HDMI data 2 channel negative	VDD33_HDMI
	REXT	A1	I		HDMI-PHY	External reference resistor (Connect with 2kΩ to VDD33HDMI)	VDD33_HDMI
DDC (2)	DDC_SCL	A3	IO		Sch/5V/OD	DDC I^2C slave clock	VDDIO33
	DDC_SDA	B3	IO		Sch/5V/OD	DDC I^2C slave data	VDDIO33
CEC(1)	CEC	A2	IO		Sch/OD	CEC signal	VDDIO33
HPD(2)	HPDI	A4	I		5V	5V power input	VDDIO33
	HPDO	B4	O	L	N	Hot plug detect output	VDDIO33
Audio (7)	A_SCK	K7	O	L	N	I2S/TDM bit clock signal	VDDIO18
	A_WFS	K5	O	L	N	I2S word clock TDM frame sync signal	VDDIO18
	A_SD3	J5	O	L	N	I2S data signal bit3	VDDIO18
	A_SD2	J6	O	L	N	I2S data signal bit2	VDDIO18
	A_SD1	J8	O	L	N	I2S data signal bit1	VDDIO18
	A_SD0	J9	O	L	N	I2S data signal bit0 TDM data signal	VDDIO18
	A_OSCK	J4	O	L	N	Audio Over Sampling Clock	VDDIO18
IR(1)	IR	G6	I		N	InfraRed signal (Fix low externally, if not used)	VDDIO18
I2C(2)	I2C_SCL	K4	IO		Sch/OD	I^2C slave clock	VDDIO18
	I2C_SDA	K3	IO		Sch/OD	I^2C slave data	VDDIO18
Audio PLL	BIASDA	J1	O	L	PLL	Audio PLL BIAS signal	VDDIO33

Group	Pin Name	Ball	I/O	Init (O)	Type (Note)	Function	Voltage Supply
(4)						Connect to AVSS through 0.1 μF when not used	
	DAOUT	J2	O	L	PLL	Audio PLL Clock Reference output clock Please leave open when not used	VDDIO33
	PCKIN	K1	I		PLL	Audio PLL Reference Input clock Connect to AVSS through 0.1 μF when not used	VDDIO33
	PFIL	K2	O	L	PLL	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1 μF when not used	VDDIO33
POWER (10)	VDDC11	C10 K6	-		Power	1.1V Internal core power supply	-
	VDDIO18	J7	-		Power	1.8V IO power supply	-
	VDDIO33	H2	-		Power	3.3V IO power supply	-
	VDD33_HDMI	B1 G1	-		Power	HDMI Phy 3.3Vpower supply	-
	VDD11_HDMI	B2 G2	-		Power	HDMI Phy 1.1V power supply	-
	VDD12_MIPI0	J10	-		Power	MIPI DSI 1.2V power supply for link0	-
	VDD12_MIPI1	B10	-		Power	MIPI DSI 1.2V power supply for link1	-
GROUND (18)	VSS	A10 C9 D4 D5 D6 D7 E4 E5 E6 E7 F4 F5 F6 F7 G4 G7 H1 K10	-		-	Ground	-

Total 80 pins

Note: Descriptions mean below.

N: Normal digital I/O

Sch: Schmitt trigger input

5V: 5V tolerant input

OD: Open drain

*1: Pull-Up to select 0x1F for I^2C Slave address

Pull-Down to select 0x0F for I^2C Slave address

Please consult a technical support representative before board design to determine whether pull-up or pull-down with external resistors.

2.1. TC358870XBG 80-Pin Count Summary

Table 2.2 BGA80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	-
CDSI TX0	10	-
CDSI TX1	10	-
HDMI-RX	9	-
DDC	2	-
CEC	1	-
Audio	7	-
I2C	2	-
IR	1	-
HPD	2	-
Audio PLL	4	-
POWER	10	IO, Core
GROUND	18	IO, Core, Analog
TOTAL Pin Count	**80**	Func 52 + (10+18)

2.2. Pin Layout

P-VFBGA80-0707-0.65 — Top view

	1	2	3	4	5	6	7	8	9	10
A	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	REXT	CEC	DDC_SCL	HPDI	CDSI1D3P	CDSI1D2P	CDSI1CP	CDSI1D1P	CDSI1D0P	VSS
B	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
	VDD33_HDMI	VDD11_HDMI	DDC_SDA	HPDO	CDSI1D3N	CDSI1D2N	CDSI1CN	CDSI1D1N	CDSI1D0N	VDD12_MIPI1
C	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
	HDMICP	HDMICN	No ball	No ball	No ball	No ball	No ball	No ball	VSS	VDDC11
D	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
	HDMID0P	HDMID0N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0D3N	CDSI0D3P
E	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
	HDMID1P	HDMID1N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0D2N	CDSI0D2P
F	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
	HDMID2P	HDMID2N	No ball	VSS	VSS	VSS	VSS	No ball	CDSI0CN	CDSI0CP
G	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
	VDD33_HDMI	VDD11_HDMI	No ball	VSS	TEST	IR	VSS	No ball	CDSI0D1N	CDSI0D1P
H	H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
	VSS	VDDIO33	No ball	No ball	No ball	No ball	No ball	No ball	CDSI0D0N	CDSI0D0P
J	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
	BIASDA	DAOUT	INT	A_OSCK	A_SD3	A_SD2	VDDIO18	A_SD1	A_SD0	VDD12_MIPI0
K	K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
	PCKIN	PFIL	I2C_SDA	I2C_SCL	A_WFS	VDDC11	A_SCK	RESETN	REFCLK	VSS

HDMI RX: A1, A2, B1, B2, C1, C2, D1, D2, E1, E2, F1, F2, G1, G2

APLL: J1, J2, K1, K2

CDSI1: A5, A6, A7, A8, A9, A10, B5, B6, B7, B8, B9, B10

CDSI0: D9, D10, E9, E10, F9, F10, G9, G10, H9, H10, J9, J10

Figure 2.1 TC358870XBG 80-Pin Layout (Top View)

3. Major Functional Blocks

TC358870XBG consists of the following major blocks: HDMI-RX, DSI Tx, EDID, DDC Slave, CEC, Audio, INT and I^2C Slave I/F.

DDC Slave, CEC and I^2C slave controller are always enabled which is required for configure the TC358870XBG chip and to wake up TC358870XBG chip.

The following sections describe each block in detail. Addition, there is a section describes Clock generation block.

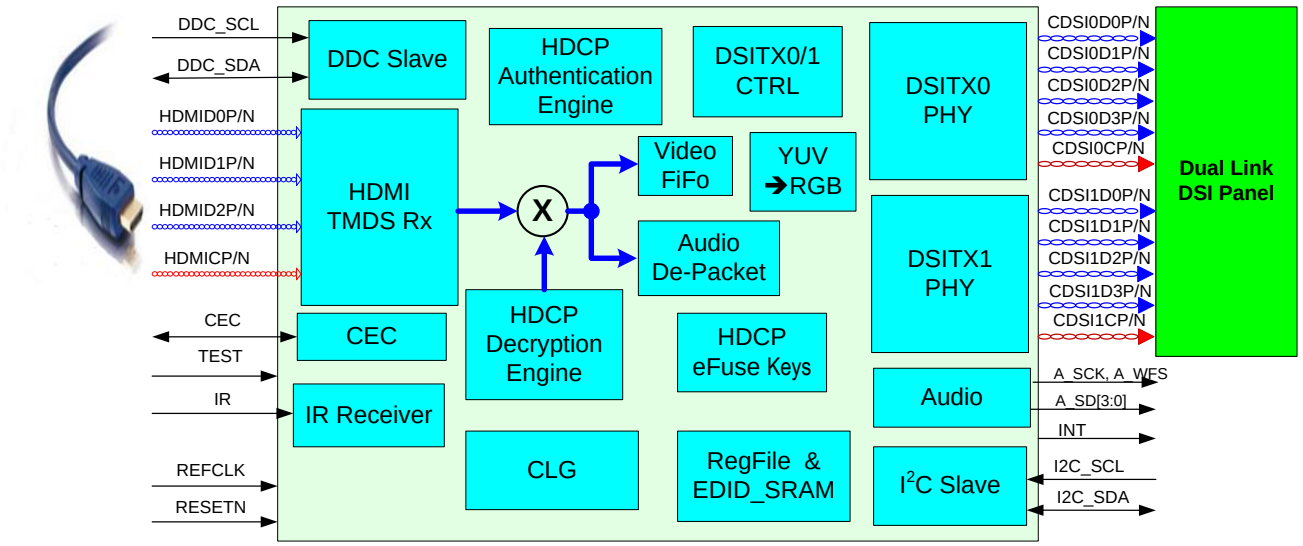


Figure 3.1 Block Diagram of TC358870XBG

3.1. HDMI-RX

Primary features

- HDMI 1.4, maximum pixel clock frequency: 297 MHz
- Video Format support
  - RGB, YCbCr444: 24-bpp
  - YCbCr422: 24-bpp
- Audio Support
- 3D Video Support

3.1.1. **3D Support**

HDMI 3D feature supports the following 3D structures.

Table 3.1 HDMI 3D Structure

3D_structureValue	Meaning
0000	Frame packing
0110	Top-and-Bottom
1000	Side-by-Side (Half)
0011	Side-by-Side (Full)

3.1.2. **InfoFrame Data**

In HDMI streams, there are InfoFrame data. TC358870XBG stores these data internally in its registers, ***0x8710 to 0x87EF***.

- When detected there are a change in the InfoFrame data, it asserts the **INT** so that the external micro-controller can get the InfoFrame data by reading the registers.

Below is the order that InfoFrame data showed the register offset.

Table 3.2 InfoFrame Data Registers Summary

Register Address Offset	Register name	Description
0x8710	AVI_0HEAD	861B AVI_info packet – Header byte 0 (= type)
0x8711	AVI_1HEAD	861B AVI_info packet – Header byte 1 (= version)
0x8712	AVI_2HEAD	861B AVI_info packet – Header byte 2 (= data length)
0x8713	AVI_0BYTE	861B AVI_info packet – Data byte 0 (= checksum)
0x8722 - 0x8714	AVI_xHEAD	861B AVI_info packet – Data byte 15 -1
0x872F - 0x8723	Reserved	Reserved
0x8730	AUD_0HEAD	861B AUD_info packet – Header byte 0 (= type)
0x8731	AUD_1HEAD	861B AUD_info packet – Header byte 1 (= version)
0x8732	AUD_2HEAD	861B AUD_info packet – Header byte 2 (= data length)
0x8733	AUD_0BYTE	861B AUD_info packet – Data byte 0 (= checksum)
0x873D - 0x8734	AUD_xBYTE	861B AUD_info packet – Data byte 10 – 1
0x873F - 0x873E	Reserved	Reserved
0x8740	MS_0HEAD	861B MS_info packet – Header byte 0 (= type)
0x8741	MS_1HEAD	861B MS_info packet – Header byte 1 (= version)
0x8742	MS_2HEAD	861B MS_info packet - Header byte 2 (= data length)
0x8743	MS_0BYTE	861B MS_info packet – Data byte 0 (= checksum)
0x874D - 0x8744	MS_xBYTE	861B MS_info packet – Data byte 10 – 1
0x874F - 0x874E	Reserved	Reserved
0x8750	SPD_0HEAD	861B SPD_info packet – Header byte 0 (= type)
0x8751	SPD_1HEAD	861B SPD_info packet – Header byte 1 (= version)
0x8752	SPD_2HEAD	861B SPD_info packet – Header byte 2 (= data length)
0x8753	SPD_0BYTE	861B SPD_info packet – Data byte 0 (= check sum)
0x876E - 0x8754	SPD_xBYTE	861B SPD_info packet – Data byte x
0x876F	Reserved	Reserved
0x8770	VS_0HEAD	861B VS_info packet – Header byte 0 (= byte)
0x8771	VS_1HEAD	861B VS_info packet – Header byte 1 (= version)
0x8772	VS_2HEAD	861B VS_info packet – Header byte 2 (= data length)
0x8773	VS_0BYTE	861B VS_info packet – Data byte 0 (= checksum)
0x878E - 0x8774	VS_xBYTE	861B VS_info packet – Data byte x
0x878F	Reserved	Reserved
0x8790	ACP_0HEAD	ACP packet – Header byte 0 (= type)
0x8791	ACP_1HEAD	ACP packet – Header byte 1
0x8792	ACP_2HEAD	ACP packet – Header byte 2
0x8793	ACP_0BYTE	ACP packet – Data byte 0
0x87AE - 0x8794	ACP_xBYTE	ACP packet – Data byte x
0x87AF	Reserved	Reserved
0x87B0	ISRC1_0HEAD	ISRC1 packet – Header byte 0
0x87B1	ISRC1_1HEAD	ISRC1 packet – Header byte 1
0x87B2	ISRC1_2HEAD	ISRC1 packet – Header byte 2
0x87C2 - 0x87B3	ISRC1_xBYTE	ISRC1 packet – Data byte x
0x87CF - 0x87C3	Reserved	Reserved
0x87D0	ISRC2_0HEAD	ISRC2 packet – Header byte 0
0x87D1	ISRC2_1HEAD	ISRC2 packet – Header byte 1
0x87D2	ISRC2_2HEAD	ISRC2 packet – Header byte 2
0x87EE - 0x87D3	ISRC2_xBYTE	ISRC2 packet – Data byte x
0x87EF	Reserved	Reserved

AVI: Auxiliary Video Information InfoFrame, InfoFrame_type = 0x02, HDMI Packet Type = 0x82

AUD: Audio InfoFrame, InfoFrame_type = 0x04, HDMI Packet Type = 0x84

MS: MPEG Source InfoFrame, InfoFrame_type = 0x05, HDMI Packet Type = 0x85

SPD: Source Product Description InfoFrame, InfoFrame_type = 0x03, HDMI Packet Type = 0x83

VS: Vendor Specific InfoFrame, InfoFrame_type = 0x01, HDMI Packet Type = 0x81

ACP: Audio Content Protection Packet, HDMI Packet Type = 0x4

ISRC1: International Standard Recoding Code, HDMI Packet Type = 0x5

ISRC2: International Standard Recoding Code, HDMI Packet Type = 0x6

3.2. Line Split

We need dual link DSI Tx to transmit out HDMI Rx received 7.2 Gbps (297 MHz x 24bpp) video stream. The splitting of one (line of) video stream is performed by left and right halves. Left half data is sent to DSI0 link, while the right one is routed to DSI1 link.

1. Left half data can be assigned/programmed to either DSITx port
2. Left half data length could be different from that of right half one.
3. The maximum Hsync skew between DSI0 and DSI1 is less than 10 MIPI link ByteClk
4. The maximum length of each half is limited to 2048+32-pixel at 24bpp due to the 4 Gbps D-PHY link speed per lane
5. The splitting for DSI Tx is shown graphically in Figure 3.2.
6. Please note there is 1-line time delay between HDMI Rx and MIPI-Tx output due to the 2-line buffer implementation in DSI Tx block
7. For dual DSI link splitting, overlapped splitting shown in Figure 3.3 is also supported.

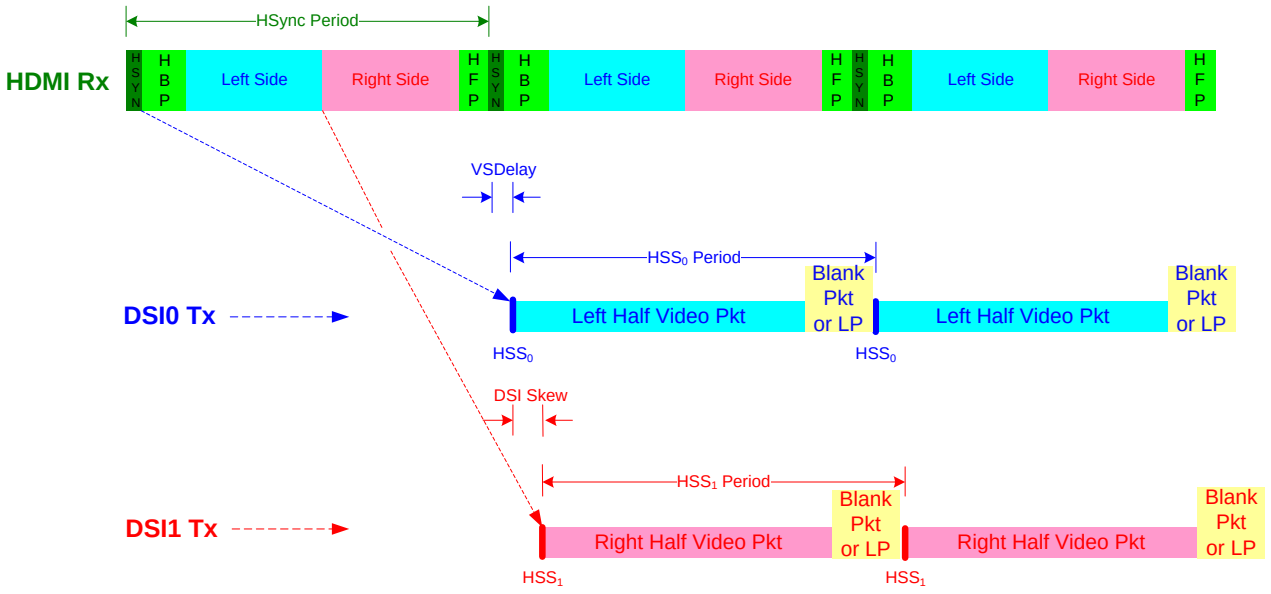


Figure 3.2 Line Splitting for Dual DSI Link

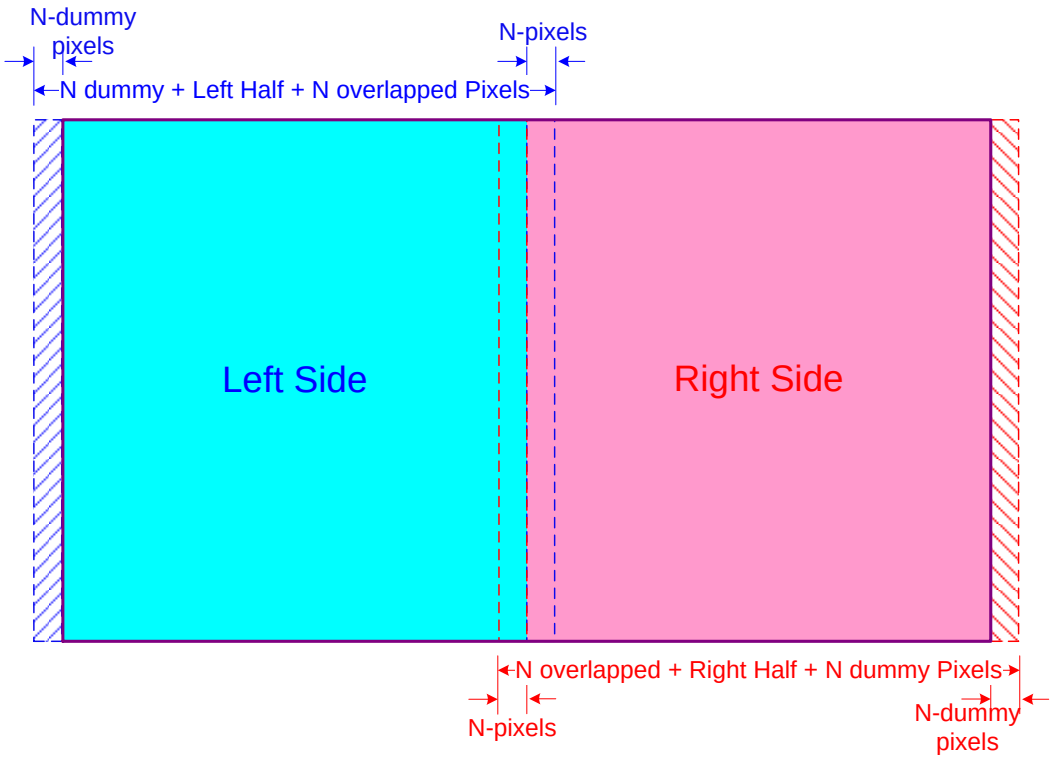


Figure 3.3 Line Overlap Splitting in Dual DSI Link

Please consult a technical support representative on a specific custom way of line splitting.

3.3. DSI Tx Controller

3.3.1. DSI TX Application

TC358870XBG can convert HDMI streams to DSI streams in order to display it directly on the DSI panel.

3.3.1.1. Program/Initialize DSI Panel

DSI panel might need to be programmed/initialized via DSI link.

1. TC358870XBG provides several ***DCSCMD_**** registers, which can be used to issue DSI command in order to program DSI panel. Please refer to section 3.3.2 for details.
2. These ***DCSCMD_**** registers can be written by an external micro-controller.
3. TC358870XBG uses DSI0 to program panel.
   (a) TC358870XBG can also use DSI1 to program panel with two LCD controllers
   (b) Simultaneously sending command to both DSI links are also supported to prevent left-right panel skew.

3.3.2. DSI TX Command Packet Operation

Below is the description of TC358870XBG sequence for transmitting out DSI, including DCS, Command over DSI TX. Host can use I^2C interface to access TC358870XBG registers.

By programming the following register, TC358870XBG will generate/transmit DSI command packets. ECC and CRC are generated and attached automatically by the hardware.

- ***DCSCMD_Q (0x0504)***
  - ✧ DSI command queue

There is a 16-bit wide by 32 deep command queue FIFO for DSI command packets in the design.

When the last byte(s) of a packet is programmed, hardware will send out a packet with the content from the DSI command queue FIFO either at the beginning of vertical front porch or the beginning of vertical back porch selected by the ***CMD_SEL (0x0500) [dcs_cm_act]*** register bit. Once the packet is sent out, hardware increments the ***DCSCMD_ST (0x0502) [dcs_cmd_done]*** status bits by 1.

Host can write another packet to the ***DCSCMD_Q*** register as long as the command queue FIFO is not full. Command queue FIFO status can be monitored in the ***DCSCMD_ST (0x0502)*** register. If there are multiple DSI command packets in the command queue FIFO, multiple DSI command packets will be sent out during either vertical front or back porch during video transmission.

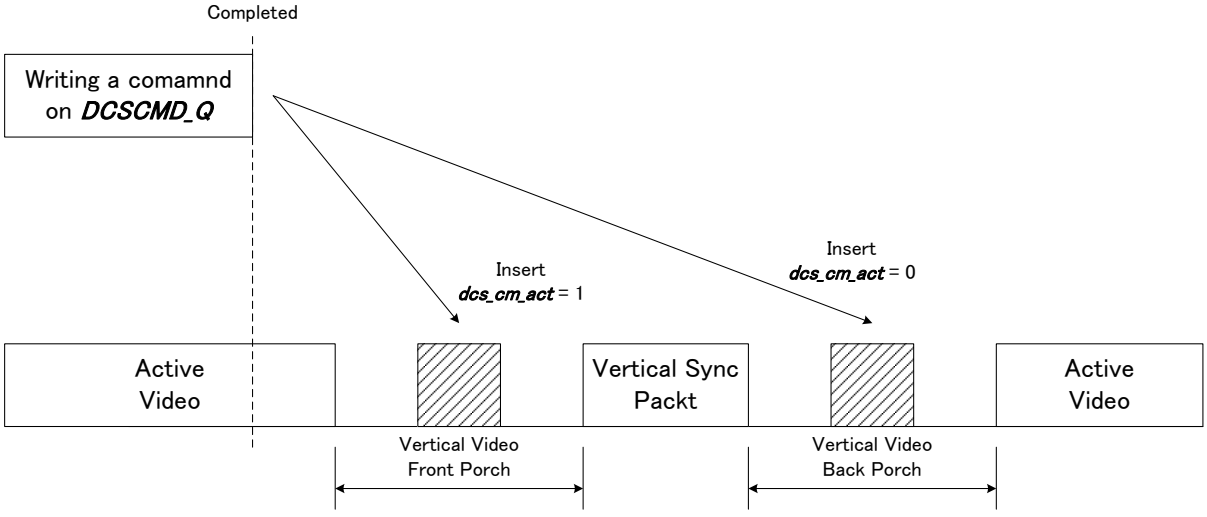


Figure 3.4 DSI Command Transmission Timing

3.3.3. TX Short Packet (DCS) Write Command

The relationship/assembly of a short DSI packet with respect to the ***DCSCMD_Q (0x0504)*** register are illustrated in Figure 3.5. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 contains either command parameter or "0x00".

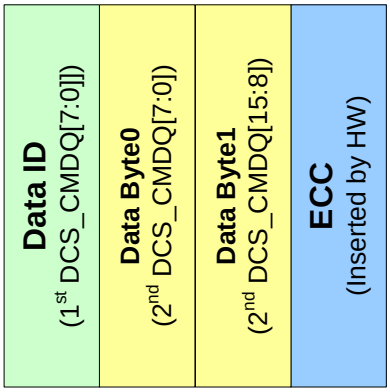


Figure 3.5 DSI Short Command Packet Assembly

The step-by-step procedure is listed below with two examples:

1. Choose desired DCS Short Write Command in register 1st ***DCSCMD_Q[7:0]*** = 0x05 or 0x15 for DCS Command without parameter or with 1 parameter, respectively.
   Note that 1st ***DCSCMD_Q[15]*** is used to indicate if the packet is a short packet or long packet: 0 means short packet and 1 means long packet
   1st ***DCSCMD_Q[14:8]*** is reserved and should be set to 0.

   Write 0x00_05 to ***DCSCMD_Q[15:0]*** for DCS Short Write Command with 0 parameter packet – note bit 15 must be set to 0 for short packet
   or
   Write 0x00_15 to ***DCSCMD_Q[15:0]*** for DCS Short Write Command with 1 parameter packet – note bit 15 must be set to 0 for short packet

2. If 1st ***DCSCMD_Q[7:0]*** = 0x15, set DCS Command Parameter in 2nd ***DCSCMD_Q***[15:8]. Otherwise set "0x00" in 2nd ***DCSCMD_Q[15:8]***. Set 2nd ***DCSCMD_Q[7:0]*** to the DCS command.

   Write {0x00, dcs_command[7:0]} to ***DCSCMD_Q[15:0]*** for DCS Command with 0 parameter
   or
   Write {parameter[7:0], dcs_command[7:0]} to ***DCSCMD_Q[15:0]*** for DCS Command with 1 parameter

3. Check ***DCSCMD_ST (0x0502)*** register for command queue FIFO status:
   - ***[dcs_cm_entry]*** indicates how many FIFO entries are still available for writing to.
   - ***[dcs_cmd_done]*** is incremented by 1 when the DSI packet has been sent out on MIPI interface.
     Note that ***[dcs_cmd_done]*** will wrap around to 0 when it is 3.
   - ***[dcs_cmd_oflow]*** indciates command queue FIFO has overflowed
     Write 1 to ***[dcs_cmd_oflow]*** to clear this bit.
   - ***[dcs_cmd_empty]*** indicates command queue FIFO is empty.
   - ***[dcs_cmd_full]*** indicates command queue FIFO is full.

Example1: TX DCS Short Command: Exit_Sleep_Mode (0x11), no parameter

DCSCMD_Q (0x0504) = 0x0005	(Short packet, Data ID = 0x05)
DCSCMD_Q (0x0504) = 0x0011	(WC1=0x00, WC0=0x11 for DSC Command)

Example2: TX DCS Short Command: Set_Pixel_Format (0x3A), 1 parameter (RGB888)

DCSCMD_Q (0x0504) = 0x0015 (Short packet, Data ID = 0x15)
DCSCMD_Q (0x0504) = 0x703A (WC1=0x70 for RGB888, WC0=0x3A for DSC Command)

3.3.4. TX Long Packet Write Command (limited to 512-byte in length)

The relationship/assembly of a long DSI packet with respect to the ***DCSCMD_**** registers are illustrated in Figure 3.6. The command code, either DCS command or Panel specific command, is stored in Data Byte 0 while Data Byte1 to Data Byte 511 contains either command parameters. The maximum word count for DSI Long Command is limited to 512 bytes. For a single byte command code, the maximum parameters length can be 511 bytes.

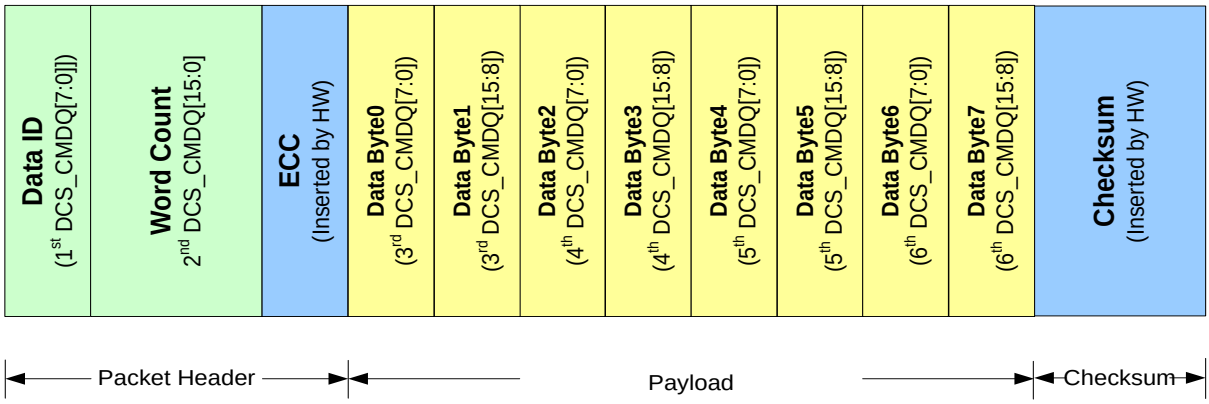


Figure 3.6 DSI Long Command Packet Assembly

The step-by-step procedure is listed below with an example:

1. Choose desired DSI Long Write Packet/Command, ex, 0x29 for Generic Long Write Packet, in register 1st ***DCSCMD_Q[7:0]*** field.
   Note that 1st ***DCSCMD_Q[15]*** is used to indicate if the packet is a short packet or long packet: 0 means short packet and 1 means long packet
   1st ***DCSCMD_Q[14:8]*** is reserved and should be set to 0.

   For example, set register 1st ***DCSCMD_Q[7:0]*** to 0x040 for DSI long packet.

   Write 0x8040 to ***DCSCMD_Q[15:0]*** for DSI long packet – note bit 15 must be set to 1 for long packet

2. Set 2nd ***DCSCMD_Q*** register to the correct word count, number of data bytes in the packet.

3. Check ***DCSCDM_ST (0x0502)*** register for command queue FIFO status:
   - ***[dcs_cm_entry]*** indicates how many FIFO entries are still available for writing to.
   - ***[dcs_cmd_done]*** is incremented by 1 when the DSI packet has been sent out on MIPI interface.
     Note that ***[dcs_cmd_done]*** will wrap around to 0 when it is 3.
   - ***[dcs_cmd_oflow]*** indciates command queue FIFO has overflowed
     Write 1 to ***[dcs_cmd_oflow]*** to clear this bit.
   - ***[dcs_cmd_empty]*** indicates command queue FIFO is empty.
   - ***[dcs_cmd_full]*** indicates command queue FIFO is full.

Example: TX Generic Long Write Packet with 4 bytes of Data: 0x12, 0x34, 0x56, 0x78

DCSCMD_Q (0x0504) = 0x8029 (DSI Long Command/Packet, Data ID = 0x29)
DCSCMD_Q (0x0504) = 0x0004 (WC1,WC0)

DCSCMD_Q (0x0504) = 0x3412 (Data1,Data0)
DCSCMD_Q (0x0504) = 0x7856 (Data3,data2)

Note that for a long packet with WC of 0 please follow the procedure in 3.3.3 TX Short Packet (DCS) Write Command since there is no payload data to write. For example, to perform a DCS Long Write with WC of 0, the following sequence should be used:

DCSCMD_Q (0x0504) = 0x0039 (DCS Long Write, Data ID = 0x39)
Note that bit 15 is 0 just like a short packet.
DCSCMD_Q (0x0504) = 0x0000 (WC1,WC0)

3.3.5. **LPRX Packet Read Command**

TC358870XBG provides a mechanism to receive long and short packets using interrupts and data FIFO. A 32 x 4byte FIFO read by ***DSI_RXFIFO (0x01B8)*** is used to store long packets received during LPRX data transactions. Application may use combination of ***DSI_RX_STATE_INT_STAT (0x01A0) [LPRX_PKT_START]***, ***[LPRX_PKT_DONE]*** and ***[LPRX_THRESH_HIT]*** interrupt to receive long packets of any size. ***[LPRX_THRESH_HIT]*** interrupt is asserted when data in the DSIRX FIFO is greater than or equal to a programmable value ***DSI_LPRX_THRESH_COUNT (0x01C0)***. ***[LPRX_PKT_DONE]*** is asserted when the last data of the long packet is written to the RX FIFO or when a short packet is received. The diagram below shows LPRX packets may be processed by the application using the Register interface.

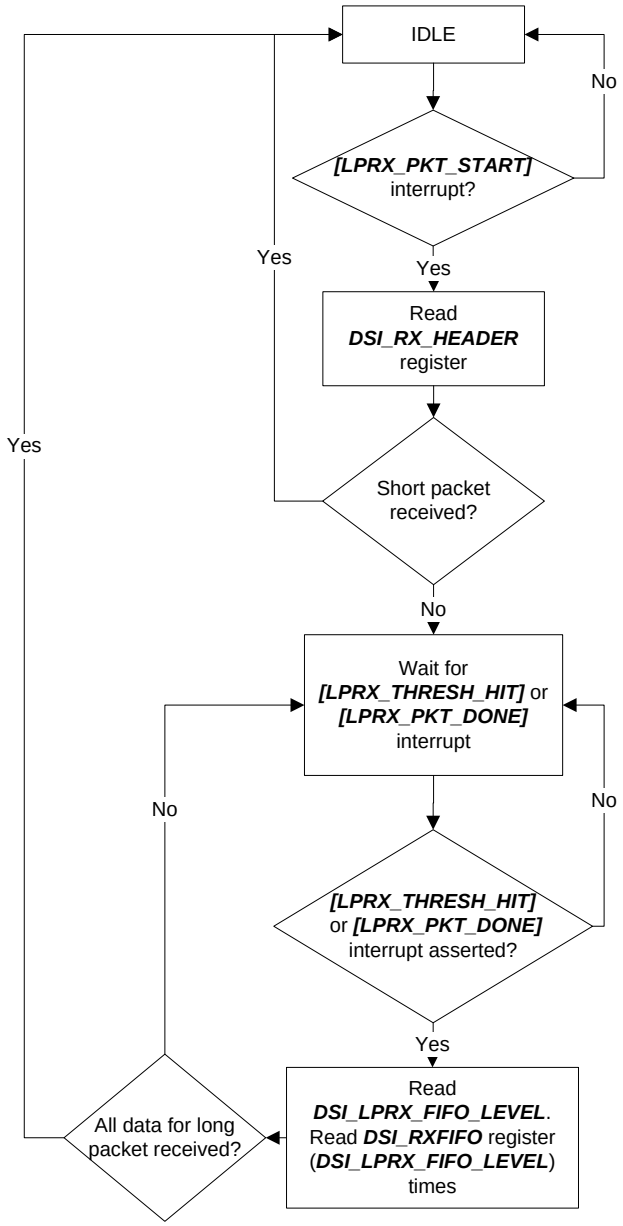


Figure 3.7 Flow diagram for LPRX data reception using Register interface

3.3.6. **3D Support**

For 3D video transmission on DSI, a two byte value continuing all information regarding the transport of stereoscopic content between host processor and display module is sent as part of the Vsync Start Packet. This two-byte value contains information regarding stereoscopic image format, data order, whether or not the stereoscopic display panel is active, and the display orientation. Please refer to the MIPI DSI Spec. for 3D support for details on these parameters.

3.4. CEC Controller

CEC uses a single line to transfer data between TC358870XBG and a HDMI source. Messages are transferred as a single frame, which is built out of a start bit followed by data bits. The bit timing is clearly defined with different timings for the start bit and data bit period. Fixed bit timing is required, because no clock information is transferred over the CEC line.

Each transferred message starts with the transmission of a start bit, which is used to indicate the start of a message and which is also used for arbitration as several device could try to start a transfer. Once arbitration is won, the following information is transmitted in blocks (header block, opcode block and operand block). Each block consists of 8 data bits, one EOM – End Of Message indicator and an acknowledge bit period, where the acknowledge will be used by the addressed device to indicate successful transmission of each block.

TC358870XBG supports the Consumer Electronics Control Protocol as defined in HDMI specification. TC358870XBG offers the physical interface and low level support for data parsing.

3.4.1. **Receive Operation Sequence**

The following are the sequences for CEC Receive operation

- TC358870XBG collects CEC byte data into Receive FIFO (maximum 16 bytes)
- TC358870XBG asserts **INT** once it received a valid byte data in the Receive FIFO or after entire message has been received or there is an error condition on the CEC signal protocol.
- TC358870XBG will keep **INT** at High level until Host complete read out all the Receive data in the FIFO.

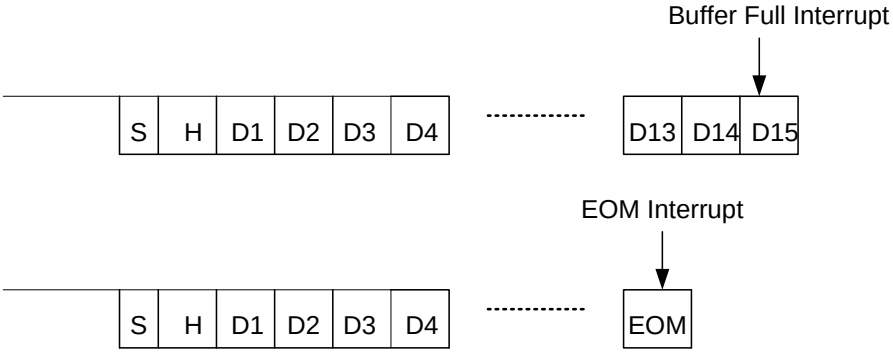


Figure 3.8 CEC reception overview

3.4.1.1. Noise cancellation time

The noise cancellation time is configurable with the ***CECRCTL1 (0x0614) [CECHNC]*** and ***[CECLNC]*** registers. The CEC line is monitored at each rising edge of the sampling clock. In the case that the CEC line has changed from "1" to "0", the change is fully recognized if "0"s of the same number as specified in the ***[CECLNC]*** bit are monitored. In the case that the CEC line has changed from "0" to "1", the change is fully recognized if "1"s of the same number as specified in the ***[CECHNC]*** bit are sampled.

The following figure illustrates the operation when the noise canceling is configured as ***[CECHNC]*** = 0x2 (3 samplings) and ***[CECLNC]*** = 0x3 (4 samplings). By canceling the noise, a signal "1" shift to "0" after "0" is sampled four times. The signal "0" shifts to "1" after "1" is sampled three times.

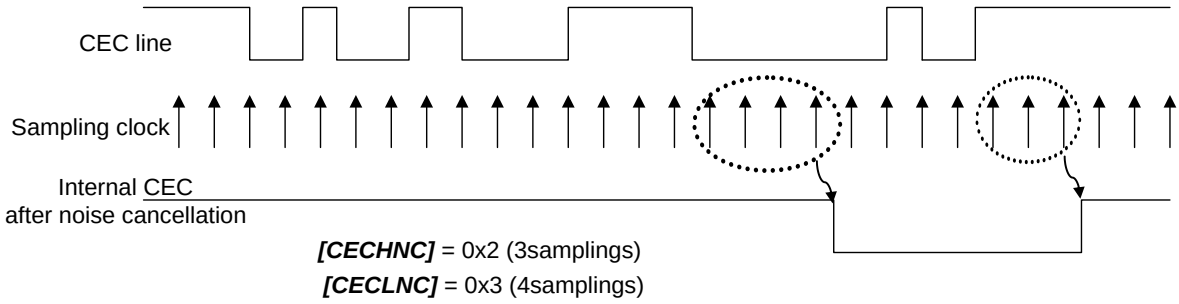


Figure 3.9 CEC noise cancellation example

3.4.1.2. Start bit detection

The following ***CECRCTL2 (0x0618)*** registers used to detect the start bit of CEC line.

- ***[CECSWAV0]*** is used to specify the fastest start bit rising timing.
- ***[CECSWAV1]*** specifies the latest start bit rising timing ((1) in the figure shown below).
- ***[CECSWAV2]*** is used to specify the minimum number of cycles of a start bit (corresponds
- to the length of a start bit measured in sampling clock cycles).
- ***[CECSWAV3]*** specifies the maximum cycle of a start bit ((2) in the figure shown below).

The start bit is considered to be valid if a rising edge during the period (1) and a falling edge during the period (2) are detected.

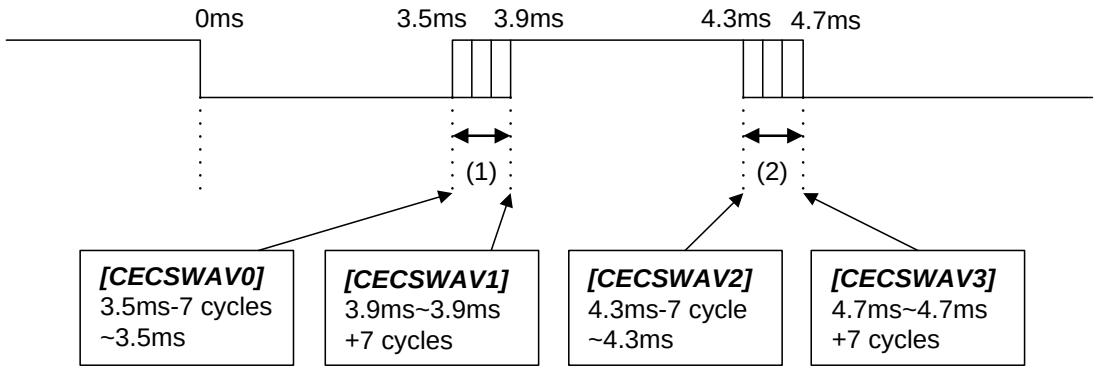


Figure 3.10 CEC start bit detection

3.4.1.3. Waveform Error Detection

The following ***CECRCTL3 (0x061C)*** registers ***[CECWAV0]***, ***[CECWAV1]***, ***[CECWAV2]*** and ***[CECWAV3]*** are used to detect logic transition on CEC line.

A waveform error interrupt is generated if a rising edge is detected during the period (1) or (2) shown below, or if no rising edge is detected in the timing described in (3).

(1) period between the beginning of a bit and the fastest logical "1" rising timing
(2) period between the latest logical "1" rising timing and the fastest logical "0" rising timing
(3) the latest logical "0" rising time

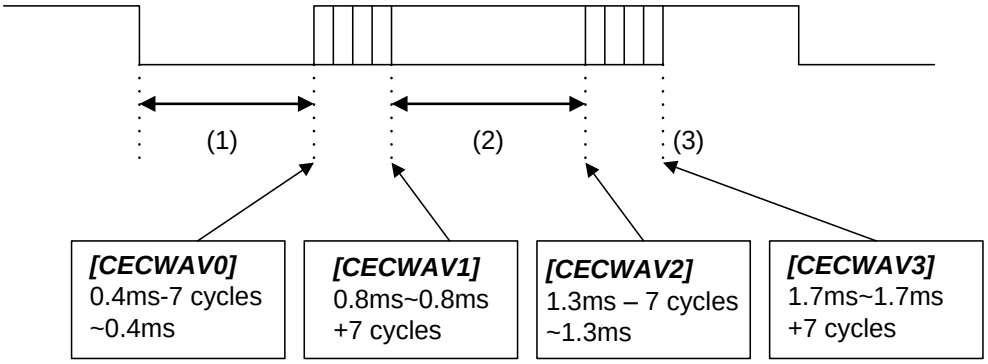


Figure 3.11 waveform error detection

3.4.1.4. Data sampling timing

The figure shown below illustrates a data sampling timing. The ***[CECDAT]*** of ***CECREN (0x060C)*** register specifies the data sampling point per two sampling clock cycles within the range of + or - 6 cycles from the reference point (approx. 1.05 ms).

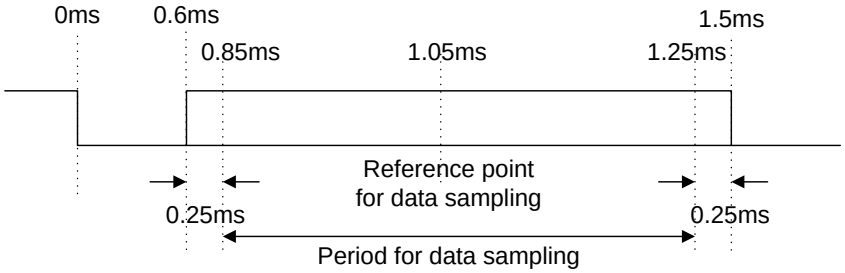


Figure 3.12 sampling time example

3.4.2. **Transmit Operation Sequence**

The following are the sequence for CEC transmit operation

- Write all transmit CEC byte data into Transmit FIFO (maximum 16 bytes)
  - Write "1" to ***CECTEN (0x0620)*** register to start the operation
- TC358870XBG asserts **INT** once CEC transmit operation is completed or there is an error condition on the CEC signal protocol.
  - Host must read the ***CECTSTAT (0x0630)*** register to know the status of the transmitting operation and take appropriate action.

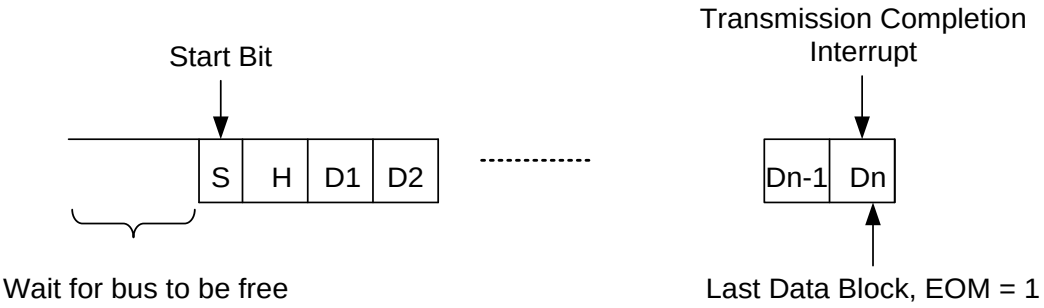


Figure 3.13 CEC transmission example

3.4.2.1. Wait Time for Bus to be Free

The wait time for a bus free check at transmission start is configured with the ***[CECFREE]*** of ***CECTCTL (0x0628)*** register. It can be specified in a range from 1 to 16 sample clock cycles. Start point to check if a bus is free is the end of final bit. If a bus is free for specified bit cycles of "1", transmission starts.

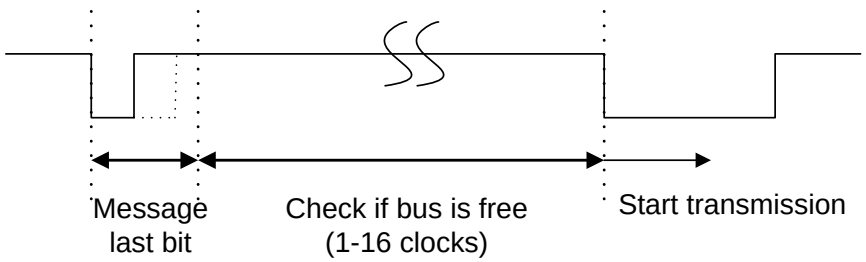


Figure 3.14 Transmission starts

3.4.2.2. Transmission Timing

The timing of the start and data bits can be adjusted with the ***CECTCTL 0x0628*** registers as shown in the figure below

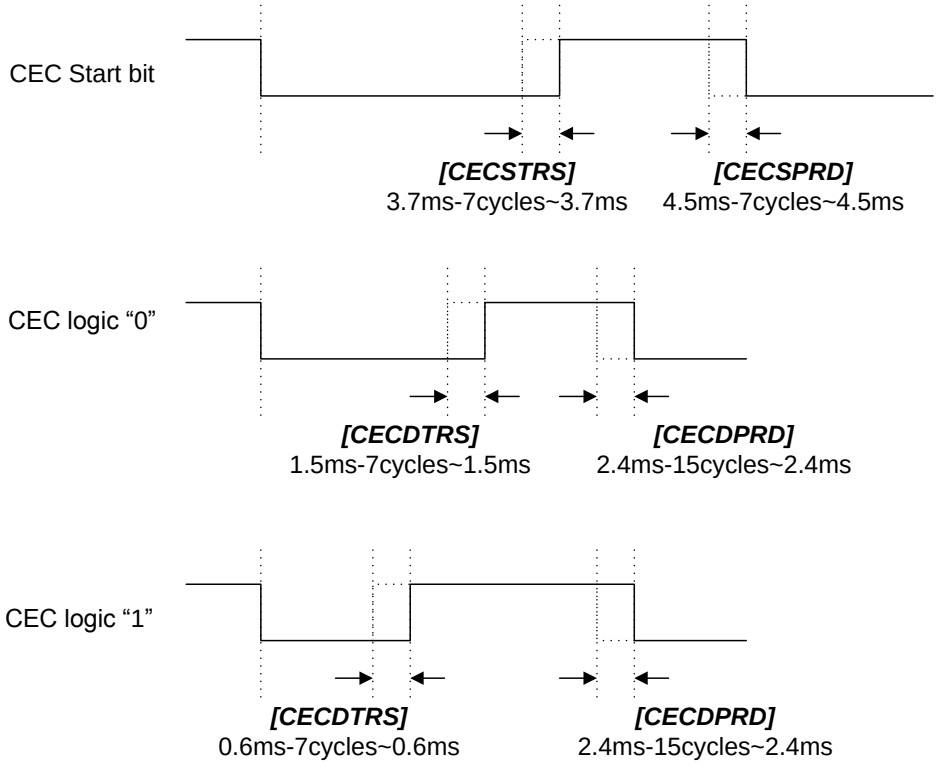


Figure 3.15 Transmission timing

3.4.3. **Arbitration lost**

An arbitration lost error occurs when CEC module detects “0” during the detection windows as shown in the figure below

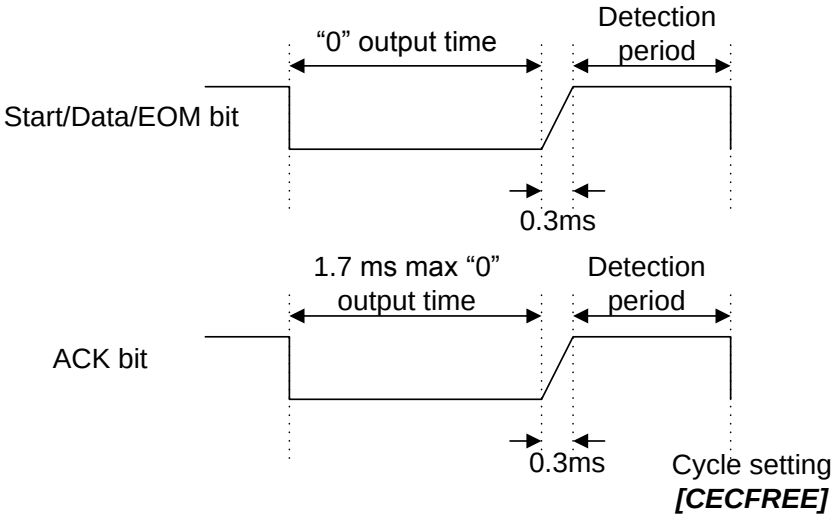


Figure 3.16 Arbitration Error check

3.4.4. **Low level functions**

In order to ensure transmission on the CEC line, the bridge serves the following low-level functions in accordance to the CEC standard:

- Monitoring of CEC line at all times for any incoming message except when CEC module is off (***CECEN (0x0600)*** register is set to "0").
- Line detection (free/occupied). This function tests the line if it is free to be used.
- Data/Frame parsing. Details of the CEC Frames (header, data blocks, EOM, ACK) will be split and stored.
- Acknowledgment of messages (positive/negative). Success or failure of message transmission will be notified to sender.
- Frame retransmission. Conditional retransmission of lost frames,
- Line error handling. Notification mechanism to inform about spurious pulses on the control signal line.
- Line Arbitration. Collision prevention mechanism.

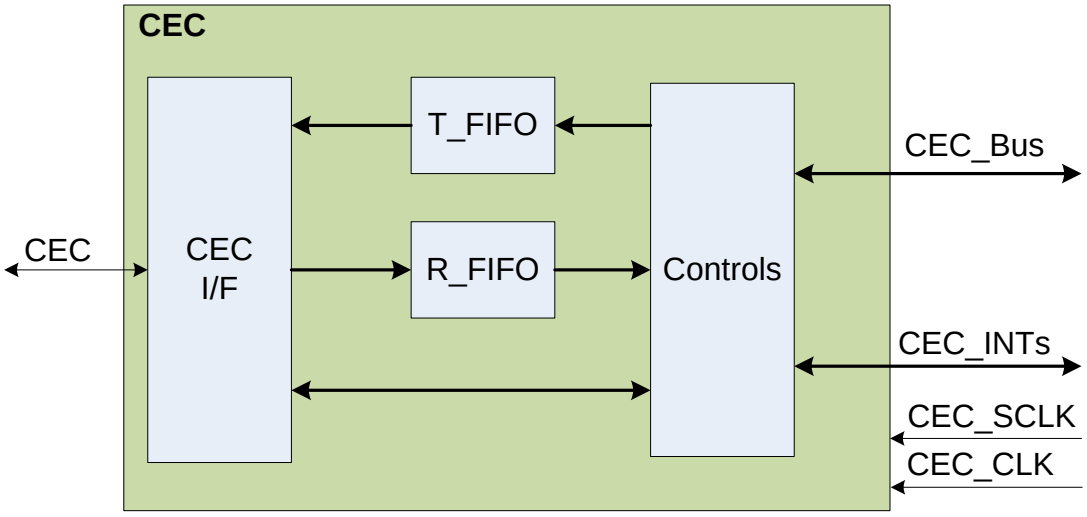


Figure 3.17 CEC Block diagram

3.5. Audio Output Function

TC358870XBG is capable of outputting audio data via I2S I/F, including TDM format.

The sampling frequency 'f_s' can be 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz.

TC358870XBG outputs Over-Sampling clock (**A_OSCK**) with frequency equal to $256f_s$ when applicable.

3.5.1. **I2S Interface**

3.5.1.1. Normal Mode

The basic features of the I2S are outlined below:

- Up to 4 output lines **A_SD0** to **A_SD3**(2 Audio channels per line = up to 8 channels)
- Support 16, 18, 20 or 24 bits data
- Support Left or Right-justify with MSB first
- Support 32 bit-wide time slot only.
- Support only Master Clock option

I2S bus in TC358870XBG is a 3-pin serial link consisting of a line for two time multiplexed data channels (left and right), a word select line and a clock line. Four more pins are provided for optionally providing 3 lines to send 6 additional audio channels and 1 line to provide the audio over-sampling clock. Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock (**A_SCK**), and word-select (**A_WFS**).

When Audio FIFO reaches certain (programmable) level, I2S controller will begin to fetch the data and transfer them over I2S interface. Once the Audio FIFO is empty, I2S controller will finish transfer the last bit of Audio data & then it will keep **A_SCK** Low until it has more data.

Notes

The time-slot is 32 bit-wide. Input data could be 16, 18, 20 or 24 bits and could be left- or right-justify with MSB first or LSB first. There are three formats show in the below figures. Figure xx(a) illustrates Standard Data Format (Sony Format) with Left-Channel “H” and Right-channel “L”, (b) Left Justified Format with Left-channel “L” and Right-channel “H”. For I2S data format, there is one clock delay to latch the data bit.

Below figure shows right justified (SONY) format.

SDO_MODE1 (0x8652) [SDO_FMT] = 0x0

ConfCtl0 (0x0004) [I2Sdlyopt] = 0x0

SDO_MODE0 (0x8651) [LR_POL] = 0x1

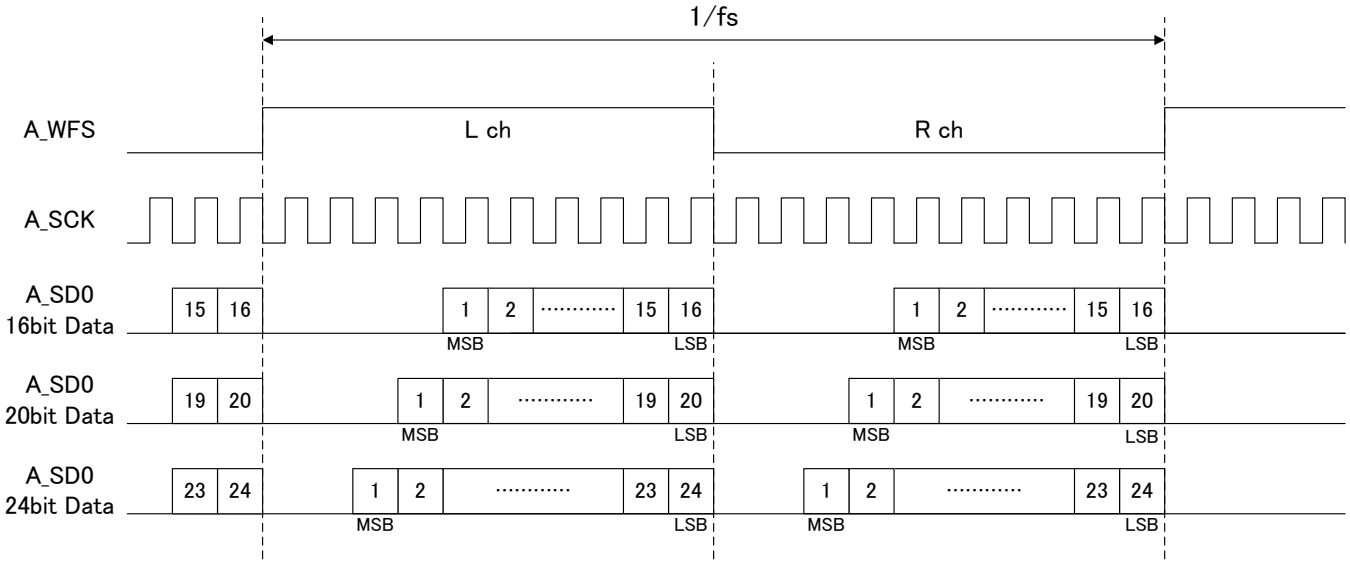


Figure 3.18 Data input timing of standard format (Sony format); L_ch=H, R_ch=L

Below figure shows left justified format.

SDO_MODE1 (0x8652)[SDO_FMT] = 0x1

ConfCtl0 (0x0004) [I2Sdlyopt] = 0x0

SDO_MODE0 (0x8651) [LR_POL] = 0x1

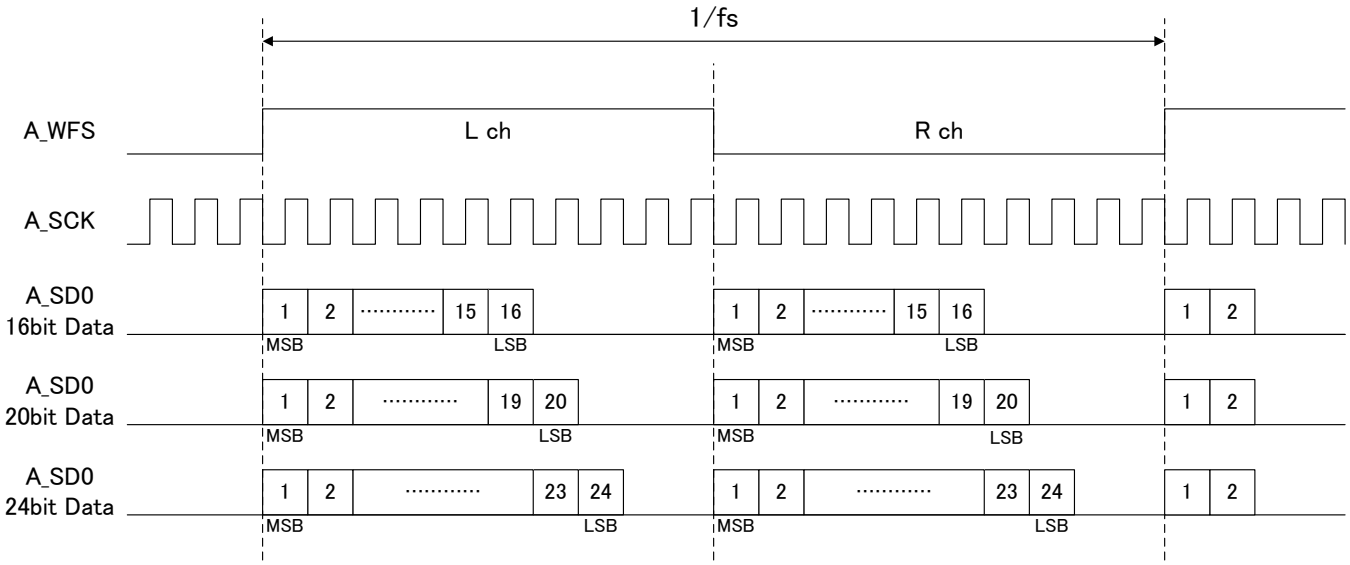


Figure 3.19 Data input timing of Left-Justified format; L_ch=H, R_ch=L

Below figure shows I2S (Philips) format.

SDO_MODE1 (0x8652) [SDO_FMT] = 0x2

ConfCtl0 (0x0004) [I2Sdlyopt] = 0x1

SDO_MODE0 (0x8651] [LR_POL] = 0x0

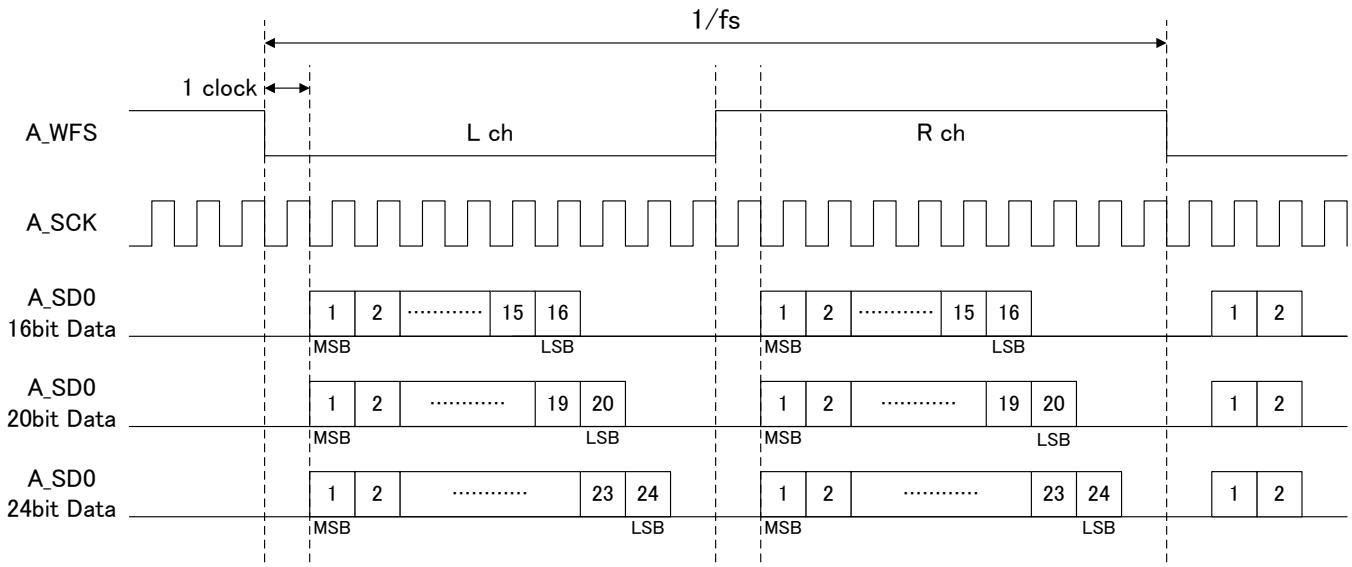


Figure 3.20 Data input timing of I2S data format (Phillips format); L_ch=L, R_ch=H

3.5.1.2. HBR Split over I2S

As a special case over I2S, the HBR audio stream can also be transmitted over the I2S.

But for HBR audio, the F_s is very high.

- F_s=768 kHz: 128fs x 768 kHz =98.304 MHz
- 768 kHz x 64= 49.152 Mbit/lane.

In some scenarios, the I2S ports of the App Processor may not be able to handle this high data rate. To handle such scenarios, the HBR stream can be split across the four (4) I2S data lanes with data rate on each lane reduced by a factor of 4.

Figure below shows how the HBR audio stream will appear on I2S .

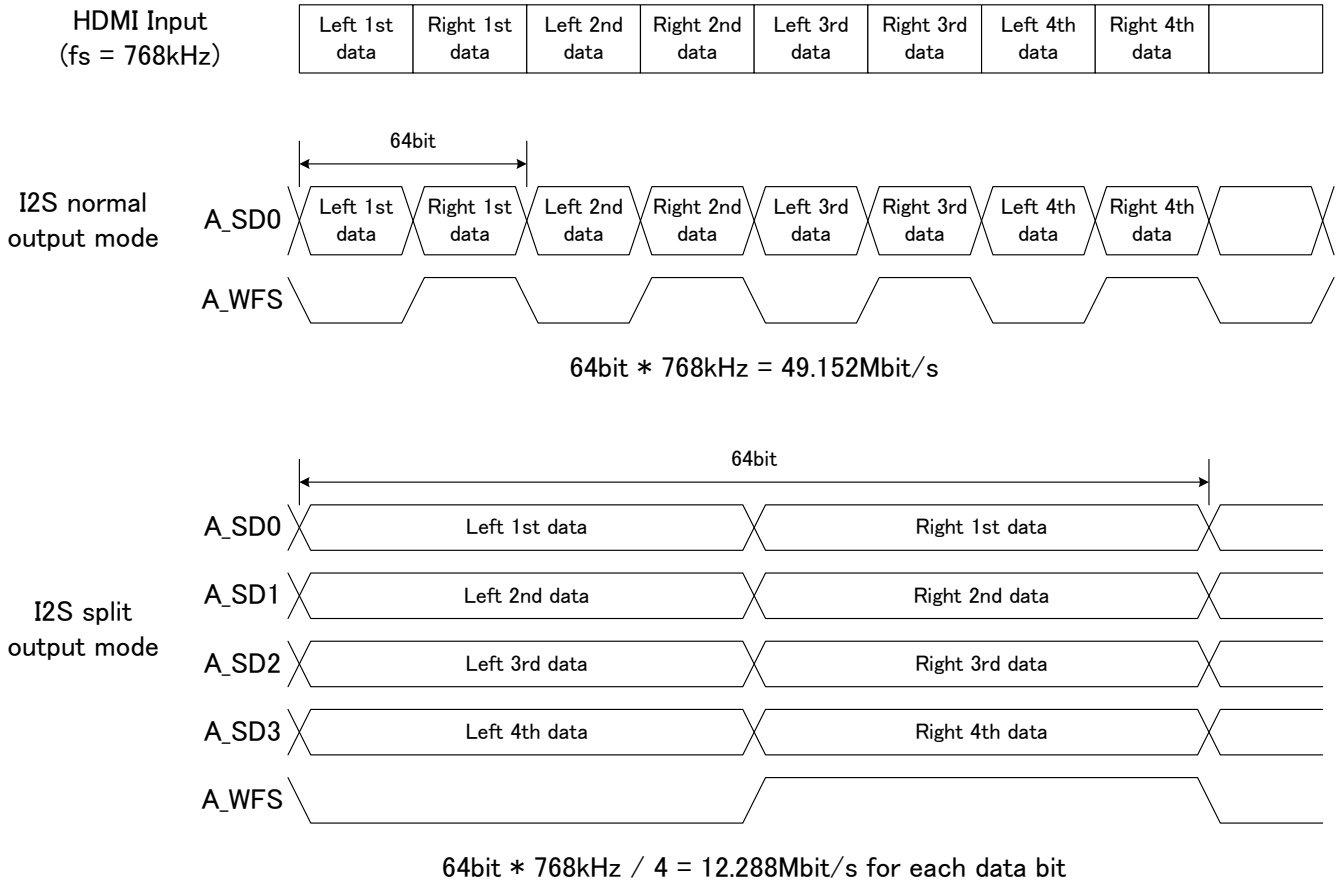


Figure 3.21 HBR Audio stream over 1 I2S lane and four (4) I2S lanes

3.5.2. **TDM (Time Division Multiplexed) Audio Interface**

The basic features of the TDM are outlined below:

- Single output channel
- Support 16, 18, 20 or 24 bits data
- Support up to 8 channels
  - TDM output fixed at 8 channels
  - Fixed at 32 bit-time slot
- Support Master clock only

TDM interface allows multiple channels of data to be transmitted on a single data line. TDM interface is comprised of three signals: a frame synchronization pulse (**A_WFS**), serial clock (**A_SCK**) and serial audio data (**A_SD0**).

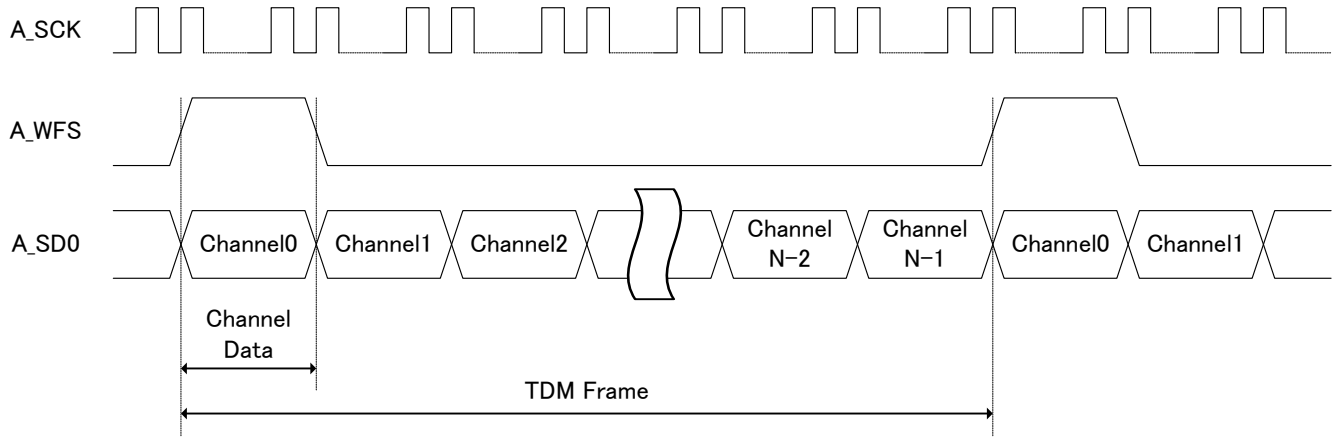


Figure 3.22 I2S N-Channel TDM timing

3.6. InfraRed (IR) Interface

The basic features of the IR are outlined below:

- Support NEC IR protocol
- Store up to 4 byte IR data read by ***IRData (0x005A)***
- Interrupt Host when IR address match and detect "end of message" transmission pulse.
- Programmable timing for Leading High time, Leading Low time, Logical "0" H and L time, Logical "1" H and L time.

Supports NEC IR transmission protocol which uses pulse distance encoding of the message bits. Below figures describes NEC InfraRed protocol.

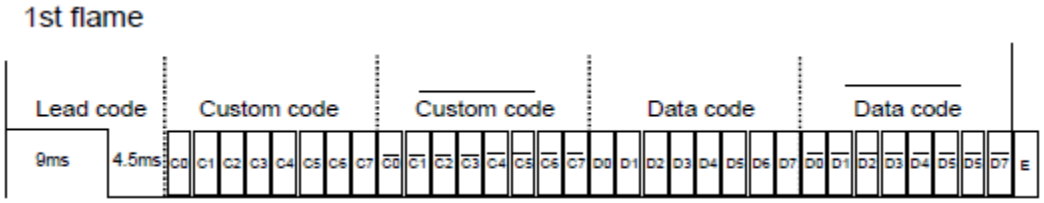


Figure 3.23 NEC Configuration of Frame



Figure 3.24 NEC Bit Description

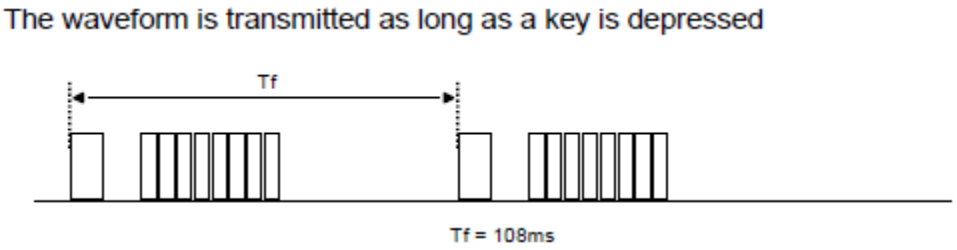


Figure 3.25 NEC Frame Interval (Tf)

3.6.1. **Programmable timing**

There are four programming timing parameters. IR modules use these timing parameters to detect Lead code, Bit H logic, Bit L logic and "END" flag. Below describes these four timing parameters

1. Detect Lead code when:
   (a) H count value is greater than ***LCHmin (0x0034)*** parameter and smaller than ***LCHmax (0x0036)*** parameter.
   (b) L count value is greater than ***LCLmin (0x0038)*** parameter and smaller than ***LCLmax (0x003A)*** parameter.
2. Detect "L" bit when:
   (a) H count value is greater than ***BHHmin (0x003C)*** parameter and smaller than ***BHHmax (0x003E)*** parameter.
   (b) L count value is greater than ***BHLmin (0x0040)*** parameter and smaller than ***BHLmax (0x0042)*** parameter.
3. Detect "H" bit when:
   (a) H count value is greater than ***BLHmin (0x0044)*** parameter and smaller than ***BLHmax (0x0046)*** parameter.
   (b) L count value is greater than ***BLLmin (0x0048)*** parameter and smaller than ***BLLmax (0x004A)*** parameter.
4. Detect "END" flag when:
   (a) After received Lead code – Custom code - /Custom code – Data code - /Data code
   (b) H count value is greater than ***EndHmin (0x004C)*** parameter and smaller than ***EndHmax (0x004E)*** parameter.

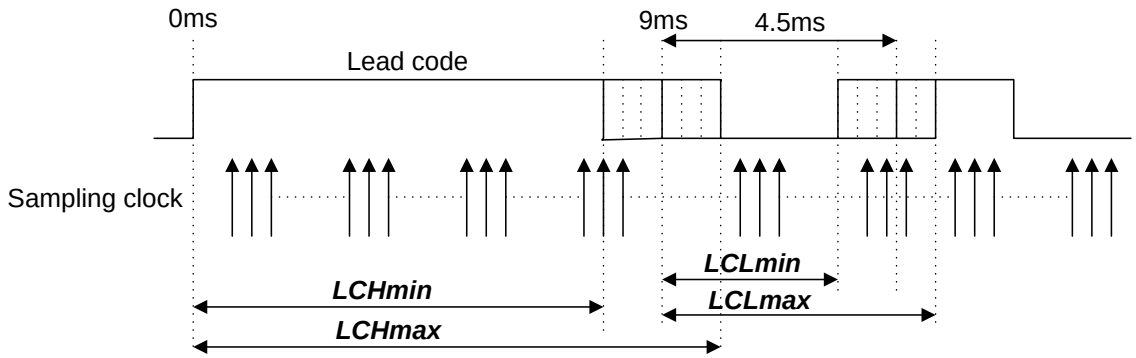


Figure 3.26 Example of Lead Code min/max values for H and L detection

3.6.2. **Basic Operation**

The following shows the IR sequences:

1. Detect Lead code
2. Receive 8-bit Custom code
3. Receive 8-bit Custom code (Inverted)
4. IR logic compare the Receive Custom code against the programmable custom code in ***[IR_ccode]*** of ***IRCtl (0x0058)*** register. If they are match then IR controller continues to collect the data code. Otherwise it will ignore the IR data.
   (a) (Step 5 – 9 assumes Custom code match)
5. Receive 8-bit Data code
6. Receive 8-bit Data code (Inverted)
7. Receive "End" code
8. After IR controller receive the "End" code, **INT** pin will be set (provided that IR_INT is not mask).
   (a) If "End" code is not received – "End" code error flag will be set. **INT** pin will be set (provided that IR_Err is not mask)
9. Host need to read the 8-bit Data code through the I^2C interface. Once the all the IR data code has been read host needs to clear the interrupt by writing "1" to the respective bit of the Interrupt Status register

Note: IR controller has buffer to store maximum 4 bytes of IR Data code and one 8-bit Custom code (for debugging purpose).

3.7. I^2C

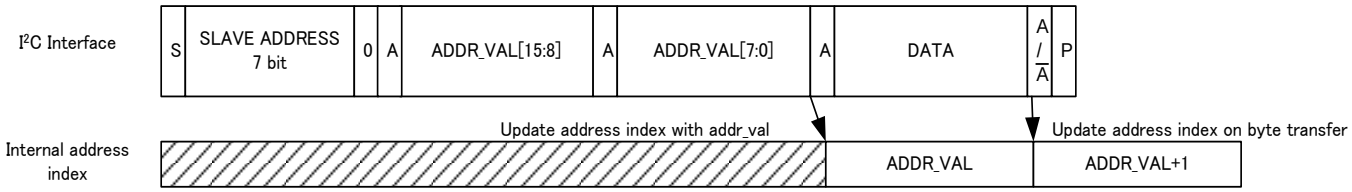
In addition to I^2C function described in section 3.3.1, the I^2C module can be addressed as a slave the following features:

- Up to 400 kHz fast mode operation
- Support special mode – Ultra fast mode 2 MHz
- Supports 7 bit slave addresses recognition
  - ✧ Slave address = 0x0F if **INT** = "Low" during reset
  - ✧ Slave address = 0x1F if **INT** = "High" during reset
- No support for general call address
- Supports 16 bit index value for TC358870XBG I^2C slave access

The I^2C slave function supports a fixed slave address only and does not support general call address. The I^2C slave function does not require any programmable configuration parameters.

3.7.1. **Providing Register Address over I²C Bus**

The I²C slave function requires the interfacing I²C master to provide the register address of the TC358870XBG register to be accessed. The I²C slave function loads the first two bytes following a write command as the register address (address index) to be accessed (see Figure 3.27 and Figure 3.28).



S = Start condition
Sr = Repeated start condition
A = Acknowledge
Ã = Not Acknowledge
P = Stop bit

Figure 3.27 Register Write Transfer over I²C Bus

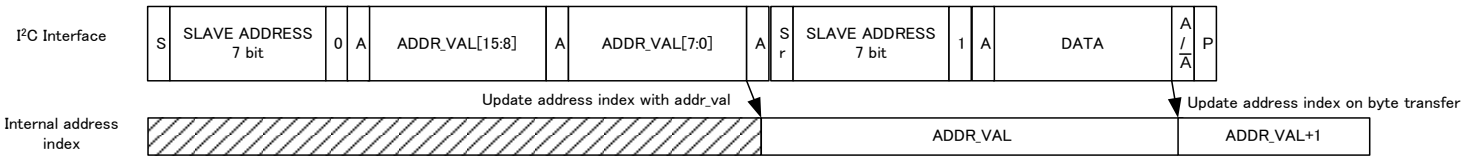


Figure 3.28 Random Register Read Transfer over I²C Bus

I²C slave function supports random write accesses and both random and continuous read accesses (see Figure 3.29).

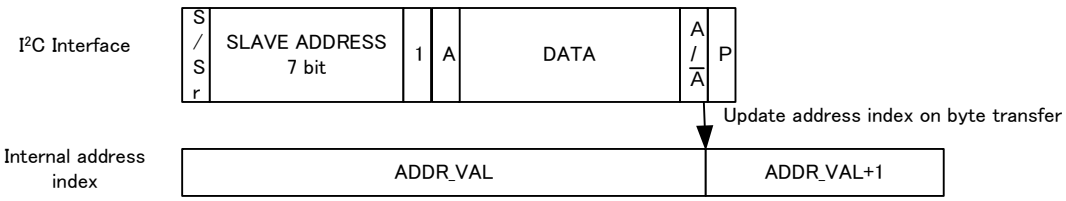


Figure 3.29 Continuous Register Read Transfer over I²C Bus

3.7.2. I²C Write Access Translation

Registers in TC358870XBG are 8, 16 and 32 bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will pack the data to either 8, 16 or 32-bit and write into the register group accordingly.

Note that data transferred on the I²C bus is sent LSB first.

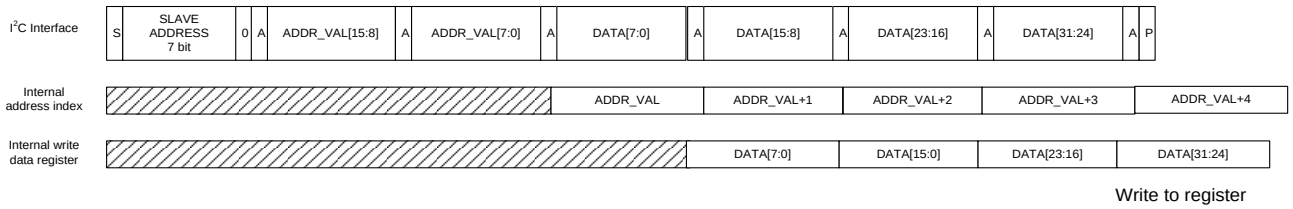


Figure 3.30 I²C Write Transfers Translated to Register Write Accesses

3.7.3. I²C Read Access Translation

Registers in TC358870XBG are 8, 16 and bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will read the 8, 16 or 32 bit data, un-pack the data to 8-bit and send to I²C controller.

Note that data transferred on the I²C bus is sent LSB first.

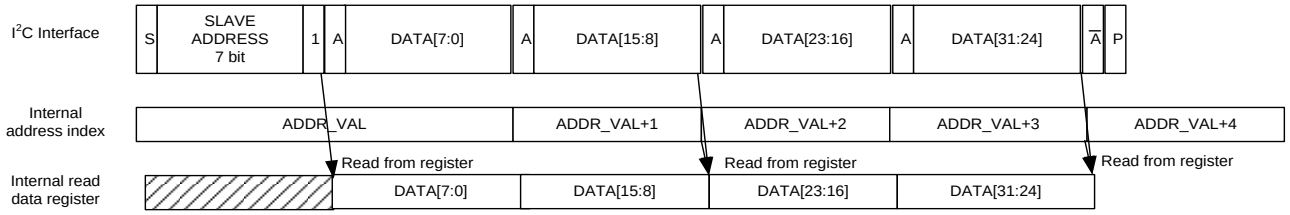
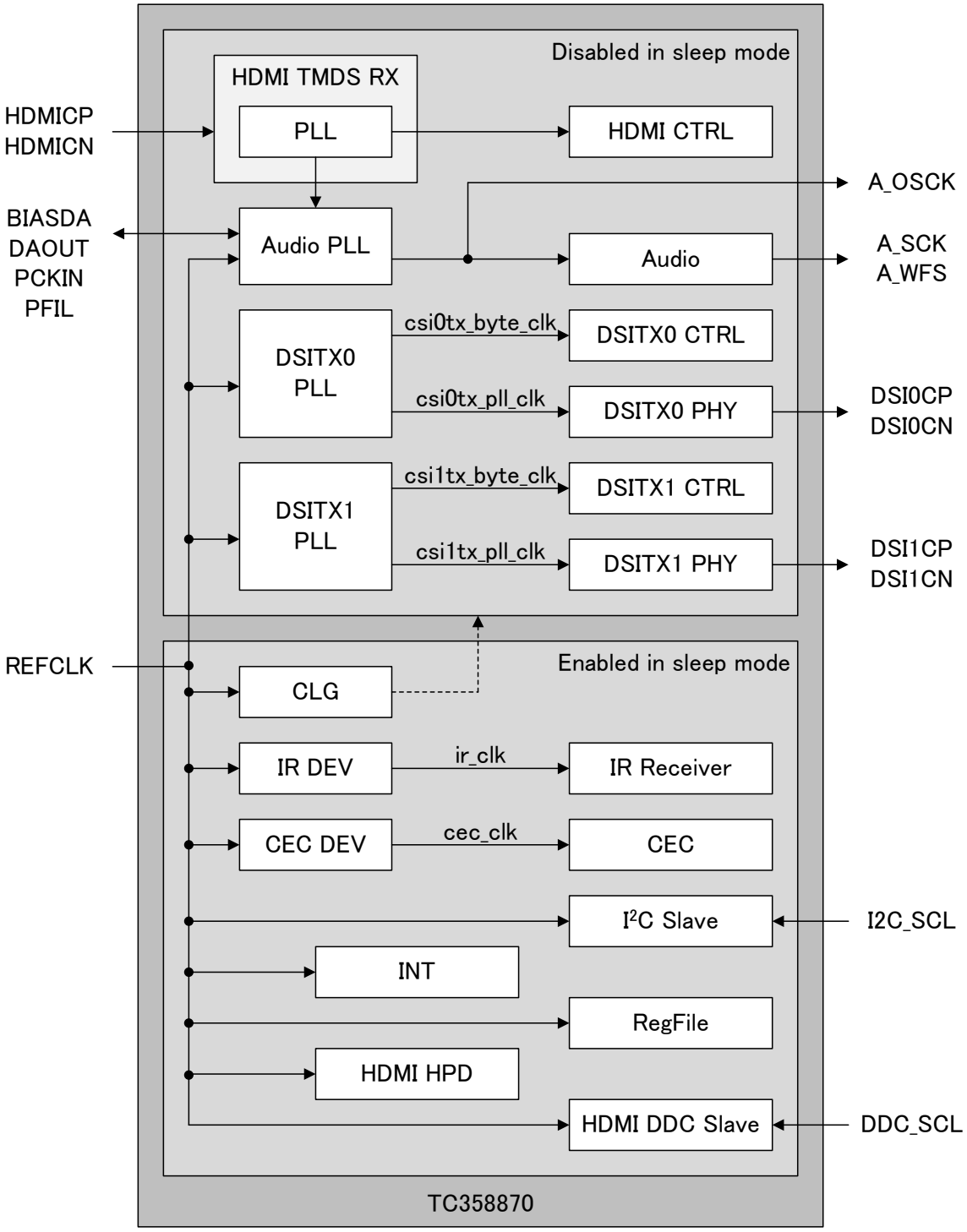


Figure 3.31 I²C Read Transfers to Register Read Accesses

4. Clock and System

TC358870XBG uses totally 4 PLLs.

- One PLL is inside the HDMI Rx PHY and is used to recover the clock from the HDMI stream.
- One PLL is inside the DSI0 Tx and is used to generate the high speed MIPI Tx clock.
- One PLL is inside the DSI1 Tx and is used to generate the high speed MIPI Tx clock.
- One PLL is used to generate the Audio over-sampling clock for audio data recovery.



CLG supports two powers states FULLY ACTIVE and SLEEP where clocks are disabled or PLL is disabled to reduce power consumption. SLEEP state is controlled by below registers.

Table 4.1 SLEEP mode control registers

Step (Note1)	*Address*	*Register*	*Field*	**Function**
1	***0x0004***	***ConfCtl0***	***[ABuf_en] [Vtx1_en] [Vtx0_en]***	Audio and Video control
2	***0x02A0 0x04A0***	***MIPI_PLL_CTRL***	***[MP_CKEN] [MP_ENABLE]***	MIPI clock and PLL control (Note2)
3	***0x0002***	***SysCtl***	***[SLEEP]***	Sleep mode control
4	***0x8410***	***PHY_CTL***	***[PHYCtl]***	HDMI PHY control
5	***0x84F0***	***APLL_CTL***	***[APPL_ON]***	Audio PLL control
6	***0x8413***	***PHY_ENB***	***[PHYEnb]***	HDMI PHY control

Note1: Shows entry steps. Exit steps are reverse order.

Note2: Shall be controlled after ***0x01B0*** and ***0x03B0 DSITX_INTERNAL_STAT*** become 0x0000.

In FULLY ACTIVE: PLL and TC358870XBG system clock are enabled. Depending on the configuration, I^2C controllers may also be enabled.

In SLEEP: PLL is disabled and no clocks are output.

- Only I^2C slave, IR Receiver, DDC Slave and CEC interfaces are enabled.
- To wake up TC358870XBG
  - ✧ Host must wake up TC358870XBG by programming enable to sleep mode registers .
  - ✧ During Sleep state, TC358870XBG will interrupt Host if either DDC Slave or CEC accesses to TC358870XBG.
- This state may be used by TC358870XBG to safely update PLL parameters when required by Host.

CLG (Clock module) uses an external input clock **REFCLK** (40 MHz to 50 MHz) to generate clocks required by internal controllers.

4.1. Clocks Generation

4.1.1. CEC clock divider configuration

CEC system clock (cec_clk) is generated from **REFCLK** with divide option for High time and Low time.

There are two parameters

(1) ***CecHclk 0x0028*** register contains the cec_clk HIGH time count (counts with **REFCLK**). HIGH time has range of 1 to 2048 **REFCLK** clock.

(2) ***CecLclk 0x002A*** register contains the cec_clk LOW time count (counts with **REFCLK**). LOW time has range of 1 to 2048 **REFCLK** clock .

4.1.2. IR clock divider configuration

IR sampling clock (ir_clk) clock is generated from **REFCLK** with divide option for High time and Low time.

There are two parameters

(1) ***IrHclk 0x002C*** register contains the ir_clk HIGH time count (counts with **REFCLK**). HIGH time has range of 1 to 2048 **REFCLK** clock.

(2) ***IrLclk 0x002E*** register contains the ir_clk LOW time count (counts with **REFCLK**). LOW time has range of 1 to 2048 **REFCLK** clock.

4.1.3. DSI PLL configuration

DSI clocks (dsitx_pll_clk and dsitx_byte_clk) are generated by the DSITX0/1_ PLL and is used for reading data from the final video and audio buffers and for handling the data through the DSI Tx stage.

The possible clock frequencies generated from the DSITX0/1 PLL are achieved by varying the values in registers ***MIPI_PLL_CONF (0x02AC)***.

dsitx_pll_clk = **REFCLK** * [(***[MP_FBD]*** + 1)/ (***[MP_PRD]*** + 1)] * [1 / (2^***[MP_FRS]***)]

Table 4.2 provides possible frequencies that may be used in TC358870XBG.

Table 4.2 Possible DSITX0/1_PLL parameters

Reference clock (MHz)	*[MP_FBD]*	*[MP_PRD]*	*[MP_FRS]*	DSItx_pll_clk (MHz)
40	255	7	1	640
	319	5	2	533.33
	319	6	2	457.143
	319	7	2	400.00

4.1.4. Audio PLL configuration

Audio PLL configuration depends on **REFCLK**. Set each value based on below formula.

[LOCK_REF_FREQ] of ***LOCK_REF_FREQA-C*** (***0x8630 to 0x8632***)

[LOCK_REF_FREQ] = **REFCLK**(Hz) / 100

[NCO_48F0] of ***NCO_48F0A-D*** (***0x8671 to0x8674***)

[NCO_48F0] = 6144000 * 2^28 / **REFCLK**(Hz)

[NCO_44F0] of ***NCO_44FA-D*** (***0x8675 to 0x8678***)

[NCO_44F0] = 5644800 * × 2^28 / **REFCLK**(Hz)

4.2. Power Up Procedure

The following sequence should happen before TC358870XBG is able to operate properly:

1. Provide voltage and clock sources to TC358870XBG.
   - Keep all the input signals at either “Hi-z” or “logic low” state before powering on TC358870XBG.
2. For voltage source, it is desired to turn on core power (1.1V) source first, then Analog PHY and IO (1.8V) power as shown in Figure 4.1.
3. **REFCLK** clock source can be 40 – 50 MHz.
4. The timing parameters for Figure 4.1 are tabulated in Table 4.3.

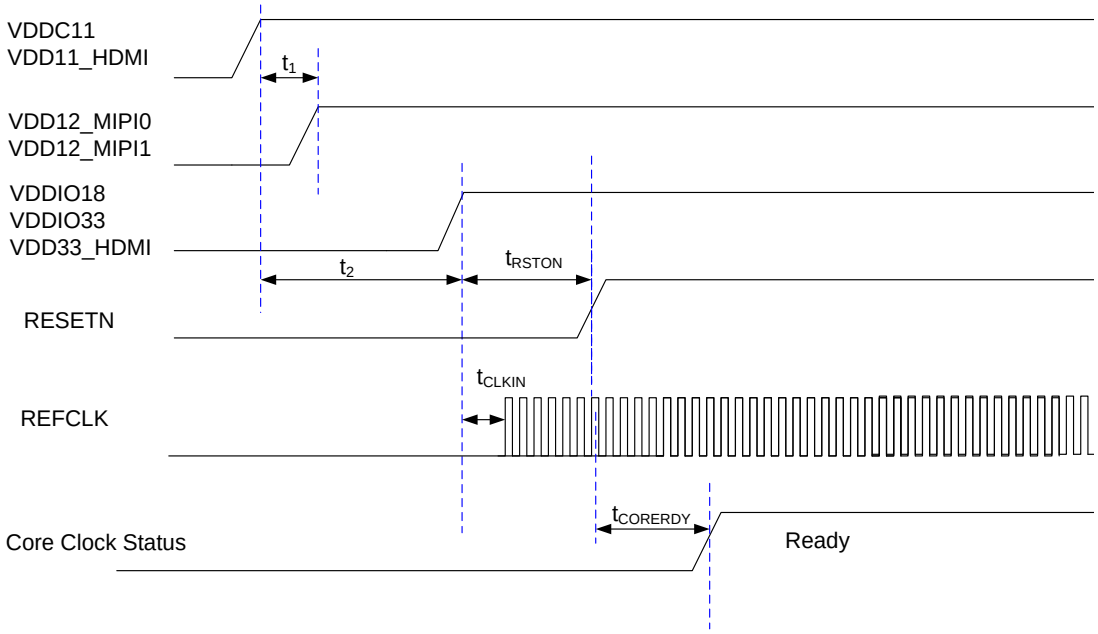


Figure 4.1 Power On Sequence

Table 4.3 Power On Sequence Timing

Item	Symbol	Min	Typ.	Max	Units
Reference clock frequency	REFCLK	40	-	50	MHz
VDD12_MIPI0/1 on delay from VDDC11.	t_1	0	-	10	ms
VDDIO18, VDDIO33, VDD33_HDMI on delay from VDDC11, VDD11_HDMI	t_2	0	-	10	ms
RESET width period	t_{RSTON}	200	-	-	ns
REFCLK input from VDDIO33	t_{CLKIN}	0	-	-	s
Period after reset de-assertion when TC358870XBG clocks are stable (Dependent on REFCLK frequency)	$t_{CORERDY}$	0.7	-	1	ms

4.3. Power Down Procedure

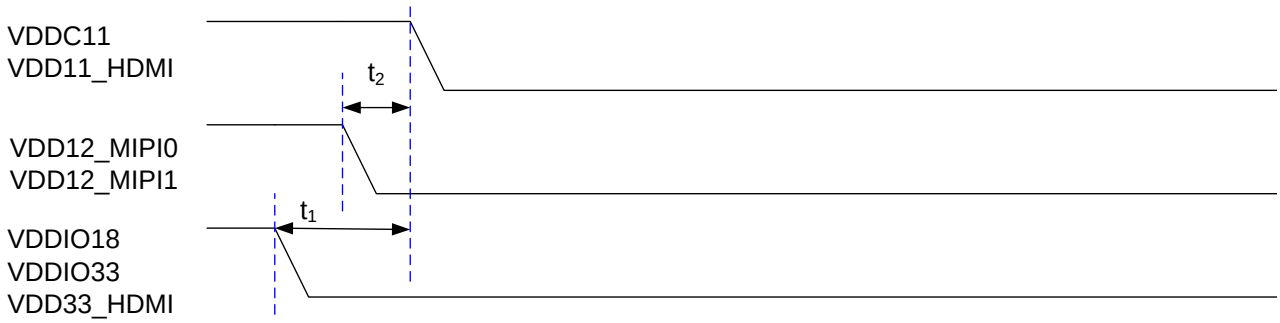


Figure 4.2 Power Down Sequence

Table 4.4 Power Down Sequence Timing

Item	Symbol	Min	Typ.	Max	Units
VDDC11, VDD11_HDMI off delay from VDDIO18/33, VDD33_HDMI	t_1	0	-	10	ms
VDD12_MIPI0/1 off delay from VDDC11 off	t_2	0	-	10	ms

5. RegFile Block (Reg)

The application processor (ISP) accesses TC358870XBG RegFile block to read status and/or write control registers through the I^2C slave interface.

5.1. Register Map

The Overall I^2C Offset address map table is provided in below Tables.

Table 5.1 Global Register Map

Segment Address	Module
0x0000 – 0x0013	Global Control Register
0x0014 – 0x001F	Interrupt Register
0x0028 – 0x002B	CEC Clock Control Register
0x002C – 0x00DF	IR Control Register
0x0080 – 0x008F	IO Control Register
0x0100 – 0x02FF	DSI_0-TX Control Register
0x0300 – 0x04FF	DSI_1-TX Control Register
0x0500 – 0x05FF	DSI-TX Wrapper Register
0x0600 – 0x06FF	CEC Register
0x0700 – 0x07FF	Reserved
0x0800 – 0x4FFF	Reserved
0x5000 – 0x5FFF	Splitter registers
0x6000 – 0x6FFF	Reserved
0x7000 – 0x709F	Internal Color Bar Control Register
0x70A0 – 0x7FFF	Reserved
0x8000 – 0x9FFF	HDMIRX
0xA000 -	Reserved

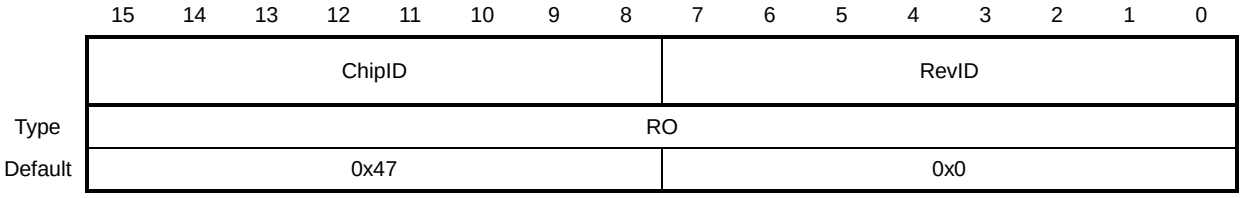
Note:

- HDMI registers are 8-bit register.
- CEC registers are 32-bit register. Host must write two consecutive 16-bit register write to form 32-bit access.
- Note: DSI registers cannot be accessed when video transfer is in progress.

The following sections provide a detailed description of the registers.

5.2. Global

5.2.1. **Chip and Revision ID (ChipID: 0x0000)**



Register Field	Bit	Description
ChipID	[15:8]	Chip ID Chip ID assigned for this device by Toshiba.
RevID	[7:0]	Revision ID Revision ID for this device assigned by Toshiba.

5.2.2. **System Control Register (SysCtl: 0x0002)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	ABRst	Reserved	SPLRst	IRRst	CecRst	CTxRst	HdmiRst	I2S_Dis	Reserved						SLEEP
Type	RO	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	RO						R/W
Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1

Register Field	Bit	Description
ABRst	14	Audio Block Software Reset (Active high) This bit is set to force Audio Block logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear ABRst when set.
SPLRst	12	SPLitter Software Reset (Active high) This bit is set to force VIP logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear VIPRst when set.
IRRst	11	IR Software Reset (Active high) This bit is set to force IR logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear IRReset when set.
CecRst	10	CEC Software Reset (Active high) This bit is set to force CEC logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CECReset when set.
CTxRst	9	DSI-TX Software Reset (Active high) This bit is set to force DSI-TX0 and DSI-TX1 logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CReset when set.
HdmiRst	8	HDMI-RX Software Reset (Active high) This bit is set to force HDMI-RX logic to reset state except all configuration registers content (regFile) and I^2C slave module. 0: Normal operation 1: Reset operation Software needs to clear HReset when set.
I2S_Dis	7	I2S Interface Disable (Active high) Control to disable I2S output interface (applies when ConfCtl.SLMB_en=0) 0: Enable I2S output interface 1: Disable I2S output interface Software needs to enable this (disabled by default).
SLEEP	0	SLEEP control 0: Normal operation 1: Sleep mode

5.2.3. **Configuration Control Register 0 (ConfCtl0: 0x0004)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TX_msel	Reserved	Reserved	AClkOpt	AudChNum		AudChSel	I2SDlyOpt	YCbCrFmt		ABuf_en	AudOutSel		AutoIndex	Vtx1_en	Vtx0_en
Type	R/W	RO	RO	R/W	R/W		R/W	R/W	R/W		R/W	R/W		R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TX_msel	[15]	DSITX Mode Select 0: DSI-TX mode 1: Reserved
Reserved	13	
AClkOpt	12	Audio Bit Clock Option 0: I2S/TDM clock are free running 1: I2S/TDM clock stops when Mute active
AudChNum	[11:10]	Audio Channel Output Channels 00: Enable 8 Audio channels 01: Enable 6 Audio channels 10: Enable 4 Audio channels 11: Enable 2 Audio channels Note: valid only AudChSel = 1
AudChSel	9	Audio Channel Number Selection Mode 0: Auto detect by HW 1: Select by AudChNum register bits Note: valid only when AudOutSel[4] = 0
I2SDlyOpt	8	I2S/TDM Data Delay Option 1'b0: No delay 1'b1: Delay by 1 clock
YCbCrFmt	[7:6]	YCbCr Video Output Format select 00: Select YCbCr444 data format 01: Select YCbCr422 12-bit data format 10: Select VPID2 parameter as data format 11: Select YCbCr422 8-bit (HDMI YCbCr422 12-bit data format, discard last 4 data bits) Note: RGB data, this field has to be set to 2'b00
ABuf_en	5	Audio TX Buffer Enable 0: disable 1: enable Note: enable only after HDMIRX and DSITX register have been setup.
AudOutSel	[4:3]	Audio Output option 0x: Reserved 10: Audio output to I2S I/F 11: Audio output to TDM I/F Note: please initialize to either “10” or “11”.
AutoIndex	2	I^2C slave index increment 0: I^2C address index does not increment on every data byte transfer 1: I^2C address index increments on every data byte transfer
Vtx1_en	1	Video TX1 Enable 0: disable 1: enable Note: enable only after HDMIRX and DSITX1 register have been setup.
Vtx0_en	0	Video TX0 Enable 0: disable 1: enable Note: enable only after HDMIRX and DSITX0 register have been setup.

5.2.4. **Configuration Control Register 1(ConfCtl1: 0x0006)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								Reserved				dcs_clks	tx_msen	tx_ofmt	
Type	RO								RO				R/W	R/W	R/W	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
dcs_clks	3	CDSI Tx SysClk source 0: HDMIRX Pxclk 1: Refclk Note: After Reset when HDMI Rx PClk is not available, set this bit to '1' is required in order to issue DSI commands for programming panel.
tx_msen	2	Magic Square Enable 0: Disable 1: Enable (for RGB666 only)
tx_ofmt	[1:0]	DSITX Output Format select 0x: RGB888 10: RGB666 packed 11: RGB666 loosely packed

5.2.5. **I2S_IO_CTL (I2S_IO_CTL: 0x0072)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												I2SCtl4	I2SCtl3	I2SCtl2	I2SCtl1
Type	RO												R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I2SCtl4	3	I2S Ctl4 CTL4 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl3	2	I2S Ctl3 CTL3 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl2	1	I2S Ctl2 CTL2 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl1	0	I2S Ctl1 CTL1 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins

5.2.6. **I2S PUDCTL (I2S PUDCTL: 0x0084)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		A_SD_3Pu	A_SD_3Pd	A_SD_2Pu	A_SD_2Pd	A_SD_1Pu	A_SD_1Pd	A_SD_0Pu	A_SD_0Pd	A_WFSPu	A_WFSPd	A_SCKPu	A_SCKPd	A_OSCKPu	A_OSCKPd
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[15:14]	These bits are write-able but the writes are ignored as these bits are not used anywhere.
A_SD_3Pu	13	A_SD_3 Pull Up
A_SD_3Pd	12	A_SD_3 Pull Down
A_SD_2Pu	11	A_SD_2 Pull Up
A_SD_2Pd	10	A_SD_2 Pull Down
A_SD_1Pu	9	A_SD_1 Pull Up
A_SD_1Pd	8	A_SD_1 Pull Down
A_SD_0Pu	7	A_SD_0 Pull Up
A_SD_0Pd	6	A_SD_0 Pull Down
A_WFSPu	5	A_WFS Pull Up
A_WFSPd	4	A_WFS Pull Down
A_SCKPu	3	A_SCK Pull Up
A_SCKPd	2	A_SCK Pull Down
A_OSCKPu	1	A_OSCK Pull Up
A_OSCKPd	0	A_OSCK Pull Down

5.2.7. **I2S Control Register (I2SCtl: 0x7082)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													I2SWFSInv	Reserved	I2SSCKInv
Type	RO													R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[15:3]	0x0	These bits used by IR Control Register
I2SWFSInv	2	0x0	I2SWFSInv (Option to use inverted or non-inverted I2S Word Select Clock) 1: Invert I2S WFS Polarity
Reserved	1	0x0	These bits used by IR Control Register
I2SSCKInv	0	0x0	I2SSCKInv (Option to use inverted or non-inverted I2S Shift Clock) 1: Invert I2S Shift Clock Polarity

Note: This register shares the address with the IR Control Register

5.3. Interrupt Registers

5.3.1. **Interrupt Status Register (IntStatus: 0x0014)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				DSITX1_INT	AMUTE_INT	HDMI_INT	DSITX0_INT	Reserved	Reserved	SYS_INT	CEC_EINT	CEC_TINT	CEC_RINT	IR_EINT	IR_DINT
Type	RO				W1C	W1C	W1C	W1C	RO	RO	W1C	W1C	W1C	W1C	W1C	W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DSITX1_INT	11	DSI-TX1 Interrupt Status
AMUTE_INT	10	Audio Mute Interrupt Status 0: Normal 1: Audio change from Normal to Mute Default = 0 (Value immediately becomes '1' after reset)
HDMI_INT	9	HDMI-RX Interrupt Status Note: all HDMI interrupt flags defined in HDMI register space
DSITX0_INT	8	DSI-TX0 Interrupt Status
SYS_INT	5	TC358870XBG System Interrupt Status 0: Normal 1: Video/Audio Overflow/Underflow/WakeUp occurs
CEC_EINT	4	CEC Error Interrupt Status 0: Normal 1: CEC Errors occurs
CEC_TINT	3	CEC Transmit Interrupt Status 0: Idle 1: Transmit completed/done
CEC_RINT	2	CEC Receive Interrupt Status 0: Idle 1: Data Received
IR_EINT	1	IR Error Interrupt Status 0: No Error 1: Error occurs (overflow error)
IR_DINT	0	IR Data Interrupt Status 0: Idle 1: Interrupt occurs (IR Data available)

Note: Write “1” to clear Interrupt. Interrupt is only active when INT_MASK = 1'b0.

Note: Pls. clear the interrupt source first (e.g. CEC interrupt bit in CEC interrupt clear register) before clearing the status bit in this register.

5.3.2. **Interrupt Mask Register (IntMask: 0x0016)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				DSITX1_MSK	AMUTE_MSK	HDMI_MSK	DSITX0_MSK	Reserved	Reserved	SYS_MSK	CEC_EMSK	CEC_TMSK	CEC_RMSK	IR_EMSK	IR_DMSK
Type	RO				R/W	R/W	R/W	R/W	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DSITX1_MSK	11	DSI-TX1 Interrupt Mask
AMUTE_MSK	10	Audio Mute Interrupt Mask
HDMI_MSK	9	HDMI-RX Interrupt Mask
DSITX0_MSK	8	DSI-TX0 Interrupt Mask
SYS_MSK	5	SYS Interrupt Mask
CEC_EMSK	4	CEC Error Interrupt Mask
CEC_TMSK	3	CEC Transmit Interrupt Mask
CEC_RMSK	2	CEC Receive Interrupt Mask
IR_EMSK	1	IR Error Interrupt Mask
IR_DMSK	0	IR Data Interrupt Mask 0: Enable Interrupt 1: Mask Interrupt

Note: if *MSK=1'b1 then *INT is never asserted

5.3.3. **Interrupt Flag Register (IntFlag: 0x0018)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				DSITX1_FLG	AMUTE_FLG	HDMI_FLG	DSITX0_FLG	Reserved	Reserved	SYS_FLG	CEC_EFLG	CEC_TFLG	CEC_RFLG	IR_EFLG	IR_DFLG
Type	RO				RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DSITX1_FLG	11	DSI-TX1 Interrupt Flag
AMUTE_FLG	10	Audio Mute Interrupt Flag Default = 0 (Value immediately becomes '1' after reset)
HDMI_FLG	9	HDMI-RX Interrupt Flag
DSITX0_FLG	8	DSI-TX0 Interrupt Flag
SYS_FLG	5	SYS Interrupt Flag
CEC_EFLG	4	CEC Error Interrupt Flag
CEC_TFLG	3	CEC Transmit Interrupt Flag
CEC_RFLG	2	CEC Receive Interrupt Flag
IR_EFLG	1	IR Error Interrupt Flag
IR_DFLG	0	IR Data Interrupt Flag 0: Idle 1: Interrupt occurs (Data available)

Note: *MASK does not affect these flag status

5.3.4. **SYS Interrupt Status Register (IntSYSStatus: 0x001A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															HPI_chg
Type	RO															RO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
HPI_chg	0	HPDI status 0: Normal 1: change Note: only valid during sleep mode. Use to wake up the host when HDPI is changing.

Note: These status will be clear when write “1” to SYS_INT register bit in IntStatus register.

5.4. IR Registers

5.4.1. IR Clock High Time Register 0 (IrHclk: 0x002C)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					irhclk			irhclk							
Type	RO					R/W			R/W							
Default	0	0	0	0	0	0	1	0	0x29							

Register Field	Bit	Description
irhclk	[10:0]	IR Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk …

5.4.2. IR Clock Low Time Register 0 (IrLclk: 0x002E)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					irlclk			irlclk							
Type	RO					R/W			R/W							
Default	0	0	0	0	0	0	1	0	0x29							

Register Field	Bit	Description
Irlclk	[10:0]	IR Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk …

5.4.3. IR Lead Code HMin Register (LCHmin: 0x0034)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				lchmin				lchmin							
Type	RO				R/W				R/W							
Default	0x0				0x1				0x50							

Register Field	Bit	Description
lchmin	[11:0]	IR Lead Code H Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.4. **IR Lead Code HMax Register (LCHmax: 0x0036)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				lchmax				lchmax							
Type	RO				R/W				R/W							
Default	0x0				0x1				0x64							

Register Field	Bit	Description
lchmax	[11:0]	IR Lead Code H Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.5. **IR Lead Code LMin Register (LCLmin: 0x0038)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				lclmin				lclmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0xA3							

Register Field	Bit	Description
lclmin	[11:0]	IR Lead Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.6. **IR Lead Code LMax Register (LCLmax: 0x003A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				lclmax				lclmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0xB7							

Register Field	Bit	Description
lclmax	[11:0]	IR Lead Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.7. **IR Bit "H" HMin Register (BHHmin: 0x003C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bhhmin				bhhmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x0C							

Register Field	Bit	Description
bhhmin	[11:0]	IR Bit H H Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.8. **IR Bit "H" H Max Register (BHHmax: 0x003E)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bhhmax				bhhmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x20							

Register Field	Bit	Description
bhhmax	[11:0]	IR Bit H H Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.9. **IR Bit "H" LMin Register (BHLmin: 0x0040)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bhlmin				bhlmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x0C							

Register Field	Bit	Description
bhlmin	[11:0]	IR Bit H L Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.10. **IR Bit “H” LMax Register (BHLmax: 0x0042)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bhlmax				bhlmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x20							

Register Field	Bit	Description
bhlmax	[11:0]	IR Bit H L Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.11. **IR Bit “L” HMin Register (BLHmin: 0x0044)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				blhmin				blhmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x37							

Register Field	Bit	Description
blhmin	[11:0]	IR Bit L H Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.12. **IR Bit “L” HMax Register (BLHmax: 0x0046)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				blhmax				blhmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x4B							

Register Field	Bit	Description
blhmax	[11:0]	IR Bit L H Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.13. IR Bit “L” LMin Register (BLLmin: 0x0048)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bllmin				bllmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x0C							

Register Field	Bit	Description
bllmin	[11:0]	IR Bit L L Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.14. IR Bit “L” LMax Register (BLLmax: 0x004A)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				bllmax				bllmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x20							

Register Field	Bit	Description
bllmax	[11:0]	IR Bit L L Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.15. IR “END” HMin Register (EndHmin: 0x004C)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				endhmin				endhmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x0C							

Register Field	Bit	Description
endhmin	[11:0]	IR “END” H Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.16. IR "END" HMax Register (EndHmax: 0x004E)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				endhmax				endhmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x20							

Register Field	Bit	Description
endhmax	[11:0]	IR "END" H Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.17. IR Repeat Code LMin Register (RCLmin: 0x0050)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				rclmin				rclmin							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x4C							

Register Field	Bit	Description
rclmin	[11:0]	IR Repeat Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.18. IR Repeat Code LMax Register (RCLmax: 0x0052)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				rclmax				rclmax							
Type	RO				R/W				R/W							
Default	0x0				0x0				0x60							

Register Field	Bit	Description
rclmax	[11:0]	IR Repeat Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count …

5.4.19. **IR Control Register (IRCtl: 0x0058)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ir_ccode								Reserved						ir_ccodem	Reserved
Type	R/W								RO						R/W	RO
Default	0x00								0	0	0	0	0	0	0	0

Register Field	Bit	Description
ir_ccode	[15:8]	IR Custom code TC358870XBG collects ir data only if the receive “custom code” match this ir_ccode (ir_ccodem=1'b0)
ir_ccodem	1	IR Custom Code Mask 0: Match 1: No Match (mask)

5.4.20. **IR Data Register (IRData: 0x005A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ir_rccode								ir_rdata							
Type	RO								RO							
Default	0x0								0x0							

Register Field	Bit	Description
ir_rccode	[15:8]	IR Receive custom code data
ir_rdata	[7:0]	IR Receive data

5.4.21. **IR CONTROL REGISTER (IR_CONTROL: 0x7082)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														IRInv	Reserved
Type	RO														R/W	RO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
IRInv	1	IRInv (Option to use inverted or non-inverted polarity) 1: Invert IR Polarity

Note: This register shares the address with the I2S Control Register

5.5. DSI-TX0 Registers

When reserved bits are read, the value is 0. Writing Reserved bits are invalid and no affects.

5.5.1. **DSI-TX0 Control Registers**

5.5.1.1. DSITX_CLKEN (0x0108)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															DSITX En
Type	-															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DSITXEn	0	DSITX Enable 0: The clocks are gated and not provided inside of DSITX except for [DSITX_CLKEN (0x0108)]register setting for power saving. 1: The clocks are not clock gated.

5.5.1.2. PPI_CLKSEL (0x010C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				PPISYSDTClkSel1	PPISYSDTClkSel0	PPISYSCLClkSel1	PPISYSCLClkSel0	Reserved							PPIHsTxClkEn
Type	-				R/W	R/W	R/W	R/W	-							R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
PPISYSDTClkSel [1:0]	[11:10]	Clock Selection SYSDTClk clock for PPI block. PPI High Speed Data Receive Interface for CDSI shall use the same selected clock. Change these bits while PPIHsTxClkEn is Low. 00: HSCKBY8 clock is set for HSTX clock in D-PHY PPI block. 01: HSCKBY4 clock is set for HSTX clock in D-PHY PPI block. 10: HSCKBY2 clock is set for HSTX clock in D-PHY PPI block. 11: Reserved. Do not set.
PPISYSCLClkSel [1:0]	[9:8]	Clock Selection SYSCLClk clock for PPI block. PPI High Speed Data Receive Interface for CDSI shall use the same selected clock. Change these bits while PPIHsTxClkEn is Low. 00: HSCKBY8 clock is set for HSTX clock in D-PHY PPI block. 01: HSCKBY4 clock is set for HSTX clock in D-PHY PPI block. 10: HSCKBY2 clock is set for HSTX clock in D-PHY PPI block. 11: Reserved. Do not set.
PPIHsTxClkEn	0	Clock Enable signal to provide the selected HSTX clock to D-PHY PPI block. 0: Clock is gated and clock is not provided. 1: Clock is not gated and clock is provided.

5.5.1.3. MODE_CONFIG (0x0110)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											IndMode	Reserved	HSYNC_POL_SW	VSYNC_POL_SW	Reserved
Type	-											R/W	-	R/W	R/W	-
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
IndMode	4	To select LP or HS transmission mode for DSI command) 0: DSI command transmitted in HS mode. 1: DSI command transmitted in LP mode.
HSYNC_POL_SW	2	PIC_SYN_LINE_A Polarity Switch 0: HSync Active High Polarity. Must be progrrammed to 1 for DSI mode. 1: HSync Active Low Polarity.
VSYNC_POL_SW	1	PIC_COM_FRAME_A Polarity Switch 0: VSync Active High Polarity. Must be programmed to 1 for DSI mode. 1: VSync Active Low Polarity.

5.5.1.4. LANE_ENABLE (0x0118)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											CLaneEn	Reserved	DTLaneEn2	DTLaneEn1	DTLaneEn0
Type	-											R/W	-	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CLaneEn	4	Clock Lane Enable In order to transmit HSTX data, Clock Lane shall be enabled. 0: Lane operation disabled (default). Line is allowed at high impedance. 1: Lane operation enabled
DTLaneEn[2:0]	[2:0]	Data Lane Enable In order to transmit data, at least Data Lane 0 shall be enabled. 000: All data lane is disabled. 001: Data Lane 0 is enabled. 010: Data Lane 0 and 1 are enabled. 011: Data Lane 0, 1 and 2 are enabled. 100: Data Lane 0, 1, 2 and 3 are enabled. 101: Reserved. Do not set. 110: Reserved. Do not set. 111: Reserved. Do not set.

5.5.1.5. DSITX_START (0x011C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															DSITX Start
Type	-															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DSITXStart	0	This bit is used to enable DSITX for data transmission. This bit is output to STARTPPI signal. Application shall configure this bit only when DSITX is in idle mode. DSITX should discard transmit or received data if this bit is set to zero. 0: DSITX is stopped. 1: DSITX is started for data transmission after line initialization is done.

5.5.1.6. LINE_INIT_COUNT (0x0120)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LINEINITCNT15	LINEINITCNT14	LINEINITCNT13	LINEINITCNT12	LINEINITCNT11	LINEINITCNT10	LINEINITCNT9	LINEINITCNT8	LINEINITCNT7	LINEINITCNT6	LINEINITCNT5	LINEINITCNT4	LINEINITCNT3	LINEINITCNT2	LINEINITCNT1	LINEINITCNT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
LINEINITCNT[15:0]	[15:0]	Line Initialization Wait Counter. This counter is used for line initialization. The value is set in LINEINITCOUNT signal. MIPI specification requires that slave device needs to observe LP-11 for 100 μs and ignore the received data before the period at initialization time. The count value depends on SYSINITClk and the value needs to be set to achieve more than 100 μs. The counter starts after the PPIStart bit of the DSITX_START register is set. The Master device needs to output LP-11 for 100 μs in order for the slave device to observe LP-11 for the period.

5.5.1.7. HSTX_TO_COUNT (0x0124)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HSToCnt31	HSToCnt30	HSToCnt29	HSToCnt28	HSToCnt27	HSToCnt26	HSToCnt25	HSToCnt24	HSToCnt23	HSToCnt22	HSToCnt21	HSToCnt20	HSToCnt19	HSToCnt18	HSToCnt17	HSToCnt16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSToCnt15	HSToCnt14	HSToCnt13	HSToCnt12	HSToCnt11	HSToCnt10	HSToCnt9	HSToCnt8	HSToCnt7	HSToCnt6	HSToCnt5	HSToCnt4	HSToCnt3	HSToCnt2	HSToCnt1	HSToCnt0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
HSToCnt[31:0]	[31:0]	Time Out counter for High Speed Transmission. This counter is counted by TxByteClkHs. Set the counter before PPIStart. This timer is used to monitor the TX on the length of HS transmission

5.5.1.8. FUNC_ENABLE (0x0128)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved									InitInt_En	AppSideErrInt_En	DsiPrToInt_En	DsirxErrInt_En	DsiLptxInt_En	DsirxTrigInt_En	DSIRxStateInt_En
Type	-									R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	PRESP_TO_En	Reserved			HSTX_TO_En	IndTO_En	IndModeSel	Reserved							VHDelayEn
Type	-	R/W	R/W			R/W	R/W	R/W	-							R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
InitInt_En	22	This bit selects enable or disable of INIT interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
AppSideErrInt_En	21	Application Side Error Interrupt Enable. This bit selects enable or disable of Application Error Interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
DsiPrToInt_En	20	DSI PRTO Interrupt Enable. This bit selects enable or disable of DSI PRTO Interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
DsirxErrInt_En	19	DSI_RXERR Interrupt Enable This bit selects enable or disable of DSI_RXERR Interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
DsiLptxInt_En	18	DSI LPTX Interrupt Enable This bit selects enable or disable of DSI_LPTX Interrupt. This bit should be set to 1 while transmitting LPTX Data through LPTX register interface. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
DsirxTrigInt_En	17	DSI_RXTRIG Interrupt Enable This bit selects enable or disable of DSI_RXTRIG Interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
DSIRxStateInt_En	16	DSI_RX_STATE Interrupt Enable This bit selects enable or disable of DSI_RX_STATE Interrupt. When related interrupt mask bit is changed dynamically during working, the mask bit shall be changed while this Enable bit is set to low.
PRESP_TO_En	14	0: Disable the PRESP_TO timer. 1: Enable the PRESP_TO timer.
HSTX_TO_En	10	0: Disables the HSTX_TO timer 1: Enables the HSTX_TO timer
IndTO_En	9	Sync Independent Time Out Enable 0: Disable the IND_TO timer 1: Enable the IND_TO timer
IndModeSel	8	To select between input port or register bit) 0: “IND_LPMODE_A” input port will be used to select between LP or HS mode transmission. 1: “IndMode” register bit will be used to select between LP or HS mode transmission.

Register Field	Bit	Description
VHDelayEn	0	Enable the APF_VDELAYCNT (0x0170) and APF_HDELAYCNT (0x0174) registers Vertical and Horizontal DELAY Counts can be selected from APF_VDELAYCNT (0x0170) and APF_HDELAYCNT (0x0174) registers or from input ports. 0: VHDELAY Counts are from port inputs. 1: VHDELAY Counts are from registers. Must be programmed to 1 for DSI.

5.5.1.9. DSI_LPTX_MODE (0x012C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPTXTRANSMITLINENUM12	LPTXTRANSMITLINENUM11	LPTXTRANSMITLINENUM10	LPTXTRANSMITLINENUM9	LPTXTRANSMITLINENUM8	LPTXTRANSMITLINENUM7	LPTXTRANSMITLINENUM6	LPTXTRANSMITLINENUM5	LPTXTRANSMITLINENUM4	LPTXTRANSMITLINENUM3	LPTXTRANSMITLINENUM2	LPTXTRANSMITLINENUM1	LPTXTRANSMITLINENUM0	LPTX_time1	LPTX_time0	FromReg
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LPTXTRANSMITLINENUM[12:0]	[15:3]	Line number for schedule the LP packet to be sent through register interface
LPTX_time [1:0]	[2:1]	period time to transmit LPTX packet which generated by register. 00: LPTX packet will be transmitted during VFP (Vertical Front Porch). 01: LPTX packet will be transmitted during the line number equals to LPTXTRANSMITLINENUM [12:0] input. 10: LPTX packet can be transmitted as soon as possible at any non-image period. 11: Reserved.
FromReg	0	From Register This bit indicate if the LPTX command can be from Register or Input 0: LPTX command is from Input. 1: LPTX command is from DSI LPTX Registers.

5.5.1.10. DSI_PRESP_LPW_COUNT (0x013C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRESPLPWCnt31	PRESPLPWCnt30	PRESPLPWCnt29	PRESPLPWCnt28	PRESPLPWCnt27	PRESPLPWCnt26	PRESPLPWCnt25	PRESPLPWCnt24	PRESPLPWCnt23	PRESPLPWCnt22	PRESPLPWCnt21	PRESPLPWCnt20	PRESPLPWCnt19	PRESPLPWCnt18	PRESPLPWCnt17	PRESPLPWCnt16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRESPLPWCnt15	PRESPLPWCnt14	PRESPLPWCnt13	PRESPLPWCnt12	PRESPLPWCnt11	PRESPLPWCnt10	PRESPLPWCnt9	PRESPLPWCnt8	PRESPLPWCnt7	PRESPLPWCnt6	PRESPLPWCnt5	PRESPLPWCnt4	PRESPLPWCnt3	PRESPLPWCnt2	PRESPLPWCnt1	PRESPLPWCnt0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
PRESPLPWCnt[31:0]	[31:0]	Counter value for Peripheral Response time out for LPDT write request. This counter is counted by REFCLK. Set the counter before DSITX starts.

5.5.1.11. DSI_PRESP_HSR_COUNT (0x0140)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRESPHSRCnt31	PRESPHSRCnt30	PRESPHSRCnt29	PRESPHSRCnt28	PRESPHSRCnt27	PRESPHSRCnt26	PRESPHSRCnt25	PRESPHSRCnt24	PRESPHSRCnt23	PRESPHSRCnt22	PRESPHSRCnt21	PRESPHSRCnt20	PRESPHSRCnt19	PRESPHSRCnt18	PRESPHSRCnt17	PRESPHSRCnt16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRESPHSRCnt15	PRESPHSRCnt14	PRESPHSRCnt13	PRESPHSRCnt12	PRESPHSRCnt11	PRESPHSRCnt10	PRESPHSRCnt9	PRESPHSRCnt8	PRESPHSRCnt7	PRESPHSRCnt6	PRESPHSRCnt5	PRESPHSRCnt4	PRESPHSRCnt3	PRESPHSRCnt2	PRESPHSRCnt1	PRESPHSRCnt0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
PRESPHSRCnt[31:0]	[31:0]	Counter value for Peripheral Response time out for HS Read request. This counter is counted by REFCLK. Set the counter before DSITX starts.

5.5.1.12. DSI_PRESP_HSW_COUNT (0x0144)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRESPHSWCnt31	PRESPHSWCnt30	PRESPHSWCnt29	PRESPHSWCnt28	PRESPHSWCnt27	PRESPHSWCnt26	PRESPHSWCnt25	PRESPHSWCnt24	PRESPHSWCnt23	PRESPHSWCnt22	PRESPHSWCnt21	PRESPHSWCnt20	PRESPHSWCnt19	PRESPHSWCnt18	PRESPHSWCnt17	PRESPHSWCnt16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PRESPHSWCnt15	PRESPHSWCnt14	PRESPHSWCnt13	PRESPHSWCnt12	PRESPHSWCnt11	PRESPHSWCnt10	PRESPHSWCnt9	PRESPHSWCnt8	PRESPHSWCnt7	PRESPHSWCnt6	PRESPHSWCnt5	PRESPHSWCnt4	PRESPHSWCnt3	PRESPHSWCnt2	PRESPHSWCnt1	PRESPHSWCnt0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
PRESPHSWCnt[31:0]	[31:0]	Counter value for Peripheral Response time out for HS Write request. This counter is counted by REFCLK. Set the counter before DSITX starts.

5.5.1.13. FUNC_MODE (0x0150)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					CLForceTxStopModeEn	CntAutoTxMd	ECCDis	Reserved	CrcDis	HsCkMd	Reserved				EoTpEn
Type	-					R/W	R/W	R/W	-	R/W	R/W	-				R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CLForceTxStopModeEn	10	0: Clock Lanes will not be forced to STOP state when ForceTxStopmode signal is asserted internally. 1: Clock Lanes will be forced to STOP state when ForceTxStoremode signal is asserted internally.
CntAutoTxMd	9	0: When Contention is detected, the mode is automatically changed from LPTX to stop state (LP-11). The Contention Error flag will be generated in this mode. 1: When Contention is detected, the mode is not automatically changed from LPTX to stop state (LP-11). This means the DSITX continues LPTX transmission and ignores contention. The Contention Error flag is generated in this mode.

Register Field	Bit	Description
ECCDis	8	ECC Disable This bit sets operation for when there are multiple-bit ECC errors in the received data. If multiple-bit ECC errors are detected in received packet, the ECC Error multi bit (bit 9) bit of the DSI_RXERR register is asserted to “1” regardless of this bit's setting. In the case of ECC single-bit errors, the setting of this bit has no effect on the operation. Single-bit errors can be corrected, so the corrected data can be stored in the Receive FIFO regardless of this bit's setting. At this time, the ECC Error single bit (bit 8) bit of the DSI_RXERR is asserted to “1” 0: If there are multiple-bit ECC errors in the received data, subsequent processes including the fetching of data from the peripheral interface are terminated and wait for the LP Stop state. Loading to the Receive FIFO of the corresponding packets is not performed. 1: Even if multiple-bit ECC errors are detected in the received data, subsequent processes including the fetching of data from the peripheral interface continue. Either the packet in which multiple bit ECC errors were detected is loaded into the Receive FIFO or the corresponding package waits for a valid Data Type. If the Data Type is invalid, the DSI Data Type no recognized (bit 11) bit of the DSI_RXERR register is set to “1” and the packet is discarded. If a valid Data Type is recognized, the packet is stored in the Receive FIFO. In the case of a long packet, processing continues up to the reception of the data payload.
CrcDis	6	CRC Disable checking. Operation for when a CRC error was found in the received data is set. (For long receive packets only) 0: CRC checking of received long packets is performed. If CRC errors exist in the received data, the CRC Error bit (bit 10) of the DSI_RXERR register is asserted to “1”. Transfers to the Receive FIFO for the received data are performed. 1: CRC checking of received long packets is not performed. Even if there are CRC errors in the received data, no notification is made to the DSI_RXERR register. The CRC errors are ignored and transfers to the Receive FIFO for the received data are performed.
HsCkMd	5	HS Clock Mode 0: Operation in discontinuous clock mode. 1: Operation in continuous clock mode.
EoTpEn	0	EoT packet Enable This bit selects if the CDSI generate the EoTp at the end of HS transmission. 0: CDSI does not generate EoTp at the end of HS transmission and also not expects EoTp at the end of HS reception. 1: CDSI generates EoTp at the end of HS transmission.

5.5.1.14. DSIRX_VC_ENABLE (0x0154)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												RXVC3_EN	RXVC2_EN	RXVC1_EN	RXVC0_EN
Type	-												R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
RXVC3_EN	3	Virtual Channel-3 supported in LPRX path
RXVC2_EN	2	Virtual Channel-2 supported in LPRX path
RXVC1_EN	1	Virtual Channel-1 supported in LPRX path
RXVC0_EN	0	Virtual Channel-0 supported in LPRX path

5.5.1.15. IND_TO_COUNT (0x0158)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IND_TOCnt31	IND_TOCnt30	IND_TOCnt29	IND_TOCnt28	IND_TOCnt27	IND_TOCnt26	IND_TOCnt25	IND_TOCnt24	IND_TOCnt23	IND_TOCnt22	IND_TOCnt21	IND_TOCnt20	IND_TOCnt19	IND_TOCnt18	IND_TOCnt17	IND_TOCnt16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IND_TOCnt15	IND_TOCnt14	IND_TOCnt13	IND_TOCnt12	IND_TOCnt11	IND_TOCnt10	IND_TOCnt9	IND_TOCnt8	IND_TOCnt7	IND_TOCnt6	IND_TOCnt5	IND_TOCnt4	IND_TOCnt3	IND_TOCnt2	IND_TOCnt1	IND_TOCnt0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
IND_TOCnt [31:0]	[31:0]	Counter value for Sync Independent Interface at the Host side. This counter is counted by SYSClk. This counter is used to terminate the Sync Independent Interface transaction if the interface does not provide enough data as per WC. The counter will start counting during Independent Interface transaction and IND_DTVALID_A is LOW. It will reset when IND_DTVALID_A is HIGH.

5.5.1.16. INIT_INT_STAT (0x0160)

The following status bits show the unmasked status regardless the interrupt mask.
Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													Auto CalDone	HsTxVRegRdy	LineInitDone
Type	-													R/W1C	R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
AutoCalDone	2	LPRX Auto Calibration Finish. 0: Calibration is not completed. 1: Auto calibration completed.
HsTxVRegRdy	1	Voltage regulator count done signal when PPI_HSTXVREGCNT is counted. 0: Voltage regulator count not done. 1: Voltage regulator count done.
LineInitDone	0	Line Initialization Done. 0: Line is not initialized. 1: Line is initialized.

5.5.1.17. INIT_INT_MASK (0x0164)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													Mask Auto CalDone	Mask_ HsTxV RegRdy	Mask_ LineIni tDone
Type	-													R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MaskAutoCalDone	2	LPRX Auto Calibration Finish. 0: No Mask. 1: Mask.
Mask_HsTxVRegRdy	1	Voltage regulator count done signal when PPI_HSTXVREGCNT is counted. 0: No Mask 1: Mask.
Mask_LineInitDone	0	Line Initialization Done. 0: No Mask 1: Mask.

5.5.2. APF Configuration Registers

5.5.2.1. APF_VDELAYCNT (0x0170)

This register specifies the delay of output VSYNC to that of input VSYNC in DSI mode.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														VdelayCnt [17:16]	
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VdelayCnt[15:0]															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Register Field	Bit	Description
VdelayCnt	[17:0]	Used to program VHDELAY value in case of DSI mode, counted by DSI ByteClk.

5.5.2.2. APF_VC_CONFIG (0x0178)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													VC_VAL1	VC_VAL0	VC_Sel
Type	-													R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
VC_VAL [1:0]	[2:1]	Virtual Channel number configuration for port A.
VC_Sel	0	Virtual Channel selection from input port or register. 0: Virtual Channel value from input port 1: Virtual Channel value from this register bits [2:1]

5.5.2.3. DSITX_MODE (0x017C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								BlankPkt_En	Reserved						DSITXMd
Type	-								R/W	-						R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
BlankPkt_En	7	Enable to transmit HSA, HBP as a long blank packet. In DSI specification, the HSA and HBP can be a long blank packet concatenate with HSS, HSE and video packet in a single HS transmission. The WC of HSA, HBP is from DSI_HSYNC_WIDTH (0x018C) and DSI_HBPR (0x0190) registers, respectively. It is application layer's responsibility to configure these register for CDSI layer to transmit these packet in single HS period. But there is one exception. If application layer schedules LPTX data transmission in video active region when this bit set to 1, DSITX shall transmit LPTX data in HBP period and ignores this bit value. 0: HSA, HBP are in Low Power period. No long blank packet for HSA, HBP. 1: This feature is enabled.
DSITXMd	0	DSI Video Transmit mode 0: Pulse mode. 1: Event mode.

5.5.2.4. DSI_HSYNC_WIDTH (0x018C)

This register specifies the horizontal blank width count in term of byte length used for HSA period in pulse mode. In the pulse mode APF will transmit the blank packet with the WC as defined in this register. Refer to Section 8.11 in [MIPI04].

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HS_W15	HS_W14	HS_W13	HS_W12	HS_W11	HS_W10	HS_W9	HS_W8	HS_W7	HS_W6	HS_W5	HS_W4	HS_W3	HS_W2	HS_W1	HS_W0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Register Field	Bit	Description
HS_W[15:0]	[15:0]	This field gives the word count of the blanking packet that may be transmitted during Horizontal Back Porch period when DSITX_MODE (0x017C).BlankPkt_En = 1. Alternatively, this field gives the period in DSI byte clocks for which DSITX is to transition to LP mode when DSITX_MODE (0x017C).BlankPkt_En = 0.. HS_W [15:0] equal to zero is invalid for pulse mode.

5.5.2.5. DSI_HBPR (0x0190)

This register specifies the Horizontal Back Porch width in term of byte length used for HBP period in pulse mode.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HBP_W15	HBP_W14	HBP_W13	HBP_W12	HBP_W11	HBP_W10	HBP_W9	HBP_W8	HBP_W7	HBP_W6	HBP_W5	HBP_W4	HBP_W3	HBP_W2	HBP_W1	HBP_W0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Register Field	Bit	Description
HBP_W[15:0]	[15:0]	This field gives the word count of the blanking packet that may be transmitted during Horizontal Back Porch period when DSITX_MODE (0x017C).BlankPkt_En = 1. Alternatively, this field gives the period in DSI byte clocks for which DSITX is to transition to LP mode when DSITX_MODE (0x017C).BlankPkt_En = 0.

5.5.3. **RX Event Registers**

5.5.3.1. DSI_RX_STATE_INT_STAT (0x01A0)

The following status bits show the unmasked status regardless the interrupt enable mask.
Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											LPRX_PKT_START	LPRX_PKT_DONE	LPRX_THRESH_HIT	DirectionFall	DirectionRise
Type	-											R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LPRX_PKT_START	4	0: No new packet received or LPRX packet reception not complete 1: Indicates start of LPRX packet.
LPRX_PKT_DONE	3	0: Not end of packet. 1: Indicates end of packet.
LPRX_THRESH_HIT	2	0: Data Less than Threshold Count. 1: Data equal or greater than threshold Count.
DirectionFall	1	Fall edge detection of Direction signal on Data Lane 0 from PPI. 0: No detection. 1: Fall edge detection. This means BTA is done from Peripheral to Host.
DirectionRise	0	Rise edge detection of Direction signal on Data Lane 0 from PPI. 0: No detection. 1: Rise edge detection. This means BTA is done from Host to Peripheral.

5.5.3.2. DSI_RX_STATE_INT_MASK (0x01A4)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											Mask LPRX_PKT_START	Mask LPRX_PKT_DONE	Mask LPRX_THRESH_HIT	MaskDirectionFall	Mask DirectionRise
Type	-											R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Register Field	Bit	Description
MaskLPRX_PKT_START	4	0: No Mask 1: Mask
MaskLPRX_PKT_DONE	3	0: No Mask 1: Mask.
MaskLPRX_THRESH_HIT	2	0: No Mask. 1: Mask.
MaskDirectionFall	1	Fall edge detection of Direction signal on Data Lane 0 from PPI. 0: No Mask. 1: Mask.
MaskDirectionRise	0	Rise edge detection of Direction signal on Data Lane 0 from PPI. 0: No Mask. 1: Mask.

5.5.3.3. DSI_RXTRIG_INT_STAT (0x01A8)

The following status bits show the unmasked status regardless the interrupt enable mask.
Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												L0RxTrigger3	L0RxTrigger2	L0RxTrigger1	L0RxTrigger0
Type	-												R/W1C	R/W1C	R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
L0RxTrigger3	3	Reception of RxTrigger [3] on Data Lane 0. 0: No reception. 1: Reception.
L0RxTrigger2	2	Reception of RxTrigger [2] on Data Lane 0. 0: No reception. 1: Reception.
L0RxTrigger1	1	Reception of RxTrigger [1] on Data Lane 0. 0: No reception. 1: Reception.
L0RxTrigger0	0	Reception of RxTrigger [0] on Data Lane 0. 0: No reception. 1: Reception.

5.5.3.4. DSI_RXTRIG_INT_MASK (0x01AC)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												MaskL0RxTrigger3	MaskL0RxTrigger2	MaskL0RxTrigger1	MaskL0RxTrigger0
Type	-												R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Register Field	Bit	Description
MaskL0RxTrigger3	3	Reception of RxTrigger [3] on Data Lane 0. 0: No Mask. 1: Mask.
MaskL0RxTrigger2	2	Reception of RxTrigger [2] on Data Lane 0. 0: No Mask. 1: Mask.
MaskL0RxTrigger1	1	Reception of RxTrigger [1] on Data Lane 0. 0: No Mask. 1: Mask.
MaskL0RxTrigger0	0	Reception of RxTrigger [0] on Data Lane 0. 0: No Mask. 1: Mask.

5.5.3.5. DSITX_INTERNAL_STAT (0x01B0)

Writing the status bits is invalid and no affect.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						APF_Lptx_Stat	APF_VHIF_Ind_Stat	APF_VHIF_Sync_Stat	PPI_RxEsc_Busy	PPI_Init_Busy	PPI_Byte_Busy	PPI_TxEsc_Busy	PPI_CL_Busy	PPI_DT_Busy	CDSI_Stat
Type	-						R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
APF_Lptx_Stat	9	APF LPTX Internal state 0: All All state in APF LPTX module is idle state at the moment. 1: All state in APF LPTX module is not idle state at the moment.
APF_VHIF_Ind_Stat	8	APF VHIF Ind Internal State. 0: All state in APF VHIF Ind module is idle state at the moment. 1: All state in APF VHIF Ind module is not idle state at the moment.
APF_VHIF_Sync_Stat	7	APF VHIF Sync Internal State. 0: All state in APF VHIF Sync module is idle state at the moment. 1: All state in APF VHIF Sync module is not idle state at the moment.
PPI_RxEsc_Busy	6	PPI is busy in RxByteClkEsc domain. 0: Not busy. 1: Busy.
PPI_Init_Busy	5	PPI is busy in REFCLK domain. 0: Not busy. 1: Busy.
PPI_Byte_Busy	4	PPI is busy in TxByteClkHs domain. 0: Not busy. 1: Busy.
PPI_TxEsc_Busy	3	PPI is busy in TxClkEsc domain. 0: Not busy. 1: Busy.
PPI_CL_Busy	2	PPI is busy in SYSCLClk domain. 0: Not busy. 1: Busy.
PPI_DT_Busy	1	PPI is busy in SYSDTClk domain. 0: Not busy. 1: Busy.
CDSI_Stat	0	CDSI Internal State. 0: All state in CDSI module is idle state at the moment. 1: All state in CDSI module is not idle state at the moment.

5.5.3.6. DSI_ACKERROR (0x01B4)

This register holds the content of Acknowledge packets having a report of the last error received. This register will be cleared when it is read.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AckErr_report15	AckErr_report14	AckErr_report13	AckErr_report12	AckErr_report11	AckErr_report10	AckErr_report9	AckErr_report8	AckErr_report7	AckErr_report6	AckErr_report5	AckErr_report4	AckErr_report3	AckErr_report2	AckErr_report1	AckErr_report0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
AckErr_report[15:0]	[15:0]	The content of the Acknowledge packet with report of the last error received is held. The meaning of these bits are in Table 20 of DSI specification.

5.5.3.7. DSI_RXFIFO (0x01B8)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RXDATA31	RXDATA30	RXDATA29	RXDATA28	RXDATA27	RXDATA26	RXDATA25	RXDATA24	RXDATA23	RXDATA22	RXDATA21	RXDATA20	RXDATA19	RXDATA18	RXDATA17	RXDATA16
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXDATA15	RXDATA14	RXDATA13	RXDATA12	RXDATA11	RXDATA10	RXDATA9	RXDATA8	RXDATA7	RXDATA6	RXDATA5	RXDATA4	RXDATA3	RXDATA2	RXDATA1	RXDATA0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
RXDATA[31:0]	[31:0]	Data received from the peripheral interface via the DSI link is written to a 32 deep Data FIFO. This register is written with the data in the Data FIFO corresponding to the current read pointer. Reads to this register will increment the Data FIFO read pointer.

5.5.3.8. DSI_RX_HEADER (0x01BC)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								RXVC1	RXVC0	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0
Type	-								R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RXWC15	RXWC14	RXWC13	RXWC12	RXWC11	RXWC10	RXWC9	RXWC8	RXWC7	RXWC6	RXWC5	RXWC4	RXWC3	RXWC2	RXWC1	RXWC0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
RXVC[1:0]	[23:22]	Virtual channel Identifier of received packet
RXDT[5:0]	[21:16]	Data Identifier of received packet Data Identifier of the data received from the peripheral interface via the DSI link is written to this register.
RXWC[15:0]	[15:0]	Word count of received packet Word count of the data received from the peripheral interface via the DSI link is written to this register.

5.5.3.9. DSI_LPRX_THRESH_COUNT (0x01C0)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											RX_THRESH_CNT4	RX_THRESH_CNT3	RX_THRESH_CNT2	RX_THRESH_CNT1	RX_THRESH_CNT0
Type	-											R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
RX_THRESH_CNT[4:0]	[4:0]	Threshold value to assert LPRX_THRESH_HIT interrupts. LPRX_THRESH_HIT interrupt is asserted when data in the DSIRX FIFO is greater than or equal to a programmable value in this register.

5.5.3.10. DSI_LPRX_FIFO_LEVEL (0x01C4)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											RX_FIFO_LEVEL4	RX_FIFO_LEVEL3	RX_FIFO_LEVEL2	RX_FIFO_LEVEL1	RX_FIFO_LEVEL0
Type	-											R	R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
RX_FIFO_LEVEL[4:0]	[4:0]	RX_FIFO_LEVEL value indicates number of 32-bit data entries in RX FIFO.

5.5.4. **Error Experience Registers**

5.5.4.1. DSI_PRTO_INT_STAT (0x0208)

The following status bits show the unmasked status regardless the interrupt enable mask.
Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												PrespTo	Reserved	HsTxTo	Reserved
Type	-												R/W1C	-	R/W1C	-
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
PrespTo	3	Peripheral Response time out. 0: No Timeout 1: Timeout
HsTxTo	1	HSTX time out. 0: No Timeout 1: Timeout

5.5.4.2. DSI_PRTO_INT_MASK (0x020C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												MaskPrespTo	Reserved	MaskHsTxTo	Reserved
Type	-												R/W	-	R/W	-
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MaskPrespTo	3	Peripheral response time out.
MaskHsTxTo	1	HSTX time out.

5.5.4.3. APP_SIDE_ERR_INT_STAT (0x0210)

Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						Ind_Wrng_En	Line_Buf_Rd_Wrt_Violation	Reserved	ErrRxFifoOvf	Reserved	SyncBuf_Ovf_Err	IndBuf_Ovf_Err	LineBuf_Ovf_Err	ErrWC	ErrDT
Type	-						R/W1C	R/W1C	-	R/W1C	-	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Ind_Wrng_En	9	Assertion of incorrect IND_EN 0: IND_EN is asserted correctly 1: IND_EN is asserted incorrectly
Line_Buf_Rd_Wrt_Violation	8	Read and Write happens simultaneously from one of the Line Buffers. 0: No Violation 1: Line Buffer Read and Write Violation
ErrRxFifoOvf	6	Rx FIFO Overflow. 0: No Overflow. 1: Overflow.
SyncBuf_Ovf_Err	4	Sync Packet Gen FIFO Overflow 0: No Overflow 1: Overflow
IndBuf_Ovf_Err	3	Sync Independent FIFO Overflow 0: No Overflow 1: Overflow
LineBuf_Ovf_Err	2	Line Buffer FIFO Overflow. 0: No Overflow. 1: Overflow.
ErrWC	1	The WC and data valid input is not matched. Either expected data is shorter or longer than WC. This error bit is used for both VHIF or IND IF. 1: Error. 0: No Error.
ErrDT	0	Error on Data type input. 1: Data type input is not supported. 0: No error.

5.5.4.4. APP_SIDE_ERR_INT_MASK (0x0214)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						Mask_Ind_Wrng_Err	Mask_Line_Buf_Rd_Wrt_Violation	Reserved	Mask_ErrRxFifoOvf	Reserved	Mask_SyncBuf_Ovf_Err	Mask_IndBuf_Ovf_Err	MaskLineBuf_Ovf_Err	MaskErrWC	MaskErrDT
Type	-						R/W	R/W	-	R/W	-	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Register Field	Bit	Description
Mask_Ind_Wrng_Err	9	Sync Independing incorrect assertion of IND_EN 1: Mask error on incorrect assertion of IND_EN. 0: No Mask.
Mask_Line_Buf_Rd_Wrt_Violation	8	Line Buffer Read/Write Violation 1: Mask error on Violation. 0: No Mask.
Mask_ ErrRxFifoOvf	6	Rx FIFO Overflow 1: Mask error on RX FIFO Overflow. 0: No Mask.
Mask_SyncBuf_Ovf_Err	4	Sync Packet Gen FIFO Overflow 1: Mask error on Sync Packet Gen FIFO Overflow. 0: No Mask.
Mask_IndBuf_Ovf_Err	3	Sync Independent FIFO Overflow 1: Mask error on Sync Independent FIFO Overflow. 0: No Mask.
MaskLineBuf_Ovf_Err	2	Line Buffer Overflow. 1: Mask error on Line Buffer Overflow. 0: No mask.
MaskErrWC	1	1: Mask error on WC. 0: No mask.
MaskErrDT	0	Mask Error on Data type. 1: Mask error on Data type input. 0: No mask.

5.5.4.5. DSI_RX_ERR_INT_STAT (0x0218)

Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		Err_report13	Err_report12	Err_report11	Err_report10	Err_report9	Err_report8	Reserved	Err_report6	Reserved	Err_report4	Err_report3	Reserved		
Type	-		R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	-	R/W1C	-	R/W1C	R/W1C	-		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Err_report13	13	Invalid Data Length
Err_report12	12	DSI VC ID Invalid
Err_report11	11	DSI Data Type not recognized.
Err_report10	10	CRC Error (Long packet only).
Err_report9	9	ECC Error: Multiple bit.
Err_report8	8	ECC Error: Single-bit
Err_report6	6	False Control Error
Err_report4	4	Low Power Transmit Sync Error.
Err_report3	3	Escape Mode Entry command error

5.5.4.6. DSI_RX_ERR_INT_MASK (0x021C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		MaskErr_report13	MaskErr_report12	MaskErr_report11	MaskErr_report10	MaskErr_report9	MaskErr_report8	MaskErr_report7	MaskErr_report6	Reserved	MaskErr_report4	MaskErr_report3	Reserved		
Type	-		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	-		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MaskErr_report13	13	Invalid Data Length Mask 1: Mask error 0: No mask
MaskErr_report12	12	DSI VC Invalid Mask 1: Mask error 0: No mask
MaskErr_report11	11	DSI Data Type recognition error Mask 1: Mask error 0: No mask
MaskErr_report10	10	CRC Error (Long packet only) Mask 1: Mask error 0: No mask
MaskErr_report9	9	ECC Error: Multiple bit Mask 1: Mask error 0: No mask
MaskErr_report8	8	ECC Error: Single-bit Mask 1: Mask error 0: No mask
MaskErr_report7	7	This bit must be always set to “1”
MaskErr_report6	6	Faulty Control Error Mask 1: Mask error 0: No mask
MaskErr_report4	4	LP transfer Sync Error Mask 1: Mask error 0: No mask
MaskErr_report3	3	Escape Mode Entry command error Mask 1: Mask error 0: No mask

5.5.5. **DSI LPTX Registers**

5.5.5.1. DSI_LPTX_INT_STAT (0x0220)

The following status bits show the unmasked status regardless the interrupt enable mask.
Writing 1 to the status bits clears the bit to 0.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						Payload1Done	Payload0Done	Reserved							LpTxDone
Type	-						R/W1C	R/W1C	-							R/W1C
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Payload1Done	9	LP Transmit Complete of Payload1. 0: LP data which is stored in [DSI_LPTX_PAYLOAD1 (0x0238)] is not completed yet. 1: LP data which is stored in [DSI_LPTX_PAYLOAD1 (0x0238)] is completed.
Payload0Done	8	LP Transmit Complete of Payload0. 0: LP data which is stored in [DSI_LPTX_PAYLOAD0 (0x0234)] is not completed yet. 1: LP data which is stored in [DSI_LPTX_PAYLOAD0 (0x0234)] is completed.
LpTxDone	0	LP Packet Transmit is completed. 0: LP Transmit is not completed yet. 1: LP Transmit is completed.

5.5.5.2. DSI_LPTX_INT_MASK (0x0224)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						MaskPayload1Done	MaskPayload0Done	Reserved							MaskLpTxDone
Type	-						R/W	R/W	-							R/W
Default	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1

Register Field	Bit	Description
MaskPayload1Done	9	LP Transmit Complete of Payload1. 0: No Mask. 1: Mask.
MaskPayload0Done	8	LP Transmit Complete of Payload0. 0: No Mask. 1: Mask.
MaskLpTxDone	0	LP Packet Transmit is completed. 0: No Mask. 1: Mask.

5.5.5.3. DSI_LPTX_REQ (0x0228)

If the [DIS_LPTX_MODE] bit [0] is '1' then LPTX Command can be sent from registers in register 0x022C, 0x0230, 0x0234 and0x0238.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															LpTxReq
Type	-															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LpTxReq	0	LP Transmit Request. Only write is valid,. After setting '1' this bit becomes '0' when LPTXDONE is received. 0: No affect. 1: Transmit data set by.

5.5.5.4. LPTX_TYPE (0x022C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved											LPTX TrigSel4	LPTX TrigSel3	LPTX TrigSel2	LPTX TrigSel1	LPTX TrigSel0
Type	-											R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						RsTrigSel1	RsTrigSel0	LPDT	Target_Lane2	Target_lane1	Target_Lane0	LP_Command2	LP_Command1	LP_Command0	TurnReq
Type	-						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LPTXTrigSel[4:0]	[20:16]	LPTxTrigger encoding for CDSI block "LpTxTrigSel [4:0]" "TxTriggerEsc [3:0] output bit order" 00000 [3] [2] [1] [0] 00001 [3] [2] [0] [1] 00010 [3] [1] [2] [0] 00011 [3] [1] [0] [2] 00100 [3] [0] [2] [1] 00101 [3] [0] [1] [2] 00110 [2] [3] [1] [0] 00111 [2] [3] [0] [1] 01000 [2] [1] [3] [0] 01001 [2] [1] [0] [3] 01010 [2] [0] [3] [1] 01011 [2] [0] [1] [3] 01100 [1] [3] [2] [0] 01101 [1] [3] [0] [2] 01110 [1] [2] [3] [0] 01111 [1] [2] [0] [3] 10000 [1] [0] [3] [2] 10001 [1] [0] [2] [3] 10010 [0] [3] [2] [1] 10011 [0] [3] [1] [2] 10100 [0] [2] [3] [1] 10101 [0] [2] [1] [3] 10110 [0] [1] [3] [2] 10111 [0] [1] [2] [3]
RsTrigSel[1:0]	[9:8]	Reset Trigger Select is used to select which Trigger is for Reset Trigger (This is used in CDSI block) 00: Trigger0 is a Reset Trigger 01: Trigger1 is a Reset Trigger 10: Trigger2 is a Reset Trigger 11: Trigger3 is a Reset Trigger
LPDT	7	Low power Data Transmission. This bit is used to indicate low power long/short packet data transmission through LPTX register interface. When TurnReq is High, this field is ignored. The command to disabled lanes is ignored.

Register Field	Bit	Description
Target_Lane[2:0]	[6:4]	LP_Command for Enter /Exit ULPS is executed to the following target lanes. When TurnReq is High, this field is ignored. The command to disabled lanes are ignored. 000: Clock Lane 001: Data Lane 0 010: Data Lane 1 011: Data Lane 2 100: Data Lane 3 101: Reserved 110: ALL enabled Data Lanes 111: ALL enabled Lanes
LP_Command[2:0]	[3:1]	Encoded Low Power Command Request. When TurnReq is High, this field is ignored. The command to disabled lanes is ignored. 000: Reserved 001: Enter ULPS 010: Exit ULPS 011: Reserved 100: Transmit Trigger0 101: Transmit Trigger1 110: Transmit Trigger2 111: Transmit Trigger3
TurnReq	0	BTA Turn Request. 0: No affect. 1: BTA Turn Request signal is asserted to D-PHY PPI.

5.5.5.5. DSI_LPTX_PKT_HDR (0x0230)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								WC1 Data7	WC1 Data6	WC1 Data5	WC1 Data4	WC1 Data3	WC1 Data2	WC1 Data1	WC1 Data0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WC0 Data 7	WC0 Data6	WC0 Data5	WC0 Data4	WC0 Data3	WC0 Data2	WC0 Data1	WC0 Data0	VCID 1	VCID 0	DataType5	DataType4	DataType3	DataType2	DataType1	DataType0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
WC1Data[7:0]	[23:16]	Word Count 1 or Data 1. The field is the either of WC1 for long packet, or Data 1 for short packet.
WC0Data[7:0]	[15:8]	Word Count 0 or Data 0. The field is the either of WC0 for long packet, or Data 0 for short packet.
VCID[1:0]	[7:6]	Virtual Channel ID.
DataType[5:0]	[5:0]	Data Type.

Note: WC[15:0] = 0 or LPTX Long packet with WC=0 is not supported through LPTX register interface.

5.5.5.6. DSI_LPTX_PAYLOAD0 (0x0234)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PYLD0[31:16]															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PYLD0 [15:0]															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Payload data up to 8 bytes can be configured by0x0234 and 0x0238. If 9 bytes or more payload data has to be configured, it must be controlled with 0x0220. Payload1Done, Payload0Done in combination with the application layer. PLD0 is transmitted earlier than PLD1.

Data is transmitted from LSB byte.

Register Field	Bit	Description
PYLD0	[31:0]	Return Long Packet Payload Data 0 Store the payload data to answer the read request long packet. Set the payload data up to the byte size configured in WC region of [DSI_LPTX_PKT_HDR].WC1Data and [DSI_LPTX_PKT_HDR].WC0Data. CRC is added automatically.

5.5.5.7. DSI_LPTX_PAYLOAD1 (0x0238)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PYLD1 [31:16]															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PYLD1 [15:0]															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
PYLD1	[31:0]	Return Long Packet Payload Data 1 Store the payload data to answer the read request long packet. Set the payload data up to the byte size configured in WC0 and WC1 region of [DSI_LPTX_PKT_HDR (0x0230)].

5.5.6. **D-PHY Control Registers**

5.5.6.1. PPI_DPHY_DLYCNTRL (0x0240)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved												CLS_DLYCNTRL3	CLS_DLYCNTRL2	CLS_DLYCNTRL1	CLS_DLYCNTRL0
Type	-												R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	D3S_DLYCNTRL3	D3S_DLYCNTRL2	D3S_DLYCNTRL1	D3S_DLYCNTRL0	D2S_DLYCNTRL3	D2S_DLYCNTRL2	D2S_DLYCNTRL1	D2S_DLYCNTRL0	D1S_DLYCNTRL3	D1S_DLYCNTRL2	D1S_DLYCNTRL1	D1S_DLYCNTRL0	D0S_DLYCNTRL3	D0S_DLYCNTRL2	D0S_DLYCNTRL1	D0S_DLYCNTRL0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CLS_DLYCNTRL [3:0]	[19:16]	Tuning of transmit window position. The HS clock output can be delayed according to the setting. The recommended value is implementation specific.
D3S_DLYCNTRL [3:0]	[15:12]	Tuning of transmit window position. The HS data lane 3 output can be delayed according to the setting. The recommended value is implementation specific.
D2S_DLYCNTRL [3:0]	[11:8]	Tuning of transmit window position. The HS data lane 2 output can be delayed according to the setting. The recommended value is implementation specific.
D1S_DLYCNTRL [3:0]	[7:4]	Tuning of transmit window position. The HS data lane 1 output can be delayed according to the setting. The recommended value is implementation specific.
D0S_DLYCNTRL [3:0]	[3:0]	Tuning of transmit window position. The HS data lane 0 output can be delayed according to the setting. The recommended value is implementation specific.

5.5.6.2. PPI_DPHY_LPRX_THSLD (0x0244)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														D0S_CUTRSEL	D0S_LPRXVTHLOW
Type	-														R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Register Field	Bit	Description
D0S_CUTRSEL	1	LPRXVTHLOW CUTR value select for Data Lane 0. 1: LPRXVTHLOW value is set by CUTR cell. 0: LPRXVTHLOW value is set by D0S_LPRXVTHLOW.
D0S_LPRXVTHLOW	0	LPRX input threshold select for Data Lane 0. 1: LPRX input threshold is low. 0: LPRX input threshold is high.

5.5.6.3. PPI_DPHY_LPRXCALCNTRL (0x0248)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								AutoCalCnt7	AutoCalCnt6	AutoCalCnt5	AutoCalCnt4	AutoCalCnt3	AutoCalCnt2	AutoCalCnt1	AutoCalCnt0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									LPRXCALTRIM2	LPRXCALTRIM1	LPRXCALTRIM0	Reserved			
Type	-									R/W	R/W	R/W	-			
Default	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Register Field	Bit	Description
AutoCalCnt [7:0]	[23:16]	Auto Calibration Counter. The counter is counted by REFCLK. The counter value shall generate the time be more than 500ns.
LPRXCALTRIM [2:0]	[6:4]	Calibration Trimmer.

5.5.6.4. PPI_DPHY_LPRXAUTOCALST (0x024C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													LPRXCALRES	LPRXCALEN	AutoCalStrt
Type	-													R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LPRXCALRES	2	LPRX Calibration Reset. In order to reset auto calibration, set 1, and keep 1 for 500ns or more during LPRXCALEN = 0. When auto calibration function is used, keep this bit to 0. 0: Not Reset 1: Reset calibration.
LPRXCALEN	1	LPRX Calibration Enable. In order to execute calibration, set 1, and keep 1 for 500ns or more during LPRXCALRES = 0. When auto calibration function is used, keep this bit to 0. 0: Calibration Switch OFF 1: Calibration Switch ON
AutoCalStrt	0	LPRX Auto Calibration Start. When this bit is set to 1, LPRXCALRES and LPRXCALEN are ignored until the end of auto calibration. 0: Calibration is not started. 1: Start auto calibration. When this bit is set to 1, the read value is 1 until auto calibration is finished. When autocalibration is finished, the bit is cleared to 0.

5.5.6.5. PPI_DPHY_MON (0x0250)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														D0S_LPCDENMON	D0S_LPTXHIZMON
Type	-														R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CUTR_LPRXVTHLOW
Type	-															R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
D0S_LPCDENMON	17	LPCDEN signal for Data Lane 0 is monitored by this bit. The signal is synchronized to REFCLK.
D0S_LPTXHIZMON	16	LPTXHIZ signal for Data Lane 0 is monitored by this bit. The signal is synchronized to REFCLK.
CUTR_LPRXVTHLOW	0	CUTR LPRXVTHLOW Monitor This bit monitors ZEMIPICUTR calibration value. This signal from PHY is synchronized by REFCLK.

5.5.6.6. PPI_DPHY_LPTXTIMECNT (0x0254)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				LPTX TIME CNT11	LPTX TIME CNT10	LPTX TIME CNT9	LPTX TIME CNT8	LPTX TIME CNT7	LPTX TIME CNT6	LPTX TIME CNT5	LPTX TIME CNT4	LPTX TIME CNT3	LPTX TIME CNT2	LPTXT IMECNT1	LPTX TIME CNT0
Type	-				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
LPTXTIMECNT[11:0]	[11:0]	TLPX Period counter. The counter generates a timing signal for the period of TLPX. This value is set to LPTXTIMECNT signal. $T_{LPX\ period}$ = (1 + LPTXTIMECNT)* SYSDTClk for data Lane $T_{LPX\ period}$ = (1 + LPTXTIMECNT)* SYSCLClk for clock Lane

NOTE:

The minimum value for LPTXTIMECNT shall be two.

The time for (LPTXTIMECNT + 1) * (SYSDTClk period) shall be more than 50ns.

The time for (LPTXTIMECNT + 1) * (SYSCLClk period) shall be more than 50ns.

It is preferred SYSCLClk = SYSDTClk to assure TLPX is same for both clock and data lanes.

5.5.6.7. PPI_DPHY_TCLK_HEADERCNT (0x0258)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								TCLK_PREZEROCNT7	TCLK_PREZEROCNT6	TCLK_PREZEROCNT5	TCLK_PREZEROCNT4	TCLK_PREZEROCNT3	TCLK_PREZEROCNT2	TCLK_PREZEROCNT1	TCLK_PREZEROCNT0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		TCLK_PreCnt5	TCLK_PreCnt4	TCLK_PreCnt3	TCLK_PreCnt2	TCLK_PreCnt1	TCLK_PreCnt0	Reserved	TCLK_PrepareCnt6	TCLK_PrepareCnt5	TCLK_PrepareCnt4	TCLK_PrepareCnt3	TCLK_PrepareCnt2	TCLK_PrepareCnt1	TCLK_PrepareCnt0
Type	-		R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TCLK_PREZEROCNT [7:0]	[23:16]	This counter is used for TCLK-ZERO parameter in Clock Lane. This counter is counted by SYSCLClk. Set this register to satisfy the minimum of 300ns of (TCLK-ZERO + TCLK-PREPARE).
TCLK_PreCnt [5:0]	[13:8]	This counter is counted by SYSDTClk
TCLK_PrepareCnt [6:0]	[6:0]	This counter is used for TCLK_PREPARE parameter. This counter is counted by SYSCLClk. Set this register to satisfy the TCLK-PREPARE timing parameter in MIPI D-PHY specification, which is minimum 38ns and maximum 95ns.

5.5.6.8. PPI_DPHY_TCLK_TRAILCNT (0x025C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved					TCLK_ExitCnt10	TCLK_ExitCnt9	TCLK_ExitCnt8	TCLK_ExitCnt7	TCLK_ExitCnt6	TCLK_ExitCnt5	TCLK_ExitCnt4	TCLK_ExitCnt3	TCLK_ExitCnt2	TCLK_ExitCnt1	TCLK_ExitCnt0
Type	-					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								TCLK_TrailCnt7	TCLK_TrailCnt6	TCLK_TrailCnt5	TCLK_TrailCnt4	TCLK_TrailCnt3	TCLK_TrailCnt2	TCLK_TrailCnt1	TCLK_TrailCnt0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TCLK_ExitCnt [10:0]	[26:16]	TCLK_ExitCnt [10:0]
TCLK_TrailCnt [7:0]	[7:0]	This counter is used for TCLK_TRAIL parameter. This counter is counted by SYSCLClk. Set this register to satisfy the minimum of 60ns.

5.5.6.9. PPI_DPHY_THS_HEADERCNT (0x0260)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								THS_PREZERO CNT7	THS_PREZERO CNT6	THS_PREZERO CNT5	THS_PREZERO CNT4	THS_PREZERO CNT3	THS_PREZERO CNT2	THS_PREZERO CNT1	THS_PREZERO CNT0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									THS_PrepareCnt6	THS_PrepareCnt5	THS_PrepareCnt4	THS_PrepareCnt3	THS_PrepareCnt2	THS_PrepareCnt1	THS_PrepareCnt0
Type	-									R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
THS_PREZEROCNT [7:0]	[23:16]	This counter is used for THS-ZERO parameter in DataLane. This counter is counted by SYSDTClk. Set this register to satisfy the minimum of 145ns + 10*UI of (THS-ZERO + THS-PREPARE).
THS_PrepareCnt [6:0]	[6:0]	This counter is used for THS_PREPARE parameter. This counter is counted by SYSDTClk. Set this register to satisfy the THS-PREPARE timing parameter in MIPI D-PHY specification, which is minimum 40ns+4*UI and maximum 85ns+6*UI.

5.5.6.10. PPI_DPHY_TWAKEUPCNT (0x0264)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TWAKEUP_Cnt															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TWAKEUP_Cnt	[15:0]	This counter is used to exit ULPS State. TWAKEUP = TWAKEUP_Cnt * TLPX period.

5.5.6.11. PPI_DPHY_TCLK_POSTCNT (0x0268)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					TCLK_PostCnt10	TCLK_PostCnt9	TCLK_PostCnt8	TCLK_PostCnt7	TCLK_PostCnt6	TCLK_PostCnt5	TCLK_PostCnt4	TCLK_PostCnt3	TCLK_PostCnt2	TCLK_PostCnt1	TCLK_PostCnt0
Type	-					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TCLK_PostCnt[10:0]	[10:0]	This counter is used for TCLK-POSTparameter in Clock Lane. This counter is counted by SYSDTClk. Set the value greater than (60ns +52*UI).

5.5.6.12. PPI_DPHY_THSTRAILCNT (0x026C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved					THS_ExitCnt10	THS_ExitCnt9	THS_ExitCnt8	THS_ExitCnt7	THS_ExitCnt6	THS_ExitCnt5	THS_ExitCnt4	THS_ExitCnt3	THS_ExitCnt2	THS_ExitCnt1	THS_ExitCnt0
Type	-					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								THS_TrailCnt7	THS_TrailCnt6	THS_TrailCnt5	THS_TrailCnt4	THS_TrailCnt3	THS_TrailCnt2	THS_TrailCnt1	THS_TrailCnt0
Type	-								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
THS_ExitCnt[10:0]	[26:16]	THS_ExitCnt[10:0]
THS_TrailCnt[7:0]	[7:0]	This counter is used for THS_TRAIL parameter. This counter is counted by SYSDTClk.

5.5.6.13. PPI_DPHY_HSTXVREGCNT (0x0270)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HSTXVREGCNT15	HSTXVREGCNT14	HSTXVREGCNT13	HSTXVREGCNT12	HSTXVREGCNT11	HSTXVREGCNT10	HSTXVREGCNT9	HSTXVREGCNT8	HSTXVREGCNT7	HSTXVREGCNT6	HSTXVREGCNT5	HSTXVREGCNT4	HSTXVREGCNT3	HSTXVREGCNT2	HSTXVREGCNT1	HSTXVREGCNT0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
HSTXVREGCNT[15:0]	[15:0]	TX Voltage Regulator setup Wait Counter

5.5.6.14. PPI_DPHY_HSTXVREGEN (0x0274)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											D3M_HSTXVREGEN	D2M_HSTXVREGEN	D1M_HSTXVREGEN	D0M_HSTXVREGEN	CLM_HSTXVREGEN
Type	-											R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
D3M_HSTXVREGEN	4	Voltage regulator enable for HSTX Data Lane 3. 0: Disable. 1: Enable.
D2M_HSTXVREGEN	3	Voltage regulator enable for HSTX Data Lane 2. 0: Disable. 1: Enable.
D1M_HSTXVREGEN	2	Voltage regulator enable for HSTX Data Lane 1. 0: Disable. 1: Enable.
D0M_HSTXVREGEN	1	Voltage regulator enable for HSTX Data Lane 0. 0: Disable. 1: Enable.
CLM_HSTXVREGEN	0	Voltage regulator enable for HSTX Clock Lane. 0: Disable. 1: Enable.

5.5.6.15. PPI_DSI_BTA_COUNT (0x0278)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved					TXTAGOCNT 10	TXTAGOCNT 9	TXTAGOCNT 8	TXTAGOCNT 7	TXTAGOCNT 6	TXTAGOCNT 5	TXTAGOCNT 4	TXTAGOCNT 3	TXTAGOCNT 2	TXTAGOCNT 1	TXTAGOCNT 0
Type	-					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					RXTASURECNT10	RXTASURECNT9	RXTASURECNT8	RXTASURECNT7	RXTASURECNT6	RXTASURECNT5	RXTASURECNT4	RXTASURECNT3	RXTASURECNT2	RXTASURECNT1	RXTASURECNT0
Type	-					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
TXTAGOCNT[10:0]	[26:16]	This value is used to set count up value to set TTA-GO period (LP-00 drive period) when this module release drive right by BTA. The period to drive LP-00 for TTA-GO period is 4*(TXTAGOCNT + 1)* (SYSDTClk cycle). Please set the value to be TTA-GO (= 4*TLPX) period which is MIPI specification.
RXTASURECNT[10:0]	[10:0]	This value is used to set counter value for the period to drive LP00 as TTA-SURE period when drive right is acquired by BTA. The drive period is calculated by (BTA detection period + (RXTASURECNT + (3 or 2))* (SYSDTClk cycle)). Please set the period within TTA-SURE (Min TLPX, Max 2*TLPX), which is MIPI specification.

5.5.6.16. PPI_DPHYTX_ADJUST (0x027C)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Force DPHYADVld	Reserved													FLPTXCURREN1	FLPTXCURREN0
Type	R	-													R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CLS_LPTXCURREN1	CLS_LPTXCURREN0	D3S_LPTXCURREN1	D3S_LPTXCURREN0	D2S_LPTXCURREN1	D2S_LPTXCURREN0	D1S_LPTXCURREN1	D1S_LPTXCURREN0	D0S_LPTXCURREN1	D0S_LPTXCURREN0
Type	-						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0

Register Field	Bit	Description
ForceDPHYADVld	31	Force D-PHY characteristic adjustment value from the input signals. This bit is a monitor bit of FORCE_DPHY_ADVLDEN signal. This bit is static and it is fixed before releasing Reset_N. Writing this bit is invalid. 0: FORCE_DPHY_ADVLDEN signal is Low. 1: FORCE_DPHY_ADVLDEN signal is High.
FLPTXCURREN [1:0]	[17:16]	Force D-PHY LPTX output current (TRLP/TFLP tuning) value from the input signals. The bits are monitor bits of FORCE_LPTX_CURREN signal. Writing the bits is invalid. The bits are used for Data Lane 0 when FORCE_DPHY_ADVLDEN is High.
CLS_LPTXCURREN[1:0]	[9:8]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Clock Lane. The bits are output from CLS_LPTXCURR1EN and CLS_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.
D3S_LPTXCURREN[1:0]	[7:6]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3. The bits are output from D3S_LPTXCURR1EN and D3S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.
D2S_LPTXCURREN[1:0]	[5:4]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2. The bits are output from D2S_LPTXCURR1EN and D2S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Register Field	Bit	Description
D1S_LPTXCURREN[1:0]	[3:2]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1. The bits are output from D1S_LPTXCURR1EN and D1S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.
D0S_LPTXCURREN[1:0]	[1:0]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0. The bits are output from D0S_LPTXCURR1EN and D0S_LPTXCURR0EN when FORCE_DPHY_ADVLDEN is Low. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current When value is changed from 10 (default) to 00, rise/fall time is longer. When '11' is set, rise/fall time is shorter.

Note:

1. FORCE_DPHY_ADVLDEN and FORCE_LPTX_CURREN – Should be driven to 0 or 1 before Reset_N release, otherwise bit [31] & bits [17:16] will appear as 'Z' in simulation.

5.5.6.17. PPI_DPHY_POWERCNTRL (0x0284)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													EN_ZEMIPIV12	V12PEN	V12EN
Type	-													R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	Selectable	Selectable	Selectable

Register Field	Bit	Description
EN_ZEMIPIV12	2	Control signal of EN of ZEMIPIV12 power cell. 0: V12 power is turned off. 1: V12 power is turned on.
V12PEN	1	Control signal of V12PEN of ZEMIPIPLL. 0: V12 power is turned off. 1: V12 power is turned on.
V12EN	0	Control signal of V12EN of ZEMIPI. 0: V12 power is turned off. 1: V12 power is turned on.

5.5.6.18. PPI_DPHY_CAP (0x0288)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CLS_CAP1	CLS_CAP0	D3S_CAP1	D3S_CAP0	D2S_CAP1	D2S_CAP0	D1S_CAP1	D1S_CAP0	D0S_CAP1	D0S_CAP0
Type	-						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0

Register Field	Bit	Description
CLS_CAP [1:0]	[9:8]	Select output capacitors for Clock Lane.
D3S_CAP [1:0]	[7:6]	Select output capacitors for Data Lane 3.
D2S_CAP [1:0]	[5:4]	Select output capacitors for Data Lane 2.
D1S_CAP [1:0]	[3:2]	Select output capacitors for Data Lane 1.
D0S_CAP [1:0]	[1:0]	Select output capacitors for Data Lane 0.

5.5.7. **Current Status Registers**

5.5.7.1. LANE_STATUS_HS (0x0290)

Writing the status bits is invalid and no affect.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								CLActiveHS	Reserved			D3TxActiveHS	D2TxActiveHS	D1TxActiveHS	D0TxActiveHS
Type	-								R	-			R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CLActiveHS	7	High Speed State of Clock Lane. 0: LP state. 1: HS state. When the line transition from LP11 to LP00 through LP01 is detected, this bit is set. When Stopstate is detected, this bit is cleared to 0.
D3TxActiveHS	3	High Speed State of Data Lane 3. The explanation is the same as CLActiveHS.
D2TxActiveHS	2	High Speed State of Data Lane 2. The explanation is the same as CLActiveHS.
D1TxActiveHS	1	High Speed State of Data Lane 1. The explanation is the same as CLActiveHS.
D0TxActiveHS	0	High Speed State of Data Lane 0. The explanation is the same as CLActiveHS.

5.5.7.2. LANE_STATUS_LP (0x0294)

Writing the status bits is invalid and no affect.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved									L0Direction	Reserved		L3UlpsEsc	L2UlpsEsc	L1UlpsEsc	L0UlpsEsc
Type	-									R	-		R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ClUlpsActive	Reserved			L3UlpsActive	L2UlpsActive	L1UlpsActive	L0UlpsActive	ClStopState	Reserved			L3StopState	L2StopState	L1StopState	L0StopState
Type	R	-			R	R	R	R	R	-			R	R	R	R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register shows the current status and the bit value changes dynamically.
When the lanes are disabled, the status of the lane is invalid.

Register Field	Bit	Description
L0Direction	22	Direction bit status of Data Lane 0. 0: Direction signal is 0. This means that CDSI detects BTA from host and Data Lane 0 is in LPTX mode, or in LPRX mode, at which host device has not received BTA return from CDSI. 1: Direction signal is 1. This means that Data Lane 0 is in LPRX mode.
L3UlpsEsc	19	Data Lane 3 Rx Ulps Esc The explanation is the same as ClUlpsEsc. 0: Indicates that Data Lane is neither of ULPS state or Mark-1 state which is an intermediate state to exit ULPS. 1: Indicates that Data Lane is in ULPS state, including Mark-1 state which is an intermediate state to exit ULPS.
L2UlpsEsc	18	Data Lane 2 Rx Ulps Esc: The explanation is the same as L3UlpsEsc.
L1UlpsEsc	17	Data Lane 1 Rx Ulps Esc: The explanation is the same as L3UlpsEsc.
L0UlpsEsc	16	Data Lane 0 Rx Ulps Esc: The explanation is the same as L3UlpsEsc.
ClUlpsActive	15	Clock Lane Rx Ulps Active 0: Indicates that Clock Lane is not in ULPS state. 1: Indicates that Clock Lane is in ULPS state.
L3UlpsActive	11	Data Lane 3 Rx Ulps Active 0: Indicates that Data Lane 3 is not in ULPS state. 1: Indicates that Data Lane 3 is in ULPS state.
L2UlpsActive	10	Data Lane 2 Rx Ulps Active The explanation is the same as L3UlpsActive.
L1UlpsActive	9	Data Lane 1 Rx Ulps Active The explanation is the same as L3UlpsActive.
L0UlpsActive	8	Data Lane 0 Rx Ulps Active The explanation is the same as L3UlpsActive.
ClStopState	7	Clock Lane Stop State The initial value depends on the lane status. 0: Indicates that Clock Lane is not in Stop state. 1: Indicates that Clock Lane is in Stop state.
L3StopState	3	Data Lane 3 Stop State The initial value depends on the lane status. 0: Indicates that Data Lane 3 is not in Stop state. 1: Indicates that Data Lane 3 is in Stop state.

Register Field	Bit	Description
L2StopState	2	Data Lane 2 Stop State The explanation is the same as L3StopState.
L1StopState	1	Data Lane 1 Stop State
L0StopState	0	Data Lane 0 Stop State

5.5.8. **MIPI PLL Control Registers**

5.5.8.1. MIPI_PLL_CTRL (0x02A0)

PLL Control register settings.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														MP_CKEN	MP_ENABLE
Type	-														R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MP_CKEN	1	Clock enable of HSCK, HSCKB, HSBYTECK, HSCKBY2, HSCKBY4 and HSCKBY8
MP_ENABLE	0	MIPI PLL Enable

5.5.8.2. MIPI_PLL_LOCKCNT (0x02A4)

PLL lock counter. The counter to count to wait for PLL lock detection

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP_LOCKCNT															
Type	R/W															
Default	0xFFFF															

Register Field	Bit	Description
MP_LOCKCNT	[15:0]	MIPI PLL Lock count. Counter to wait until MIPI PLL lock is detected. This counter is counted by MP_CKREF.

5.5.8.3. MIPI_PLL_LOCK (0x02A8)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved															
Type	-															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															MP_LOCKUPDONE
Type	-															R
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MP_LOCKUPDONE	0	PLL lock done indication. Indicates PLL lock wait counter has expired.

5.5.8.4. MIPI_PLL_CONF (0x02AC)

PLL parameter settings.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved														MP_LBW	
Type	-														R/W	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP_PRD				MP_FRS		MP_LFBREN	MP_FBD								
Type	R/W				R/W		R/W	R/W								
Default	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MP_LBW	[17:16]	Low Bandwidth setting 00: 25% of maximum loop bandwidth. 01: 33% of maximum loop bandwidth. 10: 50% of maximum loop bandwidth. 11: maximum loop bandwidth.
MP_PRD	[15:12]	Input Divider Value; Division ration = (MP_PRD[3:0] + 1)
MP_FRS	[11:10]	Frequency range setting (post divider) for HSCK. 00: 500 MHz …1 GHz 01: 250 MHz … 500 MHz 10: 125 MHz … 250 MHz 11: 62.5 MHz…125 MHz
MP_LFBREN	9	Lower Frequency Bound Removal enable
MP_FBD	[8:0]	Feedback divider value. Division ratio = (MP_FBD[8:0] + 1)

5.6. DSI-TX1 Registers

DSI-TX1 registers are identical as in DSI-TX0 register description. Only different are the segment address assignment. TX1 registers are 0x0200 + those of TX0's.

5.7. CDSI-TX Wrapper Registers

5.7.1. DCS COMMAND SELECTION REGISTER (CMD_SEL:0x0500)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												dcs_cm_act	dcs_cm_sel		Reserved
Type	-												R/W	R/W		-
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
dcs_cm_act	3	DCS Command Active Option 0: Send DCS command at Vertical Front Porch 1: Send DCS command at Vertical Back Porch
dcs_cm_sel	[2:1]	DCS Command Select 00: Select DSITX0 I/F 01: Select DSITX1 I/F 1x: Select both DSITX0 and DSITX1 I/F Note: when select 2'b1x, when write to DCSCMD_ID, DCSCMD_WC and DCSCMD_WDn will write to both DSITX0 and DSITX1.

5.7.2. DCSCMD_ST (DCSCMD_ST:0x0502)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		dcs_cmd_entry						Reserved			dcs_cmd_done		dcs_cmd_oflow	dcs_cmd_empty	dcs_cmd_full
Type	-		RO						-			RO		RO	RO	RO
Default	0	0	32						0	0	0	0	0	0	1	0

Register Field	Bit	Description
dcs_cmd_entry	[13:8]	DCS Command Entry available for writing in the command queue FIFO Command queue FIFO is 32 deep. So valid value is 0 to 32.
dcs_cmd_done	[4:3]	DCS Command done count Note: Wrap around counter that increments by 1 for every DSI command ths send out on MIPI I/F
dcs_cmd_oflow	[2]	DCS Command FIFO overflow 0: Normal 1: Overflow Write 1 to this bit to clear overflow flag. Note that all data written that cause overflow are dropped. Host should take care not to cause overflow. Unexpected behavioral can result because of overflow.
dcs_cmd_empty	[1]	DCS Command FIFO empty 0: Fifo not empty 1: Fifo empty
dcs_cmd_full	[0]	DCS Command FIFO Full 0: Not full 1: Fifo full

5.7.3. **DCS Command Q Register (DCSCMD_Q: 0x0504)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	dcs_cmdq															
Type	WO															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
dcs_cmdq	[15:0]	0x0000	**DCS Command Queue** Write to this will write to the DCS command queue (32 deep) Note: check dcscmd_st to know the command queue status

5.7.4. **STX0_MAXFCNT (STX0_MAXFCNT:0x0510)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_maxfcnt															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Stx0_maxfcnt	[15:0]	0x0000	STX0 DSITX Maximum Frame Count

5.7.5. **STX1_MAXFCNT (STX1_MAXFCNT:0x0514)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_maxfcnt															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_maxfcnt	[15:0]	STX1 DSITX Maximum Frame Count

5.7.6. **STX0_3Dreg0 (STX0_3Dreg0:0x0580)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_3d_en		Reserved	Stx0_3dcm_line												
Type	R/W		-	R/W												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_3d_en	[15:14]	DSI 3D command mode 00: No 3D Mode VSS/DCS command 01: 3D Mode VSS transmit enable 10: 3D Mode Command Transmit enable 11: Reserved
Stx0_3dcm_line	[12:0]	STX0 DSITX Maximum Frame Count

5.7.7. **STX0_3Dreg1 (STX0_3Dreg1:0x0582)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_3d_lpldt															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_3d_lpldt	[15:0]	DSITX0 3d Mode VSS payload or 3D Mode DCS command payload

5.7.8. **STX0_3Dreg2 (STX0_3Dreg2:0x0584)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_3dcm_di								Stx0_3d_upldt							
Type	R/W								R/W							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_3dcm_di	[15:8]	DSITX0 3D DCS Command Data Identifier [7:6]: VC [5:0]: Data Type
Stx0_3d_upldt	[7:0]	DSITX0 3d Mode VSS payload or 3D Mode DCS command payload - Upper 8-bits

5.7.9. **STX0_dsiphy_ctrl0 (STX0_dsiphy_ctrl0:0x0590)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_auto_cal_cnt								Reserved		Stx0_flprx_caltrim_data			Stx0_flprx_caltrim	Stx0_flprx_cal_cntl	Stx0_auto_cal_st
Type	R/W								RO		R/W			R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_auto_cal_cnt	[15:8]	Set the count up value for auto calibration
Stx0_flprx_caltrim_data	[5:3]	Force LPRXCALTRIM data
Stx0_flprx_caltrim	2	Force LPRXCALTRIM signals 0: Not Force 1: Force
Stx0_flprx_cal_cntl	1	Enable force LPRXCAL signal control 0: LPRXCALEn and LPRXCALRES are control by CDSI internal logic 1: LPRXCALEN and LPRXCALRES signals are controlled by FORCE_LPRX_CALEN and FORCE_LPRX_CALRES
Stx0_auto_cal_st	0	Start of auto calibration of LPRX 0: Idle 1: Start

5.7.10. **STX0_dsiphy_ctrl1 (STX0_dsiphy_ctrl1:0x0592)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											Stx0_flptx_curen		Stx0_fdphy_advlden	Stx0_flprx_calres	Stx0_flprx_calen
Type	RO											R/W		R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_flptx_curen	[4:3]	Force D-Phy LPTXCURREN1 and LPTXCURREN0 signals when FORCE_DPHY_ADVIDEN is high
Stx0_fdphy_advlden	2	Force D-Phy characteristic adjustment value by the input signal
Stx0_flprx_calres	1	LPRX Calibration Reset
Stx0_flprx_calen	0	LPRX Calibration Enable

5.7.11. **STX1_3Dreg0 (STX1_3Dreg0:0x05C0)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_3d_en		Reserved	Stx1_3dcm_line												
Type	R/W		RO	R/W												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_3d_en	[15:14]	DSI 3D command mode 00: No 3D Mode VSS/DCS command 01: 3D Mode VSS transmit enable 10: 3D Mode Command Transmit enable 11: Reserved
Stx1_3dcm_line	[12:0]	STX1 DSITX Maximum Frame Count

5.7.12. **STX1_3Dreg1 (STX1_3Dreg1:0x05C2)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_3d_lpldt															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_3d_lpldt	[15:0]	DSITX1 3d Mode VSS payload or 3D Mode DCS command payload

5.7.13. **STX1_3Dreg2 (STX1_3Dreg2:0x05C4)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_3dcm_di								Stx1_3d_upldt							
Type	R/W								R/W							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_3dcm_di	[15:8]	DSITX1 3D DCS Command Data Identifier [7:6]: VC [5:0]: Data Type
Stx1_3d_upldt	[7:0]	DSITX1 3d Mode VSS payload or 3D Mode DCS command payload - Upper 8-bits

5.7.14. **STX1_dsiphy_ctrl0 (STX1_dsiphy_ctrl0:0x05D0)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_auto_cal_cnt								Reserved		Stx1_flprx_caltrim_data			Stx1_flprx_caltrim	Stx1_flprx_cal_cntrl	Stx1_auto_cal_st
Type	R/W								RO		R/W			R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_auto_cal_cnt	[15:8]	Set the count up value for auto calibration
Stx1_flprx_caltrim_data	[5:3]	Force LPRXCALTRIM data
Stx1_flprx_caltrim	2	Force LPRXCALTRIM signals 0: Not Force 1: Force
Stx1_flprx_cal_cntrl	1	Enable force LPRXCAL signal control 0: LPRXCALEn and LPRXCALRES are control by CDSI internal logic 1: LPRXCALEN and LPRXCALRES signals are controlled by FORCE_LPRX_CALEN and FORCE_LPRX_CALRES
Stx1_auto_cal_st	0	Start of auto calibration of LPRX 0: Idle 1: Start

5.7.15. **STX1_dsiphy_ctrl1 (STX1_dsiphy_ctrl1:0x05D2)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											Stx1_flptx_curen		Stx1_fdphy_advlden	Stx1_flprx_calres	Stx1_flprx_calen
Type	RO											R/W		R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_flptx_curen	[4:3]	Force D-Phy LPTXCURREN1 and LPTXCURREN0 signals when FORCE_DPHY_ADVIDEN is high
Stx1_fdphy_advlden	2	Force D-Phy characteristic adjustment value by the input signal
Stx1_flprx_calres	1	LPRX Calibration Reset
Stx1_flprx_calen	0	LPRX Calibration Enable

5.8. CEC Control Registers

5.8.1. CEC Clock High Time Register 0 (CecHclk: 0x0028)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					cechclk			cechclk							
Type	RO					R/W			R/W							
Default	0	0	0	0	0	0	1	0	0x90							

Register Field	Bit	Description
cechclk	[10:0]	CEC Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk …

5.8.2. CEC Clock Low Time Register 0 (CecLclk: 0x002A)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved					ceclclk			ceclclk							
Type	RO					R/W			R/W							
Default	0	0	0	0	0	0	1	0	0x90							

Register Field	Bit	Description
ceclclk	[10:0]	CEC Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk …

5.8.3. CEC Enable Register (CECEN: 0x0600)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CECEN
Type	RO															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.2 CEC Enable Register

Register Field	Bit	Description
CECEN	0	**CEC operation** 0: Disable 1: Enable

5.8.4. **CEC Logical Address Register (CECADD: 0x0604)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CECADD															
Type	R/W															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.3 CEC Logical Address Register

Register Field	Bit	Description
CECADD	[15:0]	**Specify logical address assigned to CEC** Each bit corresponds to individual address, therefore multiple addresses can be assigned to CEC logic

5.8.5. **CEC Reset Register (CECRST: 0x0608)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CECRST
Type	RO															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.4 CEC Reset Register

Register Field	Bit	Description
CECRST	0	**CEC soft reset** 0: Disable 1: Enable Setting this bit to “1” affects the following: - Reception: Stops immediately. The received data is discarded. -Transmission (including the CEC line): Stops immediately. - Registers: The following registers are initialized. (CECADD, CECREN, CECRCR1, CECRCR2, CECRCR3,CECTEN, CECTCR, CECRSTAT, CECTSTAT, CECRBUF01-16, CECTBUF01-16, CECRCTR)

5.8.6. **CEC Receive Enable (CECREN: 0x060C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															CECREN
Type	RO															R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.5 CEC Receive Enable Register

Register Field	Bit	Description
CECREN	0	**CEC reception enable** 0: Disable 1: Enable

5.8.7. **CEC Receive Control Register 1 (CECRCTL1: 0x0614)**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved							CECACKDIS	Reserved		CECHNC		Reserved	CECLNC		
Type	RO							R/W	RO		R/W		RO	R/W		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CECMIN			Reserved	CECMAX			Reserved	CECDAT			CECTOUT		CECRIHLD	CECOTH
Type	RO	R/W			RO	R/W			RO	R/W			R/W		R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.6 CEC Receive Control Register 1

Register Field	Bit	Description
CECACKDIS	24	Enable ACK transmission 0: Disable 1: Enable
CECHNC	[21:20]	Number of consecutive cycles sampling logical '1' for noise cancellation 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
CECLNC	[18:16]	Number of consecutive cycles sampling logical '0' for noise cancellation 000: 1 cycle 001: 2 cycles 100: 3 cycles 100: 4 cycles 111: 8 cycles

Register Field	Bit	Description
CECMIN	[14:12]	The minimum time to to detect valid bit value. Error is detected when signal changes earlier than the minimum value 000: 2.05ms 001: 2.05ms+1cycle 010: 2.05ms+2cycles 011: 2.05ms+3cycles 100: 2.05ms-1cycle 101: 2.05ms-2cycles 110: 2.05ms-3cycles 111: 2.05ms-4cycles
CECMAX	[10:8]	The maximum time to detect valid bit value. Error is detected when signal does not change within the maximum time 000: 2.75ms 001: 2.75ms+1cycle 010: 2.75ms+2cycles 011: 2.75ms+3cycles 100: 2.75ms-1cycle 101: 2.75ms-2cycles 110: 2.75ms-3cycles 111: 2.75ms-4cycles
CECDAT	[6:4]	Time to detect CEC signal as valid (0 or 1) 000: 1.05ms 001: 1.05ms+2cycles 010: 1.05ms+4cycles 011: 1.05ms+6cycles 100: 1.05ms-2cycles 101: 1.05ms-4cycles 110: 1.05ms-6cycles 111: Reserved
CECTOUT	[3:2]	Number of cycles to determine timeout 00: 1 bit cycle 01: 2 bit cycles 10: 3 bit cycles 11: Reserved
CECRIHLD	1	Suspend CEC receive error interrupt 0: Disable 1: Enable
CECOTH	0	For Testing only. Enable the CEC reception when address does not match 0: Disable 1: Enable

5.8.8. **CEC Receive Control Register 2 (CECRCTL2: 0x0618)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CECSWAV3			Reserved	CECSWAV2			Reserved	CECSWAV1			Reserved	CECSWAV0		
Type	RO	R/W			RO	R/W			RO	R/W			RO	R/W		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.7 CEC Receive Control Register 2

Register Field	Bit	Description
CECSWAV3	[14:12]	Maximum time to detect start bit 000: 4.7ms 001: 4.7ms+1cycle 010: 4.7ms+2cycles 011: 4.7ms+3cycles 100: 4.7ms+4cycles 101: 4.7ms+5cycles 110: 4.7ms+6cycles 111: 4.7ms+7cycles
CECSWAV2	[10:8]	Minimum time to detect start bit 000: 4.3ms 001: 4.3ms-1cycle 010: 4.3ms-2cycles 011: 4.3ms-3cycles 100: 4.3ms-4cycles 101: 4.3ms-5cycles 110: 4.3ms-6cycles 111: 4.3ms-7cycles
CECSWAV1	[6:4]	Maximum time to detect start bit rising 000: 3.9ms 001: 3.9ms+1cycle 010: 3.9ms+2cycles 011: 3.9ms+3cycles 100: 3.9ms+4cycles 101: 3.9ms+5cycles 110: 3.9ms+6cycles 111: 3.9ms+7cycles
CECSWAV0	[2:0]	Minimum time to detect start bit rising 000: 3.5ms 001: 3.5ms-1cycle 010: 3.5ms-2cycles 011: 3.5ms-3cycles 100: 3.5ms-4cycles 101: 3.5ms-5cycles 110: 3.5ms-6cycles 111: 3.5ms-7cycles

5.8.9. **CEC Receive Control Register 3 (CECRCTL3: 0x061C)**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								Reserved	CECWAV3			Reserved	CECWAV2		
Type	RO								RO	R/W			RO	R/W		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CECWAV1			Reserved	CECWAV0			Reserved			CECACKEI	CECMINEI	CECMAXEI	CECRSTEI	CECWAVEI
Type	RO	R/W			RO	R/W			RO			R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.8 CEC Receive Control Register 3

Register Field	Bit	Description
CECWAV3	[22:20]	The latest rising timing of logical 0 000: 1.7ms 001: 1.7ms+1cycle 010: 1.7ms+2cycles 011: 1.7ms+3cycles 100: 1.7ms+4cycles 101: 1.7ms+5cycles 110: 1.7ms+6cycles 111: 1.7ms+7cycles
CECWAV2	[18:16]	The fastest rising timing of a logical 0 000: 1.3ms 001: 1.3ms-1cycle 010: 1.3ms-2cycles 011: 1.3ms-3cycles 100: 1.3ms-4cycles 101: 1.3ms-5cycles 110: 1.3ms-6cycles 111: 1.3ms-7cycles
CECWAV1	[14:12]	The latest rising timing of logical 1 000: 0.8ms 001: 0.8ms+1cycle 010: 0.8ms+2cycles 011: 0.8ms+3cycles 100: 0.8ms+4cycles 101: 0.8ms+5cycles 110: 0.8ms+6cycles 111: 0.8ms+7cycles
CECWAV0	[10:8]	The fastest rising of a logical 1 000: 0.4ms 001: 0.4ms-1cycle 010: 0.4ms-2cycles 111: 0.4ms-3cycles 100: 0.4ms-4cycles 101: 0.4ms-5cycles 110: 0.4ms-6cycles 111: 0.4ms-7cycles
CECACKEI	4	ACK collision error interrupt enable 0: Disable 1: Enable
CECMINEI	3	Minimum timing error detection interrupt enable 0: Disable 1: Enable

Register Field	Bit	Description
CECMAXEI	2	Maximum timing error detection interrupt enable 0: Disable 1: Enable
CECRSTEI	1	Start bit interrupt enable 0: Disable 1: Enable
CECWAVEI	0	Waveform error interrupt enable 0: Disable 1: Enable

5.8.10. **CEC Transmit Enable Register (CECTEN: 0x0620)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														CECT Busy	CECT EN
Type	RO														RO	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.9 CEC Transmit Enable Register

Register Field	Bit	Description
CECTBusy	1	CEC transmit state (read only) 0: idle 1: active
CECTEN	0	CEC transmission control 0: Disable 1: Enable

5.8.11. **CEC Transmit Control Register (CECTCTL: 0x0628)**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								Reserved	CECSTRS			Reserved	CECSPRD		
Type	RO								RO	R/W			RO	R/W		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	CECDTRS			CECDPRD				Reserved			CECBRD	CECFREE			
Type	RO	R/W			R/W				RO			R/W	R/W			
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.10 CEC Transmit Control Register

Register Field	Bit	Description
CECSTRS	[22:20]	Rising cycle time of the start bit – between the default values and 0-7 cycles 000: default value (to 3.7ms) 001: default value – 1 cycle 010: default value – 2 cycles 011: default value – 3 cycles 100: default value – 4 cycles 101: default value – 5 cycles 110: default value – 6 cycles 111: default value – 7 cycles
CECSPRD	[18:16]	Start bit cycle time 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
CECDTRS	[14:12]	Rising cycle time of data bit 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
CECDPRD	[11:8]	Data bit cycle time 0000: RV 1000: RV – 8 cycles 0001: RV – 1 cycle 1001: RV – 9 cycles 0010: RV – 2 cycles 1010: RV – 10 cycles 0011: RV – 3 cycles 1011: RV – 11 cycles 0100: RV – 4 cycles 1100: RV – 12 cycles 0101: RV – 5 cycles 1101: RV – 13 cycles 0110: RV – 6 cycles 1110: RV – 14 cycles 0111: RV – 7 cycles 1111: RV – 15 cycles
CECBRD	4	Broadcast transmit enable 0: disable 1: enable

Register Field	Bit	Description
CECFREE	[3:0]	Number of cycles for checking the line to be inactive before the start of transmission 0000: 1-bit cycle 1000: 9 bit cycle 0001: 2 bit cycle 1001: 10 bit cycle 0010: 3 bit cycle 1010: 11 bit cycle 0011: 4 bit cycle 1011: 12 bit cycle 0100: 5 bit cycle 1100: 13 bit cycle 0101: 6 bit cycle 1101: 14 bit cycle 0110: 7 bit cycle 1110: 15 bit cycle 0111: 8 bit cycle 1111: 16 bit cycle

5.8.12. **CEC Receive Interrupt Status Register (CECRSTAT: 0x062C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved									CECRIWA	CECRIOR	CECRIACK	CECRIMIN	CECRIMAX	CECRISTA	CECRIEND
Type	RO									RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.11 CEC Receive Interrupt Status Register

Register Field	Bit	Description
CECRIWA	6	CEC Waveform error interrupt flag
CECRIOR	5	Receive buffer full flag
CECRIACK	4	ACK collision detection flag
CECRIMIN	3	Bit cycle time is less than minimum time flag
CECRIMAX	2	Bit cycle time is greater than maximum time flag
CECRISTA	1	Start bit detection flag
CECRIEND	0	Reception of CEC message with EOM

5.8.13. **CEC Transmit Interrupt Status Register (CECTSTAT: 0x0630)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											CECTIUR	CECTIACK	CECTIAL	CECTIEND	Reserved
Type	RO											RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.12 Interrupt Flag Register

Register Field	Bit	Description
CECTIUR	4	Transmission is completed and the transmit buffer is empty
CECTIACK	3	ACK error detection flag
CECTIAL	2	Arbitration loss flag (“0” is detected while transmit “1”)
CECTIEND	1	Data block transmission completion flag
Reserved	0	Reserved

5.8.14. **CEC Receive Buffer Registers (01-16) (CECRBUF01-16: 0x0634-0x0670)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved						CECRACK	CECEOM	CECRBYTE							
Type	RO						RO	RO	RO							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.13 CEC Receive Buffer Registers (01-16)

Register Field	Bit	Description
CECRACK	9	ACK bit received
CECEOM	8	EOM bit received
CECRBYTE	[7:0]	CEC byte received

5.8.15. **CEC Transmit Buffer Registers (01-16) (CECTBUF01-16: 0x0674-0x06B0)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							CECTEOM	CECTBYTE							
Type	RO							R/W	R/W							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.14 CEC Transmit Buffer Registers (01-16)

Register Field	Bit	Description
CECTEOM	8	EOM bit value to be transmitted
CECTBYTE	[7:0]	Byte data to be transmitted

5.8.16. **CEC Receive Byte Counter Register (CECRCTR: 0x06B4)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved											CECRCTR				
Type	RO											RO				
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.15 Interrupt Flag Register

Register Field	Bit	Description
CECRCTR	[4:0]	Numbers of bytes received

5.8.17. **CEC Interrupt Enable Register (CECIMSK: 0x06C0)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														CECTIM	CECRIM
Type	RO														R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.16 CEC Interrupt Enable Register

Register Field	Bit	Description
CECTIM	1	CEC Transmit status interrupt enable 0: disable 1: enable
CECRIM	0	CEC Receive status interrupt enable 0: disable 1: enable

5.8.18. **CEC Interrupt Clear Register (CECICLR: 0x06CC)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved														CECTICLR	CECRICLR
Type	RO														WO	WO
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5.17 CEC Interrupt Enable Register

Register Field	Bit	Description
CECTICLR	1	Host writes “1” to this bit to clear CEC Transmit status interrupt
CECRICLR	0	Host writes “1” to this bit to clear CEC Receive status interrupt

5.9. Splitter Control Registers

5.9.1. **STX0_CTRL (STX0_CTRL:0x5000)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							Stx0_spbp	Reserved							Stx0_lcd_csel
Type	RO							R/W	RO						R/W	R/W
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx0_spbp	8	STX0 Splitter bypass 0: Enable Split 1: Bypass
Stx0_lcd_csel	0	STX0 LCD Controller Clock Select (DSITX0 video path) 0: 2 x DSI Clock (Default) 1: 1 x DSI Clock

5.9.2. **STX0 Packet ID Register 1 (STX0_PacketID1: 0x5002)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx0_VPID1								Stx0_VPID0							
Type	R/W								R/W							
Default	0x34								0x35							

Register Field	Bit	Description
Stx0_VPID1	[15:8]	DSITX0 Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
Stx0_VPID0	[7:0]	DSITX0 Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

5.9.3. **STX0_WC (STX0_WC:0x5008)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx0_wc															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx0_wc	[15:0]	Splitter TX0 Line Word Count Defined total number of byte for each line. Note: only valid when stcx_wc is not equal to “0”. Word Count is directly from HDMIRX source if stx_ehw = “1”.

5.9.4. **STX0_DPX (STX0_DPX:0x500A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		stx0_de_px						Reserved		stx0_db_px					
Type	RO		R/W						RO		R/W					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
stx0_de_px	[13:8]	Splitter TX0 End Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted … 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the end of the line
stx0_db_px	[5:0]	Splitter TX0 Beginning Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted … 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the beginning of the line

5.9.5. **STX0_FPX (STX0_FPX:0x500C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx_ehw	stx_Tx1sel	Reserved		stx0_fpxv											
Type	R/W	R/W	RO		R/W											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
stx_ehw	15	Spitter TX HW enable 0: Select Manual setting (used stx0/1_fpxv, stx0/1_lpx parameters) 1: automatically split line into half for both stx0 and stx1
stx_Tx1sel	14	Spitter TX L/R select 0: Select 1st half of the line for STX0, 2nd half for STX1 1: Select 2nd half of the line for STX0, 1st half for STX1 Note: 1) only valid when stx_ehw = 1 2) if stx_hsel=0 - stx0_db_px indicates # Dummy pixel inserted at beginning - stx0_de_px indicates # pixels overlap at the end (not Dummy pixel) if stx_hsel=1 - stx0/1_db_px indicates # pixels overlap at the beginning (Not Dummy pixel) - stx0/1_de_px indicates # Dummy pixels inserted at the end
stx0_fpxv	[11:0]	Splitter TX0 First Pixel Valid 12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line … 12'hFFF: 4096 pixel in HDMIRX line Note: Note: This parameter indicates the first pixel location to transmit to DSITX0

5.9.6. **STX0_LPX (STX0_LPX:0x500E)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				stx0_lpxv											
Type	RO				R/W											
Default	0	0	0	0	0x000											

Register Field	Bit	Description
stx0_lpxv	[11:0]	Splitter TX0 Last Pixel Valid 12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line … 12'hFFF: 4096 pixel in HDMIRX line Note: This parameter indicates the last pixel location to transmit to DSITX0

5.9.7. **STX0_DRPX (STX0_DRPX:0x5010)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx0_dRpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx0_dRpx	[15:0]	**TX0 Red Dummy Pixel**

5.9.8. **STX0_DGPX (STX0_DGPX:0x5012)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx0_dGpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx0_dGpx	[15:0]	**TX0 Green Dummy Pixel**

5.9.9. **STX1_CTRL (STX1_CTRL:0x5080)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							Stx1_spbp	Reserved							Stx1_lcd_csel
Type	RO							R/W	RO						R/W	R/W
Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_spbp	8	**STX1 Splitter bypass** 0: Enable Split 1: Bypass
Stx1_lcd_csel	0	**STX1 LCD Controller Clock Select (DSITX0 video path)** 0: 2 x DSI Clock (Default) 1: 1 x DSI Clock

5.9.10. **STX1 Packet ID Register 1 (STX1_PacketID1: 0x5082)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_VPID1								Stx1_VPID0							
Type	R/W								R/W							
Default	0x34								0x35							

Register Field	Bit	Description
Stx1_VPID1	[15:8]	DSITX1 Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
Stx1_VPID0	[7:0]	DSITX1 Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

5.9.11. **STX0_DBPX (STX0_DBPX:0x5014)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx0_dBpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx0_dBpx	[15:0]	TX0 Blue Dummy Pixel

5.9.12. **STX1_WC (STX1_WC:0x5088)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Stx1_wc															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
Stx1_wc	[15:0]	Splitter TX1 Line Word Count Defined total number of byte for each line. Note: only valid when Note: only valid when stc1_wc is not equal to “0”. Word Count is directly from HDMIRX source if stx_ehw = “1”

5.9.13. **STX1_DPX (STX1_DPX:0x508A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved		Stx1_de_px						Reserved		Stx1_db_px					
Type	RO		R/W						RO		R/W					
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Stx1_de_px	[13:8]	Splitter TX1 End Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted … 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the end of the line
Stx1_db_px	[5:0]	Splitter TX1 Beginning Dummy Pixel 6'h00: No dummy pixel inserted 6'h01: Dummy pixel inserted … 6'h2x: 32 Dummy pixels inserted (maximum) Note: These Dummy pixels inserted at the beginning of the line

5.9.14. **STX1_FPX (STX1_FPX:0x508C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Stx1_fpxv											
Type	RO				R/W											
Default	0	0	0	0	0x000											

Register Field	Bit	Description
Stx1_fpxv	[11:0]	Splitter TX1 First Pixel Valid 12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line … 12'hFFF: 4096 pixel in HDMIRX line Note: Note: This parameter indicates the first pixel location to transmit to DSITX1

5.9.15. **STX1_LPX (STX1_LPX:0x508E)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Stx1_lpxv											
Type	RO				R/W											
Default	0	0	0	0	0x000											

Register Field	Bit	Description
Stx1_lpxv	[11:0]	Splitter TX1 Last Pixel Valid 12'h000: 1st pixel in HDMIRX line 12'h001: 2nd pixel in HDMIRX line … 12'hFFF: 4096 pixel in HDMIRX line Note: This parameter indicates the last pixel location to transmit to DSITX1

5.9.16. **STX1_DRPX (STX1_DRPX:0x5090)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx1_dRpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx1_dRpx	[15:0]	TX1 Red Dummy Pixel

5.9.17. **STX1_DGPX (STX1_DGPX:0x5092)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx1_dGpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx1_dGpx	[15:0]	TX1 Green Dummy Pixel

5.9.18. **STX1_DBPX (STX1_DBPX:0x5094)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	stx1_dBpx															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
stx1_dBpx	[15:0]	TX1 Blue Dummy Pixel

5.10. Internal Color Bar Generator

5.10.1. **Color Bar Control Register (CB_CTRL: 0x7000)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved												cb_csel	cb_type		cb_en
Type	RO												R/W	R/W		R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
cb_csel	3	Color Bar Clock Select 0: CDSITX0 CDSICLK 1: CDSITX1 CDSICLK/2
cb_type	[2:1]	Color Bar Type 0x: Reserved 10: Color bar mode 11: Color Checkers mode
cb_en	0	Color Bar Enable 0: Disable 1: Enable

5.10.2. **Color Bar HSW Register (CB_HSW: 0x7008)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	cb_hs_width														
Type	RO	R/W														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
cb_hs_width	[14:0]	Color Bar – HS Width

5.10.3. **Color Bar VSW Register (CB_VSW: 0x700A)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved	cb_vs_width														
Type	RO	R/W														
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register Field	Bit	Description
cb_vs_width	[14:0]	Color Bar – VS Height

5.10.4. **Color Bar H-Total Register (CB_HTotal: 0x700C)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_h_total															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_h_total	[15:0]	Color Bar – H Total

5.10.5. **Color Bar V-Total Register (CB_VTotal: 0x700E)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_v_total															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_v_total	[15:0]	Color Bar – V Total

5.10.6. **Color Bar HActive Register (CB_HAct: 0x7010)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_h_act															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_h_act	[15:0]	Color Bar – H Active

5.10.7. **Color Bar VActive Register (CB_VAct: 0x7012)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_v_act															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_v_act	[15:0]	Color Bar – V Active

5.10.8. **Color Bar HStart Register (CB_HStart: 0x7014)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_h_start															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_h_start	[15:0]	Color Bar – H Start

5.10.9. **Color Bar VStart Register (CB_VStart: 0x7016)**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	cb_v_start															
Type	R/W															
Default	0x0000															

Register Field	Bit	Description
cb_v_start	[15:0]	Color Bar – V Start

5.11. HDMI Rx System Control

5.11.1. PHY CONTROL REGISTER (PHY_CTL) (0x8410)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved															PHYCtl
Type	RO														R/W	R/W
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Register Field	Bit	Description
PHYCtl	0	PHY power ON/OFF control mode 0: HOST manual setting 1: Linked with DDC5V detection

5.11.2. PHY ENABLE REGISTER (PHY_ENB) (0x8413)

	7	6	5	4	3	2	1	0
	Reserved							PHYEnb
Type	R/W							R/W
Default	0	0	1	1	1	1	1	0

Register Field	Bit	Description
PHYEnb	0	PHY Suspend mode 0: Suspend 1: Normal Operation Note: When PHY power ON/OFF control mode is for “HOST manual setting” (address 0x8410[0] == 0) only, → Write is enabled in this register. When PHY power ON/OFF control mode is “DDC5V detect link” (address0x04_10[0] == 1), DDC5V input =H, → Suspend is automatically cleared.

5.11.3. PHY RESET REGISTER (PHY_RSTX) (0x8414)

	7	6	5	4	3	2	1	0
	Reserved							PHYRstX
Type	R/W							R/W
Default	1	0	1	1	0	0	1	1

Register Field	Bit	Description
PHYRstX	0	PHY Rest Control 0: Reset 1: Normal Operation

5.11.4. **APLL CONTROL REGISTER (APLL_CTL) (0x84F0)**

	7	6	5	4	3	2	1	0
	Reserved		APLL_CPCTL		Reserved			APPL_ON
Type	RO		R/W		RO			R/W
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Description
APLL_CPCTL	[5:4]	Audio PLL Charge pump setting 00: HiZ 01: L-fix 10: H-fix 11: Normal Action
APPL_ON	0	Audio DAC/PLL Power ON/OFF Setting 0: Power OFF 1: Power ON

5.11.5. **DDC IO CONTROL REGISTER (DDCIO_CTL) (0x84F4)**

	7	6	5	4	3	2	1	0
	Reserved							DDCPWR
Type	RO							R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
DDCPWR	0	5V tolerant I/O Power Down signal. 0: Power Down 1: Normal Action

5.11.6. **INTERRUPT0 REGISTER (HDMI_INT0) (0x8500)**

	7	6	5	4	3	2	1	0
	I_KEY	Reserved					I_MISC	Reserved
Type	RO	RO					RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_KEY	7	KEY-EDID (address 0x85_0F) interrupt 0: No interrupt 1: Interrupt generated
I_MISC	1	MISC (address 0x85_0B) interrupt 0: No interrupt 1: Interrupt generated

5.11.7. **INTERRUPT1 REGISTER (HDMI_INT1) (0x8501)**

	7	6	5	4	3	2	1	0
	I_GBD	I_HDCP	I_ERR	I_AUD	I_CBIT	I_PACKET	I_CLK	I_SYS
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_GBD	7	GBD (address 0x85_09) interrupt 0: No interrupt 1: Interrupt generated
I_HDCP	6	HDCP (address 0x85_08) interrupt 0: No interrupt 1: Interrupt generated
I_ERR	5	ERR (address 0x85_07) interrupt 0: No interrupt 1: Interrupt generated
I_AUD	4	Audio Buffer (address 0x85_06) interrupt 0: No interrupt 1: Interrupt generated
I_CBIT	3	Audio CBIT (address 0x85_05) interrupt 0: No interrupt 1: Interrupt generated
I_PACKET	2	Info Packet (address 0x85_04) interrupt 0: No interrupt 1: Interrupt generated
I_CLK	1	Pixel CLK (address 0x85_03) interrupt 0: No interrupt 1: Interrupt generated
I_SYS	0	SYSTEM (address 0x85_02) interrupt 0: No interrupt 1: Interrupt generated

5.11.8. **SYSTEM INTERRUPT (SYS_INT) (0x8502)**

	7	6	5	4	3	2	1	0
	I_ACR_CTS	I_ACRN	I_DVI	I_HDMI	I_NOPMBDET	I_DPMBDET	I_TMDS	I_DDC
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_ACR_CTS	7	Receive CTS update interrupt 0: No interrupt 1: Interrupt generated
I_ACRN	6	Receive N update interrupt 0: No interrupt 1: Interrupt generated
I_DVI	5	HDMI→DVI change detection interrupt 0: No interrupt 1: Interrupt generated
I_HDMI	4	DVI→HDMI change detection interrupt 0: No interrupt 1: Interrupt generated
I_NOPMBDET	3	No DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_DPMBDET	2	With DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDS	1	TMDS amplitude change interrupt 0: No interrupt 1: Presence change detected (PHY squelch ON/OFF change detected)
I_DDC	0	DDC power change detection interrupt 0: No interrupt 1: 0V↔5V change detected

5.11.9. **CLOCK INTERRUPT (CLK_INT) (0x8503)**

	7	6	5	4	3	2	1	0
	I_OUT_DE_CHG	I_OUT_H_CHG	I_IN_DE_CHG	I_IN_HV_CHG	I_DC_CHG	I_PXCLK_CHG	I_PHYCLK_CHG	I_TMDSCLK_CHG
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_OUT_DE_CHG	7	Output side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated
I_OUT_H_CHG	6	(Output side) H counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_DE_CHG	5	(Input side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_HV_CHG	4	(Input side) HV counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_CHG	3	Deep Color mode change detection interrupt 0: No interrupt 1: Interrupt generated
I_PXCLK_CHG	2	Pixel CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_PHYCLK_CHG	1	PHY PLL CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDSCLK_CHG	0	TMDS CLK change detection interrupt 0: No interrupt 1: Interrupt generated

5.11.10. **PACKET INTERRUPT (PACKET_INT) (0x8504)**

	7	6	5	4	3	2	1	0
	I_PK_ISRC2	I_PK_ISRC	I_PK_ACP	I_PK_VS	I_PK_SPD	I_PK_MS	I_PK_AUD	I_PK_AVI
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_PK_ISRC2	7	ISRC2 packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_ISRC	6	ISRC1 packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_ACP	5	ACP packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_VS	4	861B VS_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_SPD	3	861B SPD_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_MS	2	861B MS_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_AUD	1	861B AUD_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_AVI	0	861B AVI_info packet update interrupt 0: No interrupt 1: Interrupt generated

* Interrupt is generated only when receive content has changed.
If the same data is repeatedly received, interrupt is not generated.

5.11.11. **CBIT INTERRUPT (CBIT_INT) (0x8505)**

	7	6	5	4	3	2	1	0
	I_AF_LOCK	I_AF_UNLOCK	Reserved	I_AU_DSD	I_AU_HBR	I_CBIT_NLPCM	I_CBIT_FS	I_CBIT
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_AF_LOCK	7	Audio clock frequency lock detection interrupt 0: No interrupt 1: Interrupt generated
I_AF_UNLOCK	6	Audio clock frequency unlock detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_DSD	4	DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR	3	HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_NLPCM	2	Normal Audio LPCM↔NLPCM change detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_FS	1	Receive data FS update interrupt 0: No interrupt 1: Interrupt generated
I_CBIT	0	Receive C_bit data [47:0] update interrupt 0: No interrupt 1: Interrupt generated

5.11.12. **AUDIO Buffer INTERRUPT (AUDIO_INT) (0x8506)**

	7	6	5	4	3	2	1	0
	I_BUF_OVER	I_BUF_NO2	I_BUF_NO1	I_BUF_CENTER	I_BUF_NU1	I_BUF_NU2	I_BUF_UNDER	I_BUFINIT_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_BUF_OVER	7	Buffer Over flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO2	6	Buffer Nearly Over (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO1	5	Buffer Nearly Over (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_CENTER	4	Buffer CENTER detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU1	3	Buffer Nearly Under (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU2	2	Buffer Nearly Under (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_UNDER	1	Buffer Under flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUFINIT_END	0	Buffer initial operation completed interrupt 0: No interrupt 1: Interrupt generated

5.11.13. **ERROR INTERRUPT (ERR_INT) (0x8507)**

	7	6	5	4	3	2	1	0
	I_EESS_ERR	I_AU_FRAME	I_NO_ACP	I_NO_AVI	I_DC_NOCD	I_DC_DEERR	I_DC_BUFERR	I_DC_PPERR
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_EESS_ERR	7	EESS error generation detection interrupt *1 [6] W1C/R 1'b0 0: No interrupt 1: Interrupt generate
I_AU_FRAME	6	60958Frame discontinuous change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_ACP	5	ACP Packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_AVI	4	AVI Packet receive cut detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_NOCD	3	Deep Color CD=0 (or not defined) generates 24bit mode auto move 0: No interrupt 1: Interrupt generated
I_DC_DEERR	2	In Deep Color Packing Group, DE position abnormal generation 0: No interrupt 1: Interrupt generated
I_DC_BUFERR	1	Deep Color FIFO flow generation 0: No interrupt 1: Interrupt generated
I_DC_PPERR	0	Deep Color UnPack phase dis-unified generation 0: No interrupt 1: Interrupt generated

*1 During HDMI(=EESS) mode, detects state where Enc_Disable, Enc_Enable can no longer be detected during HDCP decoding operation.

Used for detecting the abnormal state where HDCP goes OFF without the send side sending Enc_Disable.

5.11.14. **HDCP INTERRUPT (HDCP_INT) (0x8508)**

	7	6	5	4	3	2	1	0
	I_AVM_SET	I_AVM_CLR	I_LINKERR	I_SHA_END	I_R0_END	I_KM_END	I_AKSV_END	I_AN_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_AVM_SET	7	SET AVMUTE receive interrupt 0: No receive 1: With receive
I_AVM_CLR	6	CLRAE AVMUTE receive interrupt 0: No receive 1: With receive
I_LINKERR	5	Link error detection interrupt *1 0: No link error 1: Link error generated
I_SHA_END	4	V´value operation ended interrupt 0: During idle or operation 1: Operation ended
I_R0_END	3	Ks´, M0´, R0´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_KM_END	2	Km´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_AKSV_END	1	AKSV write completed interrupt 0: During idle or write 1: Write completed notification
I_AN_END	0	AN write completed interrupt 0: During idle or write 1: Write completed notification

*1 This interrupt is generated when other device termination of HDCP encoding is detected. (Detects IDLE State after HDCP certification No.3 part)

However, it may be set up even during HDMI SET_AVMUTE.

5.11.15. **GBD INTERRUPT (GBD_INT) (0x8509)**

	7	6	5	4	3	2	1	0
	I_GBD_PKERR	I_GBD_ACLR	I_P1GBD_CHG	I_P0GBD_CHG	Reserved	I_P1GBD_DET	I_GBD_OFF	I_GBD_ON
Type	W1C/R	W1C/R	W1C/R	W1C/R	RO	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_GBD_PKERR	7	GBD packet receive ERR generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ACLR	6	GBD packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated (cutoff generated)
I_P1GBD_CHG	5	Valid P1 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
I_P0GBD_CHG	4	Valid P0 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
I_P1GBD_DET	2	P1 GBD data receive generation interrupt 0: No interrupt 1: Interrupt generated Note: Not related to change in packet content, generated each time packet is received.
I_GBD_OFF	1	Valid GBD yes→no change generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ON	0	Valid GBD no→yes change generation interrupt 0: No interrupt 1: Interrupt generated

5.11.16. **MISC INTERRUPT (MISC_INT) (0x850b)**

	7	6	5	4	3	2	1	0
	I_AU_DSD_OFF	I_AU_HBR_OFF	I_VIDEO_COLOR	I_AS_LAYOUT	I_NO_SPD	I_NO_VS	I_SYNC_CHG	I_AUDIO_MUTE
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
I_AU_DSD_OFF	7	Discontinuity of DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR_OFF	6	Discontinuity of HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_VIDEO_COLOR	5	Video Color Space (RGB, YCbCr444, YCbCr422) change detection interrupt 0: No interrupt 1: Interrupt generated
I_AS_LAYOUT	4	audio Layout Bit change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_SPD	3	SPD_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_VS	2	VS_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_SYNC_CHG	1	Video sync signal state change detection interrupt 0: No interrupt 1: Interrupt generated
I_AUDIO_MUTE	0	Audio MUTE generation interrupt 0: No interrupt 1: Interrupt generated

5.11.17. **SYS INTERRUPT MASK (SYS_INTM) (0x8512)**

	7	6	5	4	3	2	1	0
	M_ACR_CTS	M_ACR_N	M_DVI_DET	M_HDMI_DET	M_NOPMBDET	M_BPMBDET	M_TMDS	M_DDC
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_ACR_CTS	7	Receive CTS update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_ACR_N	6	Receive N value update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DVI_DET	5	HDMI→DVI change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_HDMI_DET	4	DVI→HDMI change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NOPMBDET	3	No DataIsland Preamble detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BPMBDET	2	With DataIsland Preamble detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_TMDS	1	TMDS amplitude change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DDC	0	DDC power change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.18. **CLK INTERRUPT MASK (CLK_INTM) (0x8513)**

	7	6	5	4	3	2	1	0
	Reserved	M_OUT_H_CHG	M_IN_DE_CHG	M_IN_HV_CHG	M_DC_CHG	M_PXCLK_CHG	M_PHYCLK_CHG	M_TMDS_CHG
Type	RO	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
Reserved	7	
M_OUT_H_CHG	6	(Output side) H counter change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_IN_DE_CHG	5	(Input side) DE size and position change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_IN_HV_CHG	4	(Input side) HV counter change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_CHG	3	Deep Color change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PXCLK_CHG	2	Pixel CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PHYCLK_CHG	1	PHY PLL CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_TMDS_CHG	0	TMDS CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.19. **PACKET INTERRUPT MASK (PACKET_INTM) (0x8514)**

	7	6	5	4	3	2	1	0
	M_PK_ISRC2	M_PK_ISRC	M_PK_ACP	M_PK_VS	M_PK_SPD	M_PK_MS	M_PK_AUD	M_PK_AVI
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_PK_ISRC2	7	ISRC2 packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_ISRC	6	ISRC1 packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_ACP	5	ACP packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_VS	4	861B VS_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_SPD	3	861B SPD_info packet update interrupt mask ¥ 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_MS	2	861B MS_info packet update interrupt mask ¥ 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_AUD	1	861B AUD_info packet update interrupt mask ¥ 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_AVI	0	861B AVI_info packet update interrupt mask ¥ 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.20. **CBIT INTERRUPT MASK (CBIT_INTM) (0x8515)**

	7	6	5	4	3	2	1	0
	M_AF_LOCK	M_AF_UNLOCK	Reserved	M_AU_DSD	M_AU_HBR	M_CBIT_NLPCM	M_CBIT_FS	M_CBIT
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_AF_LOCK	7	Audio clock frequency lock detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AF_UNLOCK	6	Audio clock frequency unlock detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AU_DSD	4	DSD Audio packet receive detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AU_HBR	3	HBR Audio packet receive detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_CBIT_NLPCM	2	Receive data LPCM↔NLPCM change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_CBIT_FS	1	Receive data FS update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_CBIT	0	Receive C_bit data [39:0] update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.21. **AUDIO INTERRUPT MASK (AUDIO_INTM) (0x8516)**

	7	6	5	4	3	2	1	0
	M_BUF_OVER	M_BUF_NO2	M_BUF_NO1	M_BUF_CENTER	M_BUF_NU1	M_BUF_NU2	M_BUF_UNDER	M_BUFINIT_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_BUF_OVER	7	Buffer Over flow detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NO2	6	Buffer Nearly Over (Threshold 2) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NO1	5	Buffer Nearly Over (Threshold 1) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_CENTER	4	Buffer CENTER detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NU1	3	Buffer Nearly Under (Threshold 1) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NU2	2	Buffer Nearly Under (Threshold 2) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_UNDER	1	Buffer Under flow detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUFINIT_END	0	Buffer initialization operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.22. **ERR INTERRUPT MASK (ERR_INTM) (0x8517)**

	7	6	5	4	3	2	1	0
	M_EESS_ERR	M_AU_FRAME	M_NO_ACP	M_NO_AVI	M_DC_NOCD	M_DC_DEERR	M_DC_BUFERR	M_DC_PPERR
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_EESS_ERR	7	EESS error occurrence detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AU_FRAME	6	Audio 60958Frame discontinuous detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_ACP	5	ACP packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_AVI	4	AVI packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_NOCD	3	Deep color 24bit mode auto move occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_DEERR	2	In Deep Color Packing Group, DE position abnormal occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_BUFERR	1	Deep Color FIFO flow occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_PPERR	0	Deep Color UnPack phase dis-unify occurrence 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.23. **HDCP INTERRUPT MASK (HDCP_INTM) (0x8518)**

	7	6	5	4	3	2	1	0
	M_AVM_SET	M_AVM_CLR	M_LINKERR	M_SHA_END	M_R0_END	M_KM_END	M_AKSV_END	M_AN_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_AVM_SET	7	SET AVMUTE receive interrupt mask ¥ 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AVM_CLR	6	CLRAE AVMUTE receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_LINKERR	5	Link error detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_SHA_END	4	V´ value operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_R0_END	3	Ks´, M0´, R0´ operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_KM_END	2	Km´ operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AKSV_END	1	AKSV write completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AN_END	0	AN write completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.24. **GBD INTERRUPT MASK (GBD_INTM) (0x8519)**

	7	6	5	4	3	2	1	0
	M_GBD_PKERR	M_GBD_ACLR	M_P1GBD_CHG	M_P0GBD_CHG	Reserved	M_P1GBD_DET	M_GBD_OFF	M_GBB_ON
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
M_GBD_PKERR	7	GBD packet receive error occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBD_ACLR	6	GBD packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_P1GBD_CHG	5	P1 GBD update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_P0GBD_CHG	4	P0 GBD update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_P1GBD_DET	2	P1 GBD data receive detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBD_OFF	1	No Valid GBD detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBB_ON	0	With valid GBD detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.25. **MISC INTERRUPT MASK (MISC_INTM) (0x851b)**

	7	6	5	4	3	2	1	0
	M_AU_DSD_OFF	M_AU_HBR_OFF	M_VIDEO_COLOR	M_AS_LAYOUT	M_NO_SPD	M_NO_VS	M_SYNC_CHG	M_AUDIO_MUTE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	1	1	1	1	1	1

Register Field	Bit	Description
M_AU_DSD_OFF	7	Discontinuity of DSD Audio packet receive detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AU_HBR_OFF	6	Discontinuity of HBR Audio packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_VIDEO_COLOR	5	Mask for Video Color (RGB, YCbCr444, YCbCr422) change interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AS_LAYOUT	4	audio Layout Bit change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_SPD	3	SPD_Info packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_VS	2	VS_Info packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_SYNC_CHG	1	Video sync signal state change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AUDIO_MUTE	0	Audio MUTE generation interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

5.11.26. **SYS STATUS (SYS_STATUS) (0x8520)**

	7	6	5	4	3	2	1	0
	S_SYNC	S_AVMUTE	S_HDCP	S_HDMI	S_PHY_SCDT	S_PHY_PLL	S_TMDS	S_DDC5V
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_SYNC	7	Input Video sync signal status 0: No sync signal (unstable) 1: With sync signal (stable) Note: For the generation conditions for this status, follow the address0x85C5 to 0x85CD settings.
S_AVMUTE	6	AVMUTE status 0: AVMUTE=OFF 1: AVMUTE=ON
S_HDCP	5	HDCP status 0: HDCP=OFF (no code) 1: HDCP=ON (with code)
S_HDMI	4	HDMI status 0: DVI 1: HDMI
S_PHY_SCDT	3	PHY DE detect status (PHY SCDT signal monitor) 0: No DE 1: With DE
S_PHY_PLL	2	PHY PLL status (PHY PLL_LOCK_IND signal monitor) 0: UnLock 1: Lock
S_TMDS	1	TMDS input amplitude status (PHY squelch signal monitor) 0: No input amplitude 1: With input amplitude
S_DDC5V	0	DDC_Power (DDC5V) input status 0: No input 1: With input

5.11.27. **VIDEO INPUT STATUS (VI_STATUS) (0x8521)**

	7	6	5	4	3	2	1	0
	S_V_repeat				S_V_format			
Type	RO				RO			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_V_repeat	[7:4]	Input Video signal status (Repetition) 0: No Repetition 1: Repetition = 2 2: Repetition = 3 3: Repetition = 4 … 9: Repetition = 10
S_V_format	[3:0]	Video format status detected from input DE size *Shows the status before implementation of correction using repetition. 1: VGA (Horizontal 631 to 649, Vertical 471 to 489) 2: 240p/480i (Horizontal 1401 to 1449, Vertical 231 to 249) 3: 288p/576i (Horizontal 1401 to 1449, Vertical 279 to 297) 4: W240p/480i (Horizontal 2801 to 2899, Vertical 231 to 249) 5: W288p/576i (Horizontal 2801 to 2899, Vertical 279 to 297) 6: 480p (Horizontal 701 to 729, Vertical 471 to 489) 7: 576p (Horizontal 701 to 729, Vertical 567 to 585) 8: W480p (Horizontal 1401 to 1449, Vertical 471 to 489) 9: W576p (Horizontal 1401 to 1449, Vertical 567 to 585) 10: WW480p (Horizontal 2801 to 2899, Vertical 471 to 489) 11: WW576p (Horizontal 2801 to 2899, Vertical 567 to 585) 12: 720p (Horizontal 1261 to 1289, Vertical 711 to 729) 13: 1035i (Horizontal 1911 to 1929, Vertical 507 to 527) 14: 1080i (Horizontal 1911 to 1929, Vertical 531 to 549) 15: 1080p (Horizontal 1911 to 1929, Vertical 1071 to 1089) 0: Other than above

5.11.28. **VIDEO INPUT STATUS1 (VI_STATUS1) (0x8522)**

	7	6	5	4	3	2	1	0
	S_V_GBD	Reserved			S_DeepColor		S_V_422	S_V_interlace
Type	RO	RO			RO		RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_V_GBD	7	Effective GBD data status 0: No GBD 1: With GBD
S_DeepColor	[3:2]	Deep Color status 00: 24bit mode 01: 30bit mode 10: 36bit mode 11: 48bit mode Note: During DVI input, judged to be 24bit
S_V_422	1	Input Video signal status (422 detection) 0: 444 1: 422 Note: During DVI input, judged to be 444. During HDMI input, judged from the AVI-Info value.
S_V_interlace	0	Input Video signal status (Interlace detection) 0: Progressive 1: Interlace

5.11.29. **AUDIO STATUS0 (AU_STATUS0) (0x8523)**

	7	6	5	4	3	2	1	0
	S_A_MUTE	S_A_P_Lock	S_A_F_Lock	Reserved	S_A_DSD	S_A_HBR	S_A_NLPCM	S_A_sample
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_A_MUTE	7	AUDIO auto mute status 0: Mute OFF 1: Mute ON
S_A_P_Lock	6	AUDIO-PLL phase lock status 0: Unlock 1: Lock
S_A_F_Lock	5	AUDIO-PLL Frequency lock status 0: Unlock 1: Lock
S_A_DSD	3	1BIT Audio packet transmission status (1.5ms update) 0: No DSD transmission 1: With DSD transmission
S_A_HBR	2	HBR Audio packet transmission status (1.5ms update) 0: No HBR transmission 1: With HBR transmission
S_A_NLPCM	1	Normal AUDIO/HBR AUDIO packet compression stream detection 0: LPCM 1: Compression stream (61937-1)

Register Field	Bit	Description
S_A_sample	0	Normal AUDIO packet transmission status (1.5ms update) 0: No AUDIO transmission 1: With AUDIO transmission Note: When 1bit-audio is received, this bit is always 0.

5.11.30. **AUDIO STATUS1 (AU_STATUS1) (0x8524)**

	7	6	5	4	3	2	1	0
	3D_STRUCURE				S_VS	S_SPD	S_PKERR	S_ACP
Type	RO				RO	RO	RO	RO
Default	0				0	0	0	0

Register Field	Bit	Description
3D_STRUCURE	[7:4]	3D transmission format information in VS info 0000: Frame packing 0001 Field alternative 0010: Line alternative 0011: Side-by-Side(Full) 0100: L + depth 0101: L + depth + graphics + graphics-depth 0110: Top-and-Bottom 0111: Reserved 1000: Side-by-Side(Half) 1001 to 1110: Reserved 1111: Not used Note: Valid when S_VS_VIC_3D(0x8525[5]) is 1
S_VS	3	VS packet transmission status 0: No VS transmission 1: With VS transmission
S_SPD	2	SPD packet transmission status 0: No SPD transmission 1: With SPD transmission
S_PKERR	1	Packet receive error occurrence status 0: No Packet receive error 1: Packet receive error now occurring
S_ACP	0	ACP packet transmission status 0: No ACP transmission 1: With ACP transmission

5.11.31. **VIDEO INPUT STATUS2 (VI_STATUS2) (0x8525)**

	7	6	5	4	3	2	1	0
	S_FP_IP		S_VS_VIC_3D	Reserved				S_DC_NOCD
Type	RO		RO	RO				RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_FP_IP	[7:6]	IP judgment result 0x8980[2] due to size (Vertical V size and vertical DE size) or VIC to select whether to use size or VIC to judge. Valid during Frame packing receive. 0: Progressive 1: Interlace 2: VIC=39
S_VS_VIC_3D	5	3D format judgment result due to VS info * 0: Non-3D format 1: 3D format Note: Valid during HDMI input only. During DVI input, fixed at 0. When VS Info packet HDMI Video format(PB4 [7:5])= 3'b010, set o 1.
S_DC_NOCD	0	Status determining whether Color Depth used in current Deep Color unpack operation is in 24bit mode due to auto move 0: During normal operation (DVI mode or normal CD value) 1: CD=0 or CD=reserved or Operations due to No GC Packet

5.11.32. **CLK STATUS (CLK_STATUS) (0x8526)**

	7	6	5	4	3	2	1	0
	S_V_3D_format				S_V_HPOL	S_V_VPOL	S_CLK_U21M	S_CLK_DC
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_V_3D_format	[7:4]	3D Video format status detected from input DE size *1 1: 3D 1080i Frame Packing (Horizontal 1911 to 1929, Vertical 2219 to 2237) 2: 3D 1080p Frame Packing or L+depth (Horizontal 1911 to 1929, Vertical 2196 to 2214) 3: 3D 720p Frame Packing or L+depth (Horizontal 1271 to 1289, Vertical 1461 to 1479) 4: 3D 1080p Line alternative (Horizontal 1911 to 1929, Vertical 2151 to 2169) 5: 3D 720p Line alternative (Horizontal 1271 to 1289, Vertical 1431 to 1449) 6: 3D 1080i Side by Side(Full) (Horizontal 3831 to 3849, Vertical 531 to 549) 7: 3D 1080p Side by Side(Full) (Horizontal 3831 to 3849, Vertical 1071 to 1089) 8: 3D 720p Side by Side(Full) (Horizontal 2551 to 2569, Vertical 711 to 729) 9: 3D 1080p L+depth+G+G_depth (Horizontal 1911 to 1929, Vertical 4446 to 4464) 10: 3D 720p L+depth+G+G_depth (Horizontal 1271 to 1289, Vertical 2961 to 2979) 0: Other than above
S_V_HPOL	3	Input HSYNC polarity status 0: Low active 1: High active
S_V_VPOL	2	Input VSYNC polarity status 0: Low active 1: High active
S_CLK_U21M	1	TMDS clock detection status at less than 21 MHz 0: 21 MHz or more 1: Less than 21 MHz
S_CLK_DC	0	TMDS clock DC condition detection status 0: Non DC condition 1: DC condition Note: In reality, DC to frequency of about 1 MHz or less is “1”. Responds even when TMDS clock is not input (amplitude 0).

*1 3D 1080i Line alternative cannot identify 2D 1080p,
3D Side by Side (Half) cannot identify 2D format,
3D Top-and-Bottom cannot identify 2D format,
The above unidentifiable format is displayed as 4'd0.

5.11.33. **VI STATUS3 (VI_STATUS3) (0x8528)**

	7	6	5	4	3	2	1	0
	Reserved			S_V_color				
Type	RO			RO				
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
S_V_color	[4:0]	Input Video signal color space judgment status *1 00 000 RGB (Full) 00 001 RGB (Limited) 00 010 YCbCr601 (Full) 00 011 YCbCr601 (Limited) 00 110 YCbCr709 (Full) 00 111 YCbCr709 (Limited) 00 100 Adobe_RGB (Full) 00 101 Adobe_RGB (Limited) 01 010 xvYCC601 (Full) 01 011 xvYCC601 (Limited) 01 110 xvYCC709 (Full) 01 111 xvYCC709 (Limited) 10 010 sYCC601 (Full) 10 011 sYCC601 (Limited) 11 010 Adobe_YCC601 (Full) 11 011 Adobe_YCC601 (Limited) *Values other than above are not generated Note: Each bit has the following meaning. [0] Full/Limited identification bit [1] RGB/YCbCr identification bit [2] During RGB input, category identification bit During YCbCr input, 601/709 identification bit [4: 3] During RGB input, 00 fixed During YCbCr input, category identification bit

*1 During DVI input, judged as RGB. For range identification, follow the address0x8570[3]bit setting.

During HDMI input, judged from AVI-Info value. If at AVI-Info judged to be RGB, for the range identification follow the address0x8570[2]bit.

5.11.34. **SYS FREQ0 Register (SYS_FREQ0) (0x8540)**

	7	6	5	4	3	2	1	0
	SYS_FREQ0							
Type	R/W							
Default	0x88							

Register Field	Bit	Description
SYS_FREQ0	[7:0]	System clock frequency setting (lower bits) Set System clock frequency setting divide 10000 integer Ex. When system clock at 26 MHz, 2600 = 16'h0A28 When system clock at 27 MHz, 2700 = 16'h0A8C When system clock at 42 MHz, 4200 = 16'h1068 When system clock at 50 MHz, 4200 = 16'h1388

5.11.35. **SYS FREQ1 Register (SYS_FREQ1) (0x8541)**

	7	6	5	4	3	2	1	0
	SYS_FREQ1							
Type	R/W							
Default	0x13							

Register Field	Bit	Description
SYS_FREQ1	[7:0]	System clock frequency setting (upper bits)

5.11.36. **DDC CONTROL (DDC_CTL) (0x8543)**

	7	6	5	4	3	2	1	0
	Reserved					DDC_ ACTION	DDC5V_MODE	
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
DDC_ACTION	2	Selection of response method for DDC access from send side 0: DDC is active only while HotPLUG is being output 1: DDC is active when initialization completion INIT_END, 0x854A[0], is asserted
DDC5V_MODE	[1:0]	DDC5V_active detect delay setting To prevent chattering in the DDC5V input rising detection area, DDC5V is judged as avtime after a specified time from the rise detect point in time. 00: 0 ms 01: 50 ms 10: 100 ms 11: 200 ms Note: With this setting, the DDC5V detection interrupt, HOTPLUG automatic output, and PHY automatic power ON timing are all delayed.

5.11.37. **HPD Control Register (HPD_CTL) (0x8544)**

	7	6	5	4	3	2	1	0
	Reserved			HPD_CTL0	Reserved			HPD_OUT0
Type	RO			RW	RO			RW
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Description
HPD_CTL0	4	HOTPLUG output ON/OFF control mode 0: Host manual setting 1: DDC5V detection interlock
HPD_OUT0	0	HOTPLUT Output setting 0: HOTPLUG = “L” output 1: HOTPLUG = “H” output Note: When at DDC5V detection interlock setting, write is not valid. Become status monitor bit.

5.11.38. **INIT END REGISTER (INIT_END) (0x854A)**

	7	6	5	4	3	2	1	0
	Reserved							INIT_END
Type	RO							RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
INIT_END	0	Initialization completed flag After completion of all initialization settings, write “1” to this register. If 0x8544[4] = 1, HPDO is asserted only when INIT_END is asserted. If 0x8543[2] = 1, DDC is active only when INIT_END is asserted

5.11.39. **HDCP MODE Register (HDCP_MODE) (0x8560)**

	7	6	5	4	3	2	1	0
	Reserved						AuthMod	
Type	RO		RW	RW	RO	RW	RW	
Default	0	0	1	0	0	1	0	0

Register Field	Bit	Description
AuthMod	[1:0]	HDCP authentication mode setting 00: Automatic authentication mode 0 (for receiver) (Aksv_write → HDCP reset → Km' calculation → Ks', 0', R0' calculation) 01: Automatic authentication mode 1 (for repeater) (Aksv_write → HDCP reset → Km' calculation → Ks', M0', R0' calculation → V' calculation) 1x: Host command mode The HOST issues commands sequentially according to interrupts.

5.11.40. **HDCP COMMAND Register (HDCP_CMD) (0x8561)**

	7	6	5	4	3	2	1	0
	Reserved				ShaS	CalParam	CalKm	UnAuth
Type	RO				RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
ShaS	3	V' value calculation start command (After calculation completed, automatically clears) 1: Command issued
CalParam	2	Ks', M0', R0' calculation start command (After calculation completed, automatically clears) 1: Command issued Note: During Auto authorization mode (AUTHMOD_A=00 or 01), this command is invalid.
CalKm	1	Km calculation start command (After calculation completed, automatically clears) 1: Command issued Note: During Auto authorization mode (AUTHMOD_A=00 or 01), this command is invalid.
UnAuth	0	Unauthorized move command (automatic clear) 1: Command issued

5.11.41. **VIDEO MUTE REGISTER1 (V_MUTE1) (0x857A)**

	7	6	5	4	3	2	1	0
	Reserved		VAM_CLR_MODE		Reserved		VAM_SYNC_EN	VAM_DATA_EN
Type	RO		R/W		RO		R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
VAM_CLR_MODE	[5:4[	Clearing method selection of Video Auto Mute 00: Manual Clearing 01: Auto Clearing by mute-timer 1x: Auto Clearing by mute-timer & Vsync active edge
VAM_SYNC_EN	1	VD_o/HD_o/DE_o auto mute setting 0: auto mute OFF 1: auto mute ON by selected Factors in address 0x857B
VAM_DATA_EN	0	Y_o/CB_o/CR_o auto mute setting 0: auto mute OFF 1: auto mute ON by selected Factors in address 0x857B

5.11.42. **VIDEO MUTE REGISTER2 (V_MUTE2) (0x857B)**

	7	6	5	4	3	2	1	0
	Reserved	VAM_FACTOR6	VAM_FACTOR5	VAM_FACTOR4	VAM_FACTOR3	VAM_FACTOR2	VAM_FACTOR1	VAM_FACTOR0
Type	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	1	1	1	1	1	1

Register Field	Bit	Description
VAM_FACTOR6	6	When TMDS signal existence (PHY Squelch) change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR5	5	When DE size and position of Input side change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR4	4	When HV counter of Input side change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR3	3	When Deep Coloer mode change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR2	2	When Pixel CLK change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR1	1	When PHY PLL CLK Frequency change is detected, Video_Mute is set automatically. 0: Not set 1: Set
VAM_FACTOR0	0	When TMDS CLK change is detected, Video_Mute is set automatically. 0: Not set 1: Set

5.11.43. **VIDEO MUTE Timer REGISTER1 (VMUTE_TIMER) (0x857C)**

	7	6	5	4	3	2	1	0
	Video_mute_timer_Limit							
Type	R/W							
Default	0x14							

Register Field	Bit	Description
Video_mute_timer_Limit	[7:0]	Waiting time until Clearing of Video Mute status. 25.6 ms to 6553 ms. (set in 25.6 ms units) Note: Setting of 0 sec. (0x00) is prohibited

5.11.44. **VIDEO MUTE STATUS REGISTER (VMUTE_STATUS) (0x857D)**

	7	6	5	4	3	2	1	0
	Reserved			SYNC_MUTE_STATUS	Reserved			DATA_MUTE_STATUS
Type	RO			R/W	RO			R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
SYNC_MUTE_STATUS	4	Video SYNC (VD_o/HD_o/DE_o) auto mute status 0: Mute OFF (VD_o/HD_o/DE_o = Normal output) 1: Mute ON (VD_o/HD_o/DE_o = Logic"L") Note: Only in the case of VAM_CLR_MODE = 2'b00, Host can write "0". HOST always cannot write "1."
DATA_MUTE_STATUS	0	Video DATA (Y_o/CB_o/CR_o) auto mute status 0: Mute OFF (Y_o/CB_o/CR_o = Normal output) 1: Mute ON (Y_o/CB_o/CR_o = Black) Note: Only in the case of VAM_CLR_MODE = 2'b00, Host can write "0". HOST always cannot write "1."

5.11.45. **VIDEO MUTE AUTO REGISTER2 (VMUTE_AUTO) (0x857F)**

	7	6	5	4	3	2	1	0
	AUTO_VI_MUTE1	AUTO_VI_MUTE0	Reserved	VI_MUTE	Reserved			VI_BLACK
Type	R/W	R/W	R	R/W	RO			RW
Default	1	1	0	0	0	0	0	0

Register Field	Bit	Description
AUTO_VI_MUTE1	7	Auto mute of HD_o/VD_o/DE_o when No TMDS (PHY Squelch) detected 0: No Mute 1: Mute **Note: Use the initial value.**
AUTO_VI_MUTE0	6	Auto mute of HD_o/VD_o/DE_o when No DDC5V detected 0: No Mute 1: Mute **Note: Use the initial value.**
VI_MUTE	4	Manual Mute setup of HD_o/VD_o/DE_o 0: OFF (Normal) 1: Mute (HD_o/VD_o/DE_o “0” fixed) Note: HOST always can write "1" or "0".
VI_BLACK	0	Manual Black screen output setup 0: OFF (Normal) 1: Black screen output Note: HOST always can write "1" or "0".

5.11.46. **Input DE Horizontal Start REGISTER (DE_STR) (0x8580)**

	7	6	5	4	3	2	1	0
	DE_HStart [7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_HStart[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_HStart	[12:0]	Input DE horizontal start position

5.11.47. **Input DE Horizontal Size REGISTER (DE_HSize) (0x8582)**

	7	6	5	4	3	2	1	0
	DE_HSize [7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_HSize [12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_HSize	[12:0]	Input DE horizontal Size

5.11.48. **Input DE Vertical Start Position A REGISTER (DE_VStartA) (0x8584)**

	7	6	5	4	3	2	1	0
	DE_VStartA[7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_VStartA[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_VStartA	[12:0]	During Field alternative input →Input L image Top field effective period start position measurement result During Frame packing for interlaced format input → Input L image Top field (odd) effective period start position measurement result During Interlace format input other than above → Input Top field effective period start position measurement result During Progressive format input other than above → Input effective period start position measurement result

5.11.49. **Input DE Vertical Start Position B REGISTER (DE_VStartB) (0x8586)**

	7	6	5	4	3	2	1	0
	DE_VStartB[7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_VStartB[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_VStartB	[12:0]	During Field alternative input → Input L image Bottom field effective period start position measurement result During Frame packing for interlaced format input → Equivalent to DE_ VStartA During Interlace format input other than above → Input Bottom field effective period start position measurement result During Progressive format input other than above → Equivalent to DE_ VStartA

5.11.50. **Input DE Vertical Start Position C REGISTER (DE_VStartC) (0x8588)**

	7	6	5	4	3	2	1	0
	DE_VStartC[7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_VStartC[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_VStartC	[12:0]	During Field alternative format input →Input R image Top field valid start line measurement result Other than above, during Interlace format input →Input equal to Top field valid image start position (DE_VStartA) During Progressive input →Equal to DE_VStartA

5.11.51. **Input DE Vertical Start Position D REGISTER (DE_VStartD) (0x858A)**

	7	6	5	4	3	2	1	0
	DE_VStartD[7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_VStartD[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_VStartD	[12:0]	During Field alternative format input →Input R image Bottom field valid start line measurement result Other than above, during Interlace format input →Input equal to Bottom field valid image start position lower (DE_VStartB) During Progressive input →Equal to DE_VStartA

5.11.52. **Input DE Vertical Size REGISTER (DE_VSize) (0x858C)**

	7	6	5	4	3	2	1	0
	DE_VSize [7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			DE_VSize[12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
DE_VSize	[12:0]	Input DE vertical size measurement result Note: Line number for 1 valid rectangular region in 1V period (including active space) Note: Multiple valid regions linked in active space are measured as 1 valid rectangular region. Note: If multiple valid rectangular regions exist in the vertical direction in 1V period, like the Field alternative, it is displayed as line number for 1 valid rectangular region.

5.11.53. **Input Horizontal Size REGISTER (IN_HSize) (0x858E)**

	7	6	5	4	3	2	1	0
	IN_HSize[7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved			IN_HSize [12:8]				
Type	RO			RO				
Default	0	0	0	X	X	X	X	X

Register Field	Bit	Description
IN_HSize	[12:0]	Input horizontal Size

5.11.54. **Input Vertical Size REGISTER (IN_VSize) (0x8590)**

	7	6	5	4	3	2	1	0
	IN_VSize [7:0]							
Type	RO							
Default	X	X	X	X	X	X	X	X

	7	6	5	4	3	2	1	0
	Reserved		IN_VSize[13:8]					
Type	RO		RO					
Default	0	0	X	X	X	X	X	X

Register Field	Bit	Description
IN_VSize	[13:0]	Input vertical size measurement result Note: 2V period line number measurement result

5.11.55. **Input HV Measurement Clear REGISTER (HV_CLR) (0x8593)**

	7	6	5	4	3	2	1	0
	HOLD	Reserved	DEV_CLR	DEH_CLR	Reserved		V_CLR	H_CLR
Type	R/W	RO	R/W	R/W	RO		R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
HOLD	7	Input measurement value Hold command While this bit is set up at “1”, the input measurement count value Holds. Command clear is performed by the HOST. Note: Counter value clear command takes precedence
DEV_CLR	5	Input DE_V size, DE_V position measurement result register clear command 1: Clear Note: Command register is automatically cleared. Note: After clear is performed, a maximum of 2V period is required until the next measurement result is obtained
DEH_CLR	4	Input DE_H size, DE_H position measurement result register clear command 1: Clear Note: Command register is automatically cleared.
V_CLR	1	Input V size measurement result register clear command 1: Clear Note: Command register is automatically cleared. Note: After clear is performed, a maximum of 2V period is required until the next measurement result is obtained
H_CLR	0	Input H size measurement result register clear command 1: Clear Note: Command register is automatically cleared.

5.11.56. **HV Status REGISTER (HV_STATUS) (0x85C5)**

	7	6	5	4	3	2	1	0
	Reserved		M_HV_STATUS		Reserved		S_H_RAMG	S_V_RANG
Type	RO		R/W		RO		RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
M_HV_STATUS	[5:4]	Mask factors not used in generation of HV presence status (address0x05_20[7]bit) [5]bit= S_H_RANG mask, [4]bit= S_V_RANG mask 0: Mask OFF, 1: Mask ON Note) If both masks are OFF, S_H_RANG and S_V_RANG are AND. If both masks are ON, address0x05_20[7]bit is always “1”.
S_H_RANG	1	H cycle (FH_CNT value) absolute value 0: Outside allowed range, 1: Within allowed range
S_V_RANG	0	V cycle (FV_CNT val;ue) absolute value 0: Outside allowed range, 1: Within allowed range

5.11.57. **Vertical Range MIN REGISTER (FV_MIN) (0x85C6)**

	7	6	5	4	3	2	1	0
	FV_MIN[7:0]							
Type	R/W							
Default	0	0	1	0	1	0	0	0

	7	6	5	4	3	2	1	0
	Reserved						FV_MIN[9:8]	
Type	RO						R/W	
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
FV_MIN	[9:0]	S_V_RANG generation conditions: Allowed FV_CNT (Vsync cycle) minimum value is Setting value (FV_MIN) * 100µsec (Initial value=4ms) ex) When field rate is 120Hz Vsync cycle is 8.33ms. 8.33ms / 100µs = 83.3. Therefore, FV_MIN must be less than 83 (0x53) if HDMIRX IP allows receiving video format that field rate is 120Hz. Note) Set marginal value because mesurement value of Vsync cycle includes measurement error.

5.11.58. **Vertical Range MAX REGISTER (FV_MAX) (0x85C8)**

	7	6	5	4	3	2	1	0
	FV_MAX[7:0]							
Type	R/W							
Default	1	1	0	0	0	0	1	0

	7	6	5	4	3	2	1	0
	Reserved						FV_MAX [9:8]	
Type	RO						R/W	
Default	0	0	0	0	0	0	0	1

Register Field	Bit	Description
FV_MAX	[9:0]	S_V_RANG generation conditions: Allowed FV_CNT (Vsync cycle) maximum value is Setting value (FV_MAX) * 100µsec (Initial value=45ms) ex) When field rate is 24Hz Vsync cycle is 41.67ms. 41.67ms / 100µs = 416.7. Therefore, FV_MAX must be more than 417 (0x1A1) if HDMIRX IP allows receiving video format that field rate is 24Hz. Note) Set marginal value because mesurement value of Vsync cycle includes measurement error.

5.11.59. **Horizontal Range MIN REGISTER (FH_MIN) (0x85CA)**

	7	6	5	4	3	2	1	0
	FH_MIN [7:0]							
Type	R/W							
Default	1	0	0	1	0	1	1	0

	7	6	5	4	3	2	1	0
	FH_MIN [15:8]							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
FH_MIN	[15:0]	S_H_RANG generation conditions: Allowed FH_CNT (Hsync cycle) minimum value is Setting value (FH_MIN) * CLK_SYSTEM Cycle(20ns) Note) Initial value=3μs when CLK_SYSTEM cycle is 20ns. ex) When video format is 1080p@60Hz Hsync cycle is 14.815μs. 14.815μs / 20ns = 740.75. Therefore, FH_MIN must be less than 740(0x2E4) if HDMIRX IP allows receiving 1080p@60Hz. Note) Set marginal value because mesurement value of Hsync cycle includes measurement error.

5.11.60. **Horizontal Range MAX REGISTER (FH_MAX) (0x85CC)**

	7	6	5	4	3	2	1	0
	FH_MAX [7:0]							
Type	R/W							
Default	1	1	1	0	0	1	0	0

	7	6	5	4	3	2	1	0
	FH_MAX [15:8]							
Type	R/W							
Default	0	0	0	0	1	1	0	0

Register Field	Bit	Description
FH_MAX	[15:0]	S_H_RANG generation conditions: Allowed FH_CNT (Hsync cycle) maximum value is Setting value (FH_MAX) * CLK_SYSTEM Cycle(20ns) Note) Initial value=66μs when CLK_SYSTEM cycle is 20ns. ex) When video format is 576i@50Hz Hsync cycle is 64.0μs. 64.0μs / 20ns = 3200. Therefore, FH_MAX must be more than 3200(0xC80) if HDMIRX IP allows receiving 576i@50Hz. Note) Set marginal value because mesurement value of Hsync cycle includes measurement error.

5.11.61. **EDID MODE REGISTER (EDID_MODE) (0x85E0)**

	7	6	5	4	3	2	1	0
	Reserved						EDID_MODE	
Type	RO						R/W	
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
EDID_MODE	[1:0]	EDID access response mode selection 00: DDC line direct connection EEPROM mode (Absolutely no response to EDID access from DDC line) 01: Internal EDID-RAM & DDC2B mode (No response to 0x60slave =>Returns NACK) 1x: Internal EDID-RAM & E-DDC mode

5.11.62. **EDID Length REGISTER 1 (EDID_LEN1) (0x85E3)**

	7	6	5	4	3	2	1	0
	EDID_LEN[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
EDID_LEN[7:0]	[7:0]	EDID data size stored in RAM Note: Sets Data byte number Read from EEPROM Note: If EDID_LEN[10:0]=0 is set, no read Note: if EDID_LEN[10:0]>0x400 (1024 or more) is set, 1024 bytes only are Read Note: If EEPROM not used, and data is written directly to RAM from HOST, data size is set.

5.11.63. **EDID Length REGISTER 2 (EDID_LEN2) (0x85E4)**

	7	6	5	4	3	2	1	0
	Reserved					EDID_LEN[10:8]		
Type	RO					R/W		
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
EDID_LEN[10:8]	[2:0]	EDID data size stored in RAM (upper address bits)

5.12. HDMI Rx Audio Control

5.12.1. **FORCE MUTE (FORCE_MUTE) (0x8600)**

	7	6	5	4	3	2	1	0
	Reserved			FORCE_AMUTE	Reserved			FORCE_DMUTE
Type	RO			R/W	RO			R/W
Default	0	0	0	1	0	0	0	1

Register Field	Bit	Description
FORCE_AMUTE	4	Forced AMUTEOUT terminal control 0: Mute OFF 1: Mute ON Note: Setting and clear is possible at HOST only Note: For Mute ON polarity, follow the 0x8608[5] setting
FORCE_DMUTE	0	Forced data MUTE control 0: Mute OFF 1: Mute ON Note: Setting and clear is possible at HOST only Note: For Mute signal, follow the 0x8608[2:0] setting

5.12.2. **CMD AUD (CMD_AUD) (0x8601)**

	7	6	5	4	3	2	1	0
	Reserved					CMD_BUFINIT	CMD_LOCKDET	CMD_MUTE
Type	RO					R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CMD_BUFINIT	2	Buffer initialization start command 1: Command issued Note: After buffer initialization completed, automatically clears Note: When in automatic command issue mode (address0x8604[2:1]≠ 2'b00), issue of commands from HOST is prohibited. Note: When issuing commands from HOST, always issue the MUTE start command first.
CMD_LOCKDET	1	Audio clock frequency lock detection start command 1: Command issued Note: The reproduced Audio clock frequency detects unification with FS information transmitted by Cannel Status bit, and issues interrupt. For observation cycle and detection precision, follow the address 0x8630 to 33 setting. Note: After frequency lock detection, automatically clears * Use not recommended
CMD_MUTE	0	MUTE start command 1: Command issued Note: Automatic command issue mode exists. For automatic issue condition, follow the AUTO_CMD0,1(address0x8602, 0x8603) setting. Note: When AUTO_PLAY3 setting ON, automatically clears to "0” when Buffer initialization completed. Note: For Mute signal, follow the 0x8608[2:0] setting Note: For AMUTE terminal output polarity, follow the 0x8608[5] setting

5.12.3. **AUDIO AUTO MUTE Command REGISTER (AMute_Auto) (0x8602)**

	7	6	5	4	3	2	1	0
	Auto_ Mute7	Auto_ Mute6	Auto_ Mute5	Auto_ Mute4	Auto_ Mute3	Auto_ Mute2	Auto_ Mute1	Auto_ Mute0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	0	0	1	1

Register Field	Bit	Description
Auto_Mute7	7	In PHY-A/B switch, automatically set CMD_MUTE 0: Not set 1: Set
Auto_Mute6	6	In LPCM/NLPCM change detection, automatically set CMD_MUTE 0: Not set 1: Set Note: OR conditions for LPCM→NLPCM detect and NLPCM→LPCM detect
Auto_Mute5	5	In FS change detection, automatically set CMD_MUTE 0: Not set 1: Set
Auto_Mute4	4	In PHY output clock change detection, automatically set CMD_MUTE 0: Not set 1: Set
Auto_Mute3	3	In Non LPCM detection period, automatically set CMD_MUTE 0: Not set 1: Set
Auto_Mute2	2	In Audio clock frequency unlock detect period, automatically set CMD_MUTE 0: Not set 1: Set *Use not recommended
Auto_Mute1	1	In PHY no output clock detect period, automatically set CMD_MUTE 0: Not set 1: Set
Auto_Mute0	0	In DVI mode period, or in DDC5V =0V period, automatically set CMD_MUTE 0: Not set 1: Set

5.12.4. **Auto Command REGISTER 0 (AUTO_CMD1) (0x8603)**

	7	6	5	4	3	2	1	0
	Reserved					Auto_ Mute10	Auto_ Mute9	Auto_ Mute8
Type	RO					R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
Auto_Mute10	2	In 60958 frame discontinuous detect, automatically issue CMD_MUTE 0: Not issue 1: Issue
Auto_Mute9	1	In SET_AVMUTE receive period, automatically issue CMD_MUTE 0: Not issue 1: Issue
Auto_Mute8	0	In buffer flow detect, automatically issue CMD_MUTE 0: Not issue 1: Issue

5.12.5. **Auto Command REGISTER 0 (AUTO_CMD2) (0x8604)**

	7	6	5	4	3	2	1	0
	Reserved				Auto_ Play3	Auto_ Play2	Reserved	
Type	RO				R/W	R/W	RO	
Default	0	0	0	0	1	1	0	0

Register Field	Bit	Description
Auto_Play3	3	In Buffer initialization end detect, automatically clears MUTE_CMD 0: Not clear 1: Clear
Auto_Play2	2	After generation of MUTE factor selected in AUTO_MUTE setting “after fixed time B” automatically issue CMD_BUFINIT 0: Not issue 1: Issue Note: Priority over frequency lock detect (=equivalent to lock detect time limit) Note: If MUTE factor continues for fixed period, issue command at end edge of factor. Note: If MUTE factor is generated during fixed time measurement, restart time measurement from beginning.

5.12.6. **Buffer Initialization Start Period (BUFINIT_START) (0x8606)**

	7	6	5	4	3	2	1	0
	BUFINIT_START							
Type	R/W							
Default	0x05							

Register Field	Bit	Description
BUFINIT_START	[7:0]	Wait time setting until Buffer initialization start in AUTO_PLAY2 →“fixed time B” 0.1 to 25.5sec. (set in 0.1 sec. units) Note: Setting of 0 sec. (0x00) is prohibited

5.12.7. **FS MUTE REGISTER (FS_MUTE) (0x8607)**

	7	6	5	4	3	2	1	0
	FS_else_MUTE	FS22_MUTE	FS24_MUTE	FS88_MUTE	FS96_MUTE	FS176_MUTE	FS192_MUTE	FS_NO_MUTE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
FS_else_MUTE	7	Other than FS = 22k,24k,32k,44k,48k,88k,96,176k,192k 0: Do not Mute 1: Mute
FS22_MUTE	6	When at FS = 22.05 kHz, routinely 0: Do not Mute 1: Mute
FS24_MUTE	5	When at FS = 24 kHz, routinely 0: Do not Mute 1: Mute
FS88_MUTE	4	When at FS = 88.2 kHz, routinely 0: Do not Mute 1: Mute
FS96_MUTE	3	When at FS = 96 kHz, routinely 0: Do not Mute 1: Mute
FS176_MUTE	2	When at FS = 176.4 kHz, routinely 0: Do not Mute 1: Mute
FS192_MUTE	1	When at FS = 192 kHz, routinely 0: Do not Mute 1: Mute
FS_NO_MUTE	0	When at FS = not indicated, routinely 0: Do not Mute 1: Mute

Write FS Bit corresponding to set specification to ”0”.

FS=48 kHz, 44.1 kHz, 32 kHz are outside FS_MUTE applicability. (In the standard, 48 kHz, 44.1 kHz, 32 kHz must be reproduced)

5.12.8. **AUDIO MUTE MODE REGISTER (MUTE_MODE) (0x8608)**

	7	6	5	4	3	2	1	0
	AMUTE_DLY		AMUTE_ POL	O_AMUTE_ EN	Reserved	MUTE_ LRCK	MUTE_ BCK	MUTE_ SDO
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Default	0	1	1	1	0	0	0	1

Register Field	Bit	Description
AMUTE_DLY	[7:6]	When MUTE cleared, AMUTE output delay adjustment (*2) 00: No delay 01: 100ms delay 10: 200ms delay 11: 300ms delay
AMUTE_POL	5	AMUTE polarity (*1) 0: ”0” output 1: ”1” output
O_AMUTE_EN	4	AMUTE signal ON/OFF when MUTE ON (*1) 0: OFF (”0” output fixed) 1: ON
MUTE_LRCK	2	LRCK output when MUTE ON (*1) 0: Do not Mute 1: Mute
MUTE_BCK	1	BCK output when MUTE ON (*1) 0: Do not Mute 1: Mute
MUTE_SDO	0	SDO/DADO output when MUTE ON (*1) 0: Do not Mute 1: Mute

*1 Actually setting to MUTE ON occurs when any of the following items occur.
When HOST sets FORCE_MUTE (address0x8600)
When HOST sets CMD_MUTE (address0x8601[0])
When factor selected in AUTO_MUTE (address0x8602 to 0x8603) is generated
When other than FS received in FS_MUTE(address0x8607) is selected

*2 If using AMUTEOUT to perform transistor mute at set output stage, this setting can also be used to delay the Mute clear timing.

5.12.9. **AUDIO LAYOUT MONITOR REGISTER (LAYOUT_MONI) (0x861A)**

	7	6	5	4	3	2	1	0
	Reserved			MONI_LAYOUT	MONI_PR			
Type	R			R	R			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MONI_LAYOUT	4	Layout bit monitor 0: Layout = 0 1: Layout = 1
MONI_PR	[3:0]	Present bit monitor [3] Sub packet 3 PR bit [2] Sub packet 2 PR bit [1] Sub packet 1 PR bit [0] Sub packet 0 PR bit Note) When Layout0, Read value is not reliable

5.12.10. **AUDIO SAMPLE FREQUENCY MODE REGISTER (FS_SET) (0x8621)**

	7	6	5	4	3	2	1	0
	Reserved			NLPCM	FS			
Type	R/W			R/W	R/W			
Default	0	0	0	0	0x2			

Register Field	Bit	Description
NLPCM	4	Normal Audio linear PCM/nonlinear PCM identification information extraction result 0: LPCM 1: Compression stream Note: When 0x8620[6]==0, Follow the 0x8620[5:4] setting, and HW automatically set, write from Host is invalid. If 0x8620[6]==1, HOST determines and sets. Note: LPCM/NLPCM change interrupt (address0x8505[3:2]) is generated when this register has a change.
FS	[3:0]	AUDIO sampling frequency information extraction result 4'h0: 44.1 kHz 4'h2: 48 kHz 4'h3: 32 kHz 4'h4: 22.05 kHz 4'h6: 24 kHz 4'h8: 88.2 kHz 4'hA: 96 kHz 4'hC: 176.4 kHz 4'hE: 192 kHz **4'h9: 768 kHz** **4'h5: 384 kHz** **4'h7: 352.8 kHz** **4'hB: 705.6 kHz** Note: If 0x08620[3]==0, Follow 0x8620[2:0] setting, HW is automatically set, write from Host is invalid. If 0x8620[3]==1, Host determines and sets. Note: FS change interrupt (address0x08505[1]) is generated when this register has a change.

5.12.11. **CBIT Byte 0 (CBIT_BYTE0) (0x8622)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE0							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE0	[7:0]	Channel Status bit [7:0]

5.12.12. **CBIT Byte 1 (CBIT_BYTE1) (0x8623)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE1							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE1	[7:0]	Channel Status bit [15:8]

5.12.13. **CBIT Byte 2 (CBIT_BYTE2) (0x8624)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE2							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE2	[7:0]	Channel Status bit [23:16]

5.12.14. **CBIT Byte 3 (CBIT_BYTE3) (0x8625)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE3							
Type	R/W							
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
CBIT_BYTE3	[7:0]	Channel Status bit [31:24]

5.12.15. **CBIT Byte 4 (CBIT_BYTE4) (0x8626)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE4							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE4	[7:0]	Channel Status bit [39:32]

5.12.16. **CBIT Byte 5 (CBIT_BYTE5) (0x8627)**

	7	6	5	4	3	2	1	0
	CBIT_BYTE5							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE5	[7:0]	Channel Status bit [47:40]

5.12.17. **Audio Sample Counter Register 0 (Audio_Counter0) (0x862E)**

	7	6	5	4	3	2	1	0
	AS_COUNT0							
Type	RO							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
AS_COUNT0	[7:0]	Audio sample count measurement result during 100 ms

5.12.18. **Audio Sample Counter Register 1 (Audio_Counter1) (0x862F)**

	7	6	5	4	3	2	1	0
	AS_COUNT1							
Type	RO							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
AS_COUNT1	[7:0]	Audio sample count measurement result during 100 ms

5.12.19. **Audio System Frequency Register A (LOCK_REF_FREQA-C) (0x8630)**

	7	6	5	4	3	2	1	0
	LOCK_REF_FREQ[7:0]							
Type	RO							
Default	0	0	1	0	0	0	0	0

Register Field	Bit	Description
LOCK_REF_FREQ[7:0]	[7:0]	System clock (=CLK_SYSTEM) frequency setting. Set system clock frequency setting ÷100 integer Ex.) When system clock at 42MHz, 4200 =16'h1068

5.12.20. **Audio System Frequency Register A (LOCK_REF_FREQA-C) (0x8631)**

	7	6	5	4	3	2	1	0
	LOCK_REF_FREQ[15:8]							
Type	RO							
Default	1	0	1	0	0	0	0	1

Register Field	Bit	Description
LOCK_REF_FREQ[15:8]	[7:0]	System clock (=CLK_SYSTEM) frequency setting. Set system clock frequency setting ÷100 integer Ex.) When system clock at 42MHz, 4200 =16'h1068

5.12.21. **Audio System Frequency Register A (LOCK_REF_FREQA-C) (0x8632)**

	7	6	5	4	3	2	1	0
	Reserved				LOCK_REF_FREQ[19:16]			
Type	R				RW			
Default	0	0	0	1	0	1	1	1

Register Field	Bit	Description

LOCK_REF_FREQ[19:16]	[3:0]	System clock (=CLK_SYSTEM) frequency setting. Set system clock frequency setting ÷100 integer Ex.) When system clock at 42MHz, 4200 =16'h1068

5.12.22. **AUDIO OUTPUT MODE 0 Register (SDO_MODE0) (0x8651)**

	7	6	5	4	3	2	1	0
	Reserved					BCK_POL	BCK_FS	LR_POL
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
BCK_POL	2	BCK polarity selection 0: Normal (ASDO data changed at down edge) 1: Inverted (ASDO data changed at up edge)
BCK_FS	1	BCK frequency selection 0: 32fs 1: 64fs
LR_POL	0	LRCK polarity selection 0: Normal (sample period: 1st half=L, 2nd half = H) 1: Inverted (sample period: 1st half = H, 2nd half = L)

5.12.23. **AUDIO OUTPUT MODE 1 Register (SDO_MODE1) (0x8652)**

	7	6	5	4	3	2	1	0
	Reserved	SDO_BIT_LENG			HBR_OUT_MODE	I2S_MODE	SDO_FMT	
Type	RO	R/W			R/W	R/W	R/W	
Default	0	1	1	0	0	0	1	0

Register Field	Bit	Description
SDO_BIT_LENG	[6:4]	ASDO output data Bit Length setting 000: 16bit (lower 8bit discarded) 001: 16bit (lower 8bit + 1 discarded) 010: 18bit (lower 6bit discarded) 011: 18bit (lower 6bit + 1 discarded) 100: 20bit (lower 4bit discarded) 101: 20bit (lower 4bit + 1 discarded) 110: 24bit no rounding 111: Output OFF (Mute)
HBR_OUT_MODE	3	HBR Audio output format setting 0: HBR output which uses only ASDO[0]. LRCK = 768 kHz 1: HBR output which uses ASDO[3:0], LRCL = 768 kHz/4 = 192 kHz
I2S_MODE	2	ASDO output format setting 3'b000: standard Back(Right) justified 3'b001: standard Front(Left) justified 3'b01x: standard I2S 3'b10x: Reserved 3'b11x: Reserved
SDO_FMT	[1:0]	

5.12.24. **AUDIO PLL Setting Register (NCO_F0_MOD) (0x8670)**

	7	6	5	4	3	2	1	0
	Reserved						NCO_F0_MOD	
Type	RO						R/W	
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
NCO_F0_MOD	[1:0]	NCO standard frequency setting for Audio PLL 00: For REFCLK = 42 MHz 01: Reserved 1x: Register setting value uses 28-bit setting for 48 kHz series use, for 44.1 kHz series use. (address 0x8671 to 78) Note: NCO standard frequency setting value calculation 48 kHz series: 6.144 MHz × 2^28 ÷ (RefClk frequency) 44.1 kHz series: 5.6448 MHz × 2^28 ÷ (RefClk clock frequency) 2'b01 should be not used. (system clock = min 40 MHz)

5.12.25. **AUDIO PLL Setting Register (NCO_48F0A) (0x8671)**

	7	6	5	4	3	2	1	0
	NCO_48F0[7:0]							
Type	R/W							
Default	0x05							

Set 6.144 MHz × 2^28 ÷ **REFCLK**

5.12.26. **AUDIO PLL Setting Register (NCO_48F0B) (0x8672)**

	7	6	5	4	3	2	1	0
	NCO_48F0[15:8]							
Type	R/W							
Default	0x51							

Set 6.144 MHz × 2^28 ÷ **REFCLK**

5.12.27. **AUDIO PLL Setting Register (NCO_48F0C) (0x8673)**

	7	6	5	4	3	2	1	0
	NCO_48F0[23:16]							
Type	R/W							
Default	0xF7							

Set 6.144 MHz × 2^28 ÷ **REFCLK**

5.12.28. **AUDIO PLL Setting Register (NCO_48F0D) (0x8674)**

	7	6	5	4	3	2	1	0
	Reserved				NCO_48F0[27:24]			
Type	RO				R/W			
Default	0	0	0	0	0	0	0	1

Set 6.144 MHz × 2^28 ÷ **REFCLK**

5.12.29. **AUDIO PLL Setting Register (NCO_44F0A) (0x8675)**

	7	6	5	4	3	2	1	0
	NCO_44F0[7:0]							
Type	R/W							
Default	0x09							

Set 5.6448 MHz × 2^28 ÷ **REFCLK**

5.12.30. **AUDIO PLL Setting Register (NCO_44F0B) (0x8676)**

	7	6	5	4	3	2	1	0
	NCO_44F0[15:8]							
Type	R/W							
Default	0x6C							

Set 5.6448 MHz × 2^28 ÷ **REFCLK**

5.12.31. **AUDIO PLL Setting Register (NCO_44F0C) (0x8677)**

	7	6	5	4	3	2	1	0
	NCO_44F0[23:16]							
Type	R/W							
Default	0xCE							

Set 5.6448 MHz × 2^28 ÷ **REFCLK**

5.12.32. **AUDIO PLL Setting Register (NCO_44F0D) (0x8678)**

	7	6	5	4	3	2	1	0
	Reserved				NCO_44F0[27:24]			
Type	RO				R/W			
Default	0	0	0	0	0	0	0	1

Set 5.6448 MHz × 2^28 ÷ **REFCLK**

5.12.33. **Audio Mode Register (Aud_mode) (0x8680)**

	7	6	5	4	3	2	1	0
	Reserved						Ex_Audio	
Type	RO						R/W	
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Ex_Audio	[1:0]	AUDIO replay packet selection 00: Normal Audio (packet typ. = 0x02) 01: HBR Audio (packet typ. = 0x09) → high bitrate audio stream 1x: DSD Audio

5.12.34. **Audio Pin Control 0 REGISTER (AOUTSEL0) (0x8690)**

	7	6	5	4	3	2	1	0
	Reserved		ALRSEL		ABCKSEL		AMCKSEL	
Type	R/W		R/W		R/W		R/W	
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
ALRSEL	[5:4]	LRCK (module) terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal
ABCKSEL	[3:2]	BMCK (module) terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal
AMCKSEL	[1:0]	AMCK (module) terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal

5.12.35. **Audio Pin Control 1 REGISTER (AOUTSEL1) (0x8691)**

	7	6	5	4	3	2	1	0
	AOUT3SEL		AOUT2SEL		AOUT1SEL		AOUT0SEL	
Type	R/W		R/W		R/W		R/W	
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
AOUT3SEL	[7:6]	ASDO3 terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal
AOUT2SEL	[5:4]	ASDO2 terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal
AOUT1SEL	[3:2]	ASOD1 terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal
AOUT0SEL	[1:0]	ASDO0 terminal control 2'b00: Normal 2'b01: Low fixed 2'b10: High fixed 2'b11: Normal

5.13. HDMI Rx InfoFrame Data

5.13.1. **Clear InfoFrame Packet Register (CLR_INFO) (0x8700)**

	7	6	5	4	3	2	1	0
	ISRC2_CLR	ISRC1_CLR	ACP_CLR	VS_CLR	SPD_CLR	MS_CLR	AUD_CLR	AVI_CLR
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
ISRC2_CLR	7	All-zero clear command for ISRC2(ETC) packet data When this bit is set to 1, Address 0x87D0 to 0x87EE are cleared to All-zero.
ISRC1_CLR	6	All-zero clear command for ISRC1 packet data When this bit is set to 1, Address 0x87B0 to 0x87C2 are cleared to All-zero.
ACP_CLR	5	All-zero clear command for ACP packet data When this bit is set to 1, Address 0x8790 to 0x87AE are cleared to All-zero.
VS_CLR	4	All-zero clear command for VS_info packet data When this bit is set to 1, Address 0x8770 to 0x878E are cleared to All-zero.
SPD_CLR	3	All-zero clear command for SPD_info packet data When this bit is set to 1, Address 0x8750 to 0x876E are cleared to All-zero.
MS_CLR	2	All-zero clear command for MS_info packet data When this bit is set to 1, Address 0x8740 to 0x874D are cleared to All-zero.
AUD_CLR	1	All-zero clear command for AUD_info packet data When this bit is set to 1, Address 0x8730 to 0x873D are cleared to All-zero.
AVI_CLR	0	All-zero clear command for AVI_info packet data When this bit is set to 1, Address 0x8710 to 0x8723 are cleared to All-zero.

5.13.2. **VS INFO PACKET TYPE CODE SETTING (TYP_VS_SET) (0x8701)**

	7	6	5	4	3	2	1	0
	TYP_VS_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_VS_SET	[7:0]	VS_info Packet Type code setting

5.13.3. **AVI INFO PACKET TYPE CODE SETTING (TYP_AVI_SET) (0x8702)**

	7	6	5	4	3	2	1	0
	TYP_AVI_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_AVI_SET	[7:0]	AVI_info Packet Type code setting

5.13.4. **SPD INFO PACKET TYPE CODE SETTING (TYP_SPD_SET) (0x8703)**

	7	6	5	4	3	2	1	0
	TYP_SPD_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_SPD_SET	[7:0]	SPD_info Packet Type code setting

5.13.5. **AUD INFO PACKET TYPE CODE SETTING (TYP_AUD_SET) (0x8704)**

	7	6	5	4	3	2	1	0
	TYP_AUD_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_AUD_SET	[7:0]	AUD_info Packet Type code setting

5.13.6. **MS INFO PACKET TYPE CODE SETTING (TYP_MS_SET) (0x8705)**

	7	6	5	4	3	2	1	0
	TYP_MS_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_MS_SET	[7:0]	MS_info Packet Type code setting

5.13.7. **ACP INFO PACKET TYPE CODE SETTING (TYP_ACP_SET) (0x8706)**

	7	6	5	4	3	2	1	0
	TYP_ACP_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_ACP_SET	[7:0]	ACP Packet Type code setting

5.13.8. **ISRC1 INFO PACKET TYPE CODE SET. (TYP_ISRC1_SET) (0x8707)**

	7	6	5	4	3	2	1	0
	TYP_ISRC1_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_ISRC1_SET	[7:0]	ISRC1 Packet Type code setting

5.13.9. **ISRC2 INFO PACKET TYPE CODE SETTING (TYP_ISRC2_SET) (0X8708)**

	7	6	5	4	3	2	1	0
	TYP_ISRC2_SET							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
TYP_ISRC2_SET	[7:0]	ISRC2 Packet Type code setting

5.13.10. **PACKET AUTO CLEAR (PK_AUTO_CLR) (0x870A)**

	7	6	5	4	3	2	1	0
	PK_AUTO_CLR7	PK_AUTO_CLR6	PK_AUTO_CLR5	PK_AUTO_CLR4	PK_AUTO_CLR3	PK_AUTO_CLR2	PK_AUTO_CLR1	PK_AUTO_CLR0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
PK_AUTO_CLR7	7	When DVI received, ISRC2_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR6	6	When DVI received, ISRC packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR5	5	When DVI received, ACP packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR4	4	When DVI received, VS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR3	3	When DVI received, SPD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR2	2	When DVI received, MS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR1	1	When DVI received, AUD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR0	0	When DVI received, AVI_info packet data cleared 1: Clear 0: Do not clear

5.13.11. **NO PACKET LIMIT (NO_PK_LIMIT) (0x870B)**

	7	6	5	4	3	2	1	0
	NO_ACP_LIMIT				NO_AVI_LIMIT			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	0	1	1	0	0

Register Field	Bit	Description
NO_ACP_LIMIT	[7:4]	After receiving ACP packet, when ACP packet not received during setting value*80ms period, ACP receive interrupt occurs. Note: At 4'b0000 setting, interrupt does not occur. Note: At 4'b0000 setting, ACP packet receive status action does not occur. Note: When DVI received, interrupt does not occur.
NO_AVI_LIMIT	[3:0]	When AVI packet not received during setting value*80msec period, AVI receive interrupt occurs. Note: At 4'b0000 setting, interrupt does not occur. Note: When DVI received, interrupt does not occur.

5.13.12. **NO PACKET CLEAR (NO_PK _CLR) (0x870C)**

	7	6	5	4	3	2	1	0
	Reserved	NO_VS_CLR	NO_SPD_CLR	NO_ACP_CLR	Reserved		NO_AVI_CLR1	NO_AVI_CLR0
Type	R/W	R/W	R/W	R/W	RO		R/W	R/W
Default	0	1	0	1	0	0	1	1

Register Field	Bit	Description
NO_VS_CLR	6	When VS receive interrupt is detected, VS storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_SPD_CLR	5	When SPD receive interrupt is detected, SPD storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_ACP_CLR	4	When ACP receive interrupt is detected, ACP storage register automatic clear 1: Clear 0: Do not clear
NO_AVI_CLR1	1	When AVI receive interrupt occurs, judge input video signal with RGB and no Repetition 1: Judge 0: No judge (preserve in status before interruption)
NO_AVI_CLR0	0	When AVI receive interrupt is detected, AVI storage register automatic clear 1: Clear 0: Do not clear

5.13.13. **ERROR PACKET LIMIT (ERR_PK_LIMIT) (0x870D)**

	7	6	5	4	3	2	1	0
	ERR_PK_MOD	ERR_PK_LIMIT						
Type	R/W	R/W						
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Description
ERR_PK_MOD	7	Packet continuing receive error detection start conditions 0: If error is included in either header/data 1: If correctable error was included in header
ERR_PK_LIMIT	[6:0]	Packet continuing receive error occurrence detection threshold If error packet is continually received up to set Packet number value, Set Packet receive error status to “1”. If absolutely no error Packet is received, return Packet receive error status for both header/data to “0”. In 0 setting, detection OFF

5.13.14. **NO PACKET LIMIT (NO_PK_LIMIT2) (0x870E)**

	7	6	5	4	3	2	1	0
	NO_VS_LIMIT				NO_SPD_LIMIT			
Type	R/W				R/W			
Default	0	0	1	1	0	0	0	0

Register Field	Bit	Description
NO_VS_LIMIT	[7:4]	If no VS packet is received during setting value*80ms period judge receive interrupt has occurred. At 0000 setting, receive interrupt detect is OFF.
NO_SPD_LIMIT	[3:0]	If no SPD packet is received during setting value*80ms period judge receive interrupt has occurred. At 0000 setting, receive interrupt detect is OFF.

5.13.15. **AVI INFO PACKET HEADER BYTE 0 (PK_AVI_0HEAD) (0x8710)**

	7	6	5	4	3	2	1	0
	AVI_0HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_0HEAD	[7:0]	861B AVI_info packet Header byte 0 (= type)

5.13.16. **AVI INFO PACKET HEADER BYTE 1 (PK_AVI_1HEAD) (0x8711)**

	7	6	5	4	3	2	1	0
	AVI_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_1HEAD	[7:0]	861B AVI_info packet Header byte 1 (= version)

5.13.17. **AVI INFO PACKET HEADER BYTE 2 (PK_AVI_2HEAD) (0x8712)**

	7	6	5	4	3	2	1	0
	AVI_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_2HEAD	[7:0]	861B AVI_info packet Header byte 2 (= data length)

5.13.18. **AVI INFO PACKET DATA BYTE 0 (PK_AVI_0BYTE) (0x8713)**

	7	6	5	4	3	2	1	0
	AVI_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_0BYTE	[7:0]	861B AVI_info packet Data byte 0 (= checksum)

5.13.19. **AVI INFO PACKET DATA BYTE 1 (PK_AVI_1BYTE) (0x8714)**

	7	6	5	4	3	2	1	0
	AVI_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_1BYTE	[7:0]	861B AVI_info packet Data byte 1

5.13.20. **AVI INFO PACKET DATA BYTE 2 (PK_AVI_2BYTE) (0x8715)**

	7	6	5	4	3	2	1	0
	AVI_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_2BYTE	[7:0]	861B AVI_info packet Data byte 2

5.13.21. **AVI INFO PACKET DATA BYTE 3 (PK_AVI_3BYTE) (0x8716)**

	7	6	5	4	3	2	1	0
	AVI_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_3BYTE	[7:0]	861B AVI_info packet Data byte 3

5.13.22. **AVI INFO PACKET DATA BYTE 4 (PK_AVI_4BYTE) (0x8717)**

	7	6	5	4	3	2	1	0
	AVI_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_4BYTE	[7:0]	861B AVI_info packet Data byte 4

5.13.23. **AVI INFO PACKET DATA BYTE 5 (PK_AVI_5BYTE) (0x8718)**

	7	6	5	4	3	2	1	0
	AVI_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_5BYTE	[7:0]	861B AVI_info packet Data byte 5

5.13.24. **AVI INFO PACKET DATA BYTE 6 (PK_AVI_6BYTE) (0x8719)**

	7	6	5	4	3	2	1	0
	AVI_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_6BYTE	[7:0]	861B AVI_info packet Data byte 6

5.13.25. **AVI INFO PACKET DATA BYTE 7 (PK_AVI_7BYTE) (0x871a)**

	7	6	5	4	3	2	1	0
	AVI_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_7BYTE	[7:0]	861B AVI_info packet Data byte 7

5.13.26. **AVI INFO PACKET DATA BYTE 8 (PK_AVI_8BYTE) (0x871b)**

	7	6	5	4	3	2	1	0
	AVI_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_8BYTE	[7:0]	861B AVI_info packet Data byte 8

5.13.27. **AVI INFO PACKET DATA BYTE 9 (PK_AVI_9BYTE) (0x871c)**

	7	6	5	4	3	2	1	0
	AVI_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_9BYTE	[7:0]	861B AVI_info packet Data byte 9

5.13.28. **AVI INFO PACKET DATA BYTE 10 (PK_AVI_10BYTE) (0x871d)**

	7	6	5	4	3	2	1	0
	AVI_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_10BYTE	[7:0]	861B AVI_info packet Data byte 10

5.13.29. **AVI INFO PACKET DATA BYTE 11 (PK_AVI_11BYTE) (0x871e)**

	7	6	5	4	3	2	1	0
	AVI_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_11BYTE	[7:0]	861B AVI_info packet Data byte 11

5.13.30. **AVI INFO PACKET DATA BYTE 12 (PK_AVI_12BYTE) (0x871f)**

	7	6	5	4	3	2	1	0
	AVI_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_12BYTE	[7:0]	861B AVI_info packet Data byte 12

5.13.31. **AVI INFO PACKET DATA BYTE 13 (PK_AVI_13BYTE) (0x8720)**

	7	6	5	4	3	2	1	0
	AVI_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_13BYTE	[7:0]	861B AVI_info packet Data byte 13

5.13.32. **AVI INFO PACKET DATA BYTE 14 (PK_AVI_14BYTE) (0x8721)**

	7	6	5	4	3	2	1	0
	AVI_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_14BYTE	[7:0]	861B AVI_info packet Data byte 14 (Reserved for standards extension)

5.13.33. **AVI INFO PACKET DATA BYTE 15 (PK_AVI_15BYTE) (0x8722)**

	7	6	5	4	3	2	1	0
	AVI_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_15BYTE	[7:0]	861B AVI_info packet Data byte 15 (Reserved for standards extension)

5.13.34. **AVI INFO PACKET DATA BYTE 16 (PK_AVI_16BYTE) (0x8723)**

	7	6	5	4	3	2	1	0
	AVI_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AVI_16BYTE	[7:0]	861B AVI_info packet Data byte 16 (Reserved for standards extension)

5.13.35. **AUD INFO PACKET HEADER BYTE 0 (PK_AUD_0HEAD) (0x8730)**

	7	6	5	4	3	2	1	0
	AUD_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_0HEAD	[7:0]	861B AUD_info packet Header byte 0 (= type)

5.13.36. **AUD INFO PACKET HEADER BYTE 1 (PK_AUD_1HEAD) (0x8731)**

	7	6	5	4	3	2	1	0
	AUD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_1HEAD	[7:0]	861B AUD_info packet Header byte 1 (= version)

5.13.37. **AUD INFO PACKET HEADER BYTE 2 (PK_AUD_2HEAD) (0x8732)**

	7	6	5	4	3	2	1	0
	AUD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_2HEAD	[7:0]	861B AUD_info packet Header byte 2 (= data length)

5.13.38. **AUD INFO PACKET DATA BYTE 0 (PK_AUD_0BYTE) (0x8733)**

	7	6	5	4	3	2	1	0
	AUD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_0BYTE	[7:0]	861B AUD_info packet Data byte 0 (= checksum)

5.13.39. **AUD INFO PACKET DATA BYTE 1 (PK_AUD_1BYTE) (0x8734)**

	7	6	5	4	3	2	1	0
	AUD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_1BYTE	[7:0]	861B AUD_info packet Data byte 1

5.13.40. **AUD INFO PACKET DATA BYTE 2 (PK_AUD_2BYTE) (0x8735)**

	7	6	5	4	3	2	1	0
	AUD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_2BYTE	[7:0]	861B AUD_info packet Data byte 2

5.13.41. **AUD INFO PACKET DATA BYTE 3 (PK_AUD_3BYTE) (0x8736)**

	7	6	5	4	3	2	1	0
	AUD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_3BYTE	[7:0]	861B AUD_info packet Data byte 3

5.13.42. **AUD INFO PACKET DATA BYTE 4 (PK_AUD_4BYTE) (0x8737)**

	7	6	5	4	3	2	1	0
	AUD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_4BYTE	[7:0]	861B AUD_info packet Data byte 4

5.13.43. **AUD INFO PACKET DATA BYTE 5 (PK_AUD_5BYTE) (0x8738)**

	7	6	5	4	3	2	1	0
	AUD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_5BYTE	[7:0]	861B AUD_info packet Data byte 5

5.13.44. **AUD INFO PACKET DATA BYTE 6 (PK_AUD_6BYTE) (0x8739)**

	7	6	5	4	3	2	1	0
	AUD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_6BYTE	[7:0]	861B AUD_info packet Data byte 6 (Reserved for standards extension)

5.13.45. **AUD INFO PACKET DATA BYTE 7 (PK_AUD_7BYTE) (0x873a)**

	7	6	5	4	3	2	1	0
	AUD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_7BYTE	[7:0]	861B AUD_info packet Data byte 7 (Reserved for standards extension)

5.13.46. **AUD INFO PACKET DATA BYTE 8 (PK_AUD_8BYTE) (0x873b)**

	7	6	5	4	3	2	1	0
	AUD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_8BYTE	[7:0]	861B AUD_info packet Data byte 8 (Reserved for standards extension)

5.13.47. **AUD INFO PACKET DATA BYTE 9 (PK_AUD_9BYTE) (0x873c)**

	7	6	5	4	3	2	1	0
	AUD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_9BYTE	[7:0]	861B AUD_info packet Data byte 9 (Reserved for standards extension)

5.13.48. **AUD INFO PACKET DATA BYTE 10 (PK_AUD_10BYTE) (0x873d)**

	7	6	5	4	3	2	1	0
	AUD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
AUD_10BYTE	[7:0]	861B AUD_info packet Data byte 10 (Reserved for standards extension)

5.13.49. **MS INFO PACKET HEADER BYTE 0 (PK_MS_0HEAD) (0x8740)**

	7	6	5	4	3	2	1	0
	MS_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_0HEAD	[7:0]	861B MS_info packet Header byte 0 (= type)

5.13.50. **MS INFO PACKET HEADER BYTE 1 (PK_MS_1HEAD) (0x8741)**

	7	6	5	4	3	2	1	0
	MS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_1HEAD	[7:0]	861B MS_info packet Header byte 1 (= version)

5.13.51. **MS INFO PACKET HEADER BYTE 2 (PK_MS_2HEAD) (0x8742)**

	7	6	5	4	3	2	1	0
	MS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_2HEAD	[7:0]	861B MS_info packet Header byte 2 (= data length)

5.13.52. **MS INFO PACKET DATA BYTE 0 (PK_MS_0BYTE) (0x8743)**

	7	6	5	4	3	2	1	0
	MS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_0BYTE	[7:0]	861B MS_info packet Data byte 0 (= checksum)

5.13.53. **MS INFO PACKET DATA BYTE 1 (PK_MS_1BYTE) (0x8744)**

	7	6	5	4	3	2	1	0
	MS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_1BYTE	[7:0]	861B MS_info packet Data byte 1

5.13.54. **MS INFO PACKET DATA BYTE 2 (PK_MS_2BYTE) (0x8745)**

	7	6	5	4	3	2	1	0
	MS_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_2BYTE	[7:0]	861B MS_info packet Data byte 2

5.13.55. **MS INFO PACKET DATA BYTE 3 (PK_MS_3BYTE) (0x8746)**

	7	6	5	4	3	2	1	0
	MS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_3BYTE	[7:0]	861B MS_info packet Data byte 3

5.13.56. **MS INFO PACKET DATA BYTE 4 (PK_MS_4BYTE) (0x8747)**

	7	6	5	4	3	2	1	0
	MS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_4BYTE	[7:0]	861B MS_info packet Data byte 4

5.13.57. **MS INFO PACKET DATA BYTE 5 (PK_MS_5BYTE) (0x8748)**

	7	6	5	4	3	2	1	0
	MS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_5BYTE	[7:0]	861B MS_info packet Data byte 5

5.13.58. **MS INFO PACKET DATA BYTE 6 (PK_MS_6BYTE) (0x8749)**

	7	6	5	4	3	2	1	0
	MS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_6BYTE	[7:0]	861B MS_info packet Data byte 6 (Reserved for standards extension)

5.13.59. **MS INFO PACKET DATA BYTE 7 (PK_MS_7BYTE) (0x874a)**

	7	6	5	4	3	2	1	0
	MS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_7BYTE	[7:0]	861B MS_info packet Data byte 7 (Reserved for standards extension)

5.13.60. **MS INFO PACKET DATA BYTE 8 (PK_MS_8BYTE) (0x874b)**

	7	6	5	4	3	2	1	0
	MS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_8BYTE	[7:0]	861B MS_info packet Data byte 8 (Reserved for standards extension)

5.13.61. **MS INFO PACKET DATA BYTE 9 (PK_MS_9BYTE) (0x874c)**

	7	6	5	4	3	2	1	0
	MS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_9BYTE	[7:0]	861B MS_info packet Data byte 9 (Reserved for standards extension)

5.13.62. **MS INFO PACKET DATA BYTE 10 (PK_MS_10BYTE) (0x874d)**

	7	6	5	4	3	2	1	0
	MS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
MS_10BYTE	[7:0]	861B MS_info packet Data byte 10 (Reserved for standards extension)

5.13.63. **SPD INFO PACKET HEADER BYTE 0 (PK_SPD_0HEAD) (0x8750)**

	7	6	5	4	3	2	1	0
	SPD_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_0HEAD	[7:0]	861B SPD_info packet Header byte 0 (= type)

5.13.64. **SPD INFO PACKET HEADER BYTE 1 (PK_SPD_1HEAD) (0x8751)**

	7	6	5	4	3	2	1	0
	SPD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_1HEAD	[7:0]	861B SPD_info packet Header byte 1 (= version)

5.13.65. **SPD INFO PACKET HEADER BYTE 2 (PK_SPD_2HEAD) (0x8752)**

	7	6	5	4	3	2	1	0
	SPD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_2HEAD	[7:0]	861B SPD_info packet Header byte 2 (= data length)

5.13.66. **SPD INFO PACKET DATA BYTE 0 (PK_SPD_0BYTE) (0x8753)**

	7	6	5	4	3	2	1	0
	SPD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_0BYTE	[7:0]	861B SPD_info packet Data byte 0 (= checksum)

5.13.67. **SPD INFO PACKET DATA BYTE 1 (PK_SPD_1BYTE) (0x8754)**

	7	6	5	4	3	2	1	0
	SPD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_1BYTE	[7:0]	861B SPD_info packet Data byte 1

5.13.68. **SPD INFO PACKET DATA BYTE 2 (PK_SPD_2BYTE) (0x8755)**

	7	6	5	4	3	2	1	0
	SPD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_2BYTE	[7:0]	861B SPD_info packet Data byte 2

5.13.69. **SPD INFO PACKET DATA BYTE 3 (PK_SPD_3BYTE) (0x8756)**

	7	6	5	4	3	2	1	0
	SPD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_3BYTE	[7:0]	861B SPD_info packet Data byte 3

5.13.70. **SPD INFO PACKET DATA BYTE 4 (PK_SPD_4BYTE) (0x8757)**

	7	6	5	4	3	2	1	0
	SPD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_4BYTE	[7:0]	861B SPD_info packet Data byte 4

5.13.71. **SPD INFO PACKET DATA BYTE 5 (PK_SPD_5BYTE) (0x8758)**

	7	6	5	4	3	2	1	0
	SPD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_5BYTE	[7:0]	861B SPD_info packet Data byte 5

5.13.72. **SPD INFO PACKET DATA BYTE 6 (PK_SPD_6BYTE) (0x8759)**

	7	6	5	4	3	2	1	0
	SPD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_6BYTE	[7:0]	861B SPD_info packet Data byte 6

5.13.73. **SPD INFO PACKET DATA BYTE 7 (PK_SPD_7BYTE) (0x875a)**

	7	6	5	4	3	2	1	0
	SPD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_7BYTE	[7:0]	861B SPD_info packet Data byte 7

5.13.74. **SPD INFO PACKET DATA BYTE 8 (PK_SPD_8BYTE) (0x875b)**

	7	6	5	4	3	2	1	0
	SPD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_8BYTE	[7:0]	861B SPD_info packet Data byte 8

5.13.75. **SPD INFO PACKET DATA BYTE 9 (PK_SPD_9BYTE) (0x875c)**

	7	6	5	4	3	2	1	0
	SPD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_9BYTE	[7:0]	861B SPD_info packet Data byte 9

5.13.76. **SPD INFO PACKET DATA BYTE 10 (PK_SPD_10BYTE) (0x875d)**

	7	6	5	4	3	2	1	0
	SPD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_10BYTE	[7:0]	861B SPD_info packet Data byte 10

5.13.77. **SPD INFO PACKET DATA BYTE 11 (PK_SPD_11BYTE) (0x875e)**

	7	6	5	4	3	2	1	0
	SPD_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_11BYTE	[7:0]	861B SPD_info packet Data byte 11

5.13.78. **SPD INFO PACKET DATA BYTE 12 (PK_SPD_12BYTE) (0x875f)**

	7	6	5	4	3	2	1	0
	SPD_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_12BYTE	[7:0]	861B SPD_info packet Data byte 12

5.13.79. **SPD INFO PACKET DATA BYTE 13 (PK_SPD_13BYTE) (0x8760)**

	7	6	5	4	3	2	1	0
	SPD_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_13BYTE	[7:0]	861B SPD_info packet Data byte 13

5.13.80. **SPD INFO PACKET DATA BYTE 14 (PK_SPD_14BYTE) (0x8761)**

	7	6	5	4	3	2	1	0
	SPD_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_14BYTE	[7:0]	861B SPD_info packet Data byte 14

5.13.81. **SPD INFO PACKET DATA BYTE 15 (PK_SPD_15BYTE) (0x8762)**

	7	6	5	4	3	2	1	0
	SPD_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_15BYTE	[7:0]	861B SPD_info packet Data byte 15

5.13.82. **SPD INFO PACKET DATA BYTE 16 (PK_SPD_16BYTE) (0x8763)**

	7	6	5	4	3	2	1	0
	SPD_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_16BYTE	[7:0]	861B SPD_info packet Data byte 16

5.13.83. **SPD INFO PACKET DATA BYTE 17 (PK_SPD_17BYTE) (0x8764)**

	7	6	5	4	3	2	1	0
	SPD_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_17BYTE	[7:0]	861B SPD_info packet Data byte 17

5.13.84. **SPD INFO PACKET DATA BYTE 18 (PK_SPD_18BYTE) (0x8765)**

	7	6	5	4	3	2	1	0
	SPD_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_18BYTE	[7:0]	861B SPD_info packet Data byte 18

5.13.85. **SPD INFO PACKET DATA BYTE 19 (PK_SPD_19BYTE) (0x8766)**

	7	6	5	4	3	2	1	0
	SPD_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_19BYTE	[7:0]	861B SPD_info packet Data byte 19

5.13.86. **SPD INFO PACKET DATA BYTE 20 (PK_SPD_20BYTE) (0x8767)**

	7	6	5	4	3	2	1	0
	SPD_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_20BYTE	[7:0]	861B SPD_info packet Data byte 20

5.13.87. **SPD INFO PACKET DATA BYTE 21 (PK_SPD_21BYTE) (0x8768)**

	7	6	5	4	3	2	1	0
	SPD_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_21BYTE	[7:0]	861B SPD_info packet Data byte 21

5.13.88. **SPD INFO PACKET DATA BYTE 22 (PK_SPD_22BYTE) (0x8769)**

	7	6	5	4	3	2	1	0
	SPD_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_22BYTE	[7:0]	861B SPD_info packet Data byte 22

5.13.89. **SPD INFO PACKET DATA BYTE 23 (PK_SPD_23BYTE) (0x876a)**

	7	6	5	4	3	2	1	0
	SPD_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_23BYTE	[7:0]	861B SPD_info packet Data byte 23

5.13.90. **SPD INFO PACKET DATA BYTE 24 (PK_SPD_24BYTE) (0x876b)**

	7	6	5	4	3	2	1	0
	SPD_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_24BYTE	[7:0]	861B SPD_info packet Data byte 24

5.13.91. **SPD INFO PACKET DATA BYTE 25 (PK_SPD_25BYTE) (0x876c)**

	7	6	5	4	3	2	1	0
	SPD_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_25BYTE	[7:0]	861B SPD_info packet Data byte 25

5.13.92. **SPD INFO PACKET DATA BYTE 26 (PK_SPD_26BYTE) (0x876d)**

	7	6	5	4	3	2	1	0
	SPD_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
SPD_26BYTE	[7:0]	861B SPD_info packet Data byte 26 (Reserved for standards extension)

5.13.93. **SPD INFO PACKET DATA BYTE 27 (PK_SPD_27BYTE) (0x876e)**

	7	6	5	4	3	2	1	0
	SPD_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	**Bit**	**Description**
SPD_27BYTE	[7:0]	861B SPD_info packet Data byte 27 (Reserved for standards extension)

5.13.94. **VS INFO PACKET HEADER BYTE 0 (PK_VS_0HEAD) (0x8770)**

	7	6	5	4	3	2	1	0
	VS_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	**Bit**	**Description**
VS_0HEAD	[7:0]	861B VS_info packet Header byte 0 (= type)

5.13.95. **VS INFO PACKET HEADER BYTE 1 (PK_VS_1HEAD) (0x8771)**

	7	6	5	4	3	2	1	0
	VS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_1HEAD	[7:0]	861B VS_info packet Header byte 1 (= version)

5.13.96. **VS INFO PACKET HEADER BYTE 2 (PK_VS_2HEAD) (0x8772)**

	7	6	5	4	3	2	1	0
	VS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_2HEAD	[7:0]	861B VS_info packet Header byte 2 (= data length)

5.13.97. **VS INFO PACKET DATA BYTE 0 (PK_VS_0BYTE) (0x8773)**

	7	6	5	4	3	2	1	0
	VS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_0BYTE	[7:0]	861B VS_info packet Data byte 0 (= checksum)

5.13.98. **VS INFO PACKET DATA BYTE 1 (PK_VS_1BYTE) (0x8774)**

	7	6	5	4	3	2	1	0
	VS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_1BYTE	[7:0]	861B VS_info packet Data byte 1

5.13.99. **VS INFO PACKET DATA BYTE 2 (PK_VS_2BYTE) (0x8775)**

	7	6	5	4	3	2	1	0
	VS_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_2BYTE	[7:0]	861B VS_info packet Data byte 2

5.13.100. **VS INFO PACKET DATA BYTE 3 (PK_VS_3BYTE) (0x8776)**

	7	6	5	4	3	2	1	0
	VS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_3BYTE	[7:0]	861B VS_info packet Data byte 3

5.13.101. **VS INFO PACKET DATA BYTE 4 (PK_VS_4BYTE) (0x8777)**

	7	6	5	4	3	2	1	0
	VS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_4BYTE	[7:0]	861B VS_info packet Data byte 4

5.13.102. **VS INFO PACKET DATA BYTE 5 (PK_VS_5BYTE) (0x8778)**

	7	6	5	4	3	2	1	0
	VS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_5BYTE	[7:0]	861B VS_info packet Data byte 5

5.13.103. **VS INFO PACKET DATA BYTE 6 (PK_VS_6BYTE) (0x8779)**

	7	6	5	4	3	2	1	0
	VS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_6BYTE	[7:0]	861B VS_info packet Data byte 6

5.13.104. **VS INFO PACKET DATA BYTE 7 (PK_VS_7BYTE) (0x877a)**

	7	6	5	4	3	2	1	0
	VS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_7BYTE	[7:0]	861B VS_info packet Data byte 7

5.13.105. **VS INFO PACKET DATA BYTE 8 (PK_VS_8BYTE) (0x877b)**

	7	6	5	4	3	2	1	0
	VS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_8BYTE	[7:0]	861B VS_info packet Data byte 8

5.13.106. **VS INFO PACKET DATA BYTE 9 (PK_VS_9BYTE) (0x877c)**

	7	6	5	4	3	2	1	0
	VS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_9BYTE	[7:0]	861B VS_info packet Data byte 9

5.13.107. **VS INFO PACKET DATA BYTE 10 (PK_VS_10BYTE) (0x877d)**

	7	6	5	4	3	2	1	0
	VS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_10BYTE	[7:0]	861B VS_info packet Data byte 10

5.13.108. **VS INFO PACKET DATA BYTE 11 (PK_VS_11BYTE) (0x877e)**

	7	6	5	4	3	2	1	0
	VS_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_11BYTE	[7:0]	861B VS_info packet Data byte 11

5.13.109. **VS INFO PACKET DATA BYTE 12 (PK_VS_12BYTE) (0x877f)**

	7	6	5	4	3	2	1	0
	VS_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_12BYTE	[7:0]	861B VS_info packet Data byte 12

5.13.110. **VS INFO PACKET DATA BYTE 13 (PK_VS_13BYTE) (0x8780)**

	7	6	5	4	3	2	1	0
	VS_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_13BYTE	[7:0]	861B VS_info packet Data byte 13

5.13.111. **VS INFO PACKET DATA BYTE 14 (PK_VS_14BYTE) (0x8781)**

	7	6	5	4	3	2	1	0
	VS_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_14BYTE	[7:0]	861B VS_info packet Data byte 14

5.13.112. **VS INFO PACKET DATA BYTE 15 (PK_VS_15BYTE) (0x8782)**

	7	6	5	4	3	2	1	0
	VS_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_15BYTE	[7:0]	861B VS_info packet Data byte 15

5.13.113. **VS INFO PACKET DATA BYTE 16 (PK_VS_16BYTE) (0x8783)**

	7	6	5	4	3	2	1	0
	VS_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_16BYTE	[7:0]	861B VS_info packet Data byte 16

5.13.114. **VS INFO PACKET DATA BYTE 17 (PK_VS_17BYTE) (0x8784)**

	7	6	5	4	3	2	1	0
	VS_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_17BYTE	[7:0]	861B VS_info packet Data byte 17

5.13.115. **VS INFO PACKET DATA BYTE 18 (PK_VS_18BYTE) (0x8785)**

	7	6	5	4	3	2	1	0
	VS_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_18BYTE	[7:0]	861B VS_info packet Data byte 18

5.13.116. **VS INFO PACKET DATA BYTE 19 (PK_VS_19BYTE) (0x8786)**

	7	6	5	4	3	2	1	0
	VS_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_19BYTE	[7:0]	861B VS_info packet Data byte 19

5.13.117. **VS INFO PACKET DATA BYTE 20 (PK_VS_20BYTE) (0x8787)**

	7	6	5	4	3	2	1	0
	VS_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_20BYTE	[7:0]	861B VS_info packet Data byte 20

5.13.118. **VS INFO PACKET DATA BYTE 21 (PK_VS_21BYTE) (0x8788)**

	7	6	5	4	3	2	1	0
	VS_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_21BYTE	[7:0]	861B VS_info packet Data byte 21

5.13.119. **VS INFO PACKET DATA BYTE 22 (PK_VS_22BYTE) (0x8789)**

	7	6	5	4	3	2	1	0
	VS_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_22BYTE	[7:0]	861B VS_info packet Data byte 22

5.13.120. **VS INFO PACKET DATA BYTE 23 (PK_VS_23BYTE) (0x878a)**

	7	6	5	4	3	2	1	0
	VS_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_23BYTE	[7:0]	861B VS_info packet Data byte 23

5.13.121. **VS INFO PACKET DATA BYTE 24 (PK_VS_24BYTE) (0x878b)**

	7	6	5	4	3	2	1	0
	VS_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_24BYTE	[7:0]	861B VS_info packet Data byte 24

5.13.122. **VS INFO PACKET DATA BYTE 25 (PK_VS_25BYTE) (0x878c)**

	7	6	5	4	3	2	1	0
	VS_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_25BYTE	[7:0]	861B VS_info packet Data byte 25

5.13.123. **VS INFO PACKET DATA BYTE 26 (PK_VS_26BYTE) (0x878d)**

	7	6	5	4	3	2	1	0
	VS_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_26BYTE	[7:0]	861B VS_info packet Data byte 26

5.13.124. **VS INFO PACKET DATA BYTE 27 (PK_VS_27BYTE) (0x878e)**

	7	6	5	4	3	2	1	0
	VS_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
VS_27BYTE	[7:0]	861B VS_info packet Data byte 27

5.13.125. **ACP INFO PACKET HEADER BYTE 0 (PK_ACP_0HEAD) (0x8790)**

	7	6	5	4	3	2	1	0
	ACP_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_0HEAD	[7:0]	861B ACP_info packet Header byte 0 (= type)

5.13.126. **ACP INFO PACKET HEADER BYTE 1 (PK_ACP_1HEAD) (0x8791)**

	7	6	5	4	3	2	1	0
	ACP_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_1HEAD	[7:0]	861B ACP_info packet Header byte 1 (= version)

5.13.127. **ACP INFO PACKET HEADER BYTE 2 (PK_ACP_2HEAD) (0x8792)**

	7	6	5	4	3	2	1	0
	ACP_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_2HEAD	[7:0]	861B ACP_info packet Header byte 2 (= data length)

5.13.128. **ACP INFO PACKET DATA BYTE 0 (PK_ACP_0BYTE) (0x8793)**

	7	6	5	4	3	2	1	0
	ACP_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_0BYTE	[7:0]	861B ACP_info packet Data byte 0 (= checksum)

5.13.129. **ACP INFO PACKET DATA BYTE 1 (PK_ACP_1BYTE) (0x8794)**

	7	6	5	4	3	2	1	0
	ACP_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_1BYTE	[7:0]	861B ACP_info packet Data byte 1

5.13.130. **ACP INFO PACKET DATA BYTE 2 (PK_ACP_2BYTE) (0x8795)**

	7	6	5	4	3	2	1	0
	ACP_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_2BYTE	[7:0]	861B ACP_info packet Data byte 2

5.13.131. **ACP INFO PACKET DATA BYTE 3 (PK_ACP_3BYTE) (0x8796)**

	7	6	5	4	3	2	1	0
	ACP_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_3BYTE	[7:0]	861B ACP_info packet Data byte 3

5.13.132. **ACP INFO PACKET DATA BYTE 4 (PK_ACP_4BYTE) (0x8797)**

	7	6	5	4	3	2	1	0
	ACP_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_4BYTE	[7:0]	861B ACP_info packet Data byte 4

5.13.133. **ACP INFO PACKET DATA BYTE 5 (PK_ACP_5BYTE) (0x8798)**

	7	6	5	4	3	2	1	0
	ACP_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_5BYTE	[7:0]	861B ACP_info packet Data byte 5

5.13.134. **ACP INFO PACKET DATA BYTE 6 (PK_ACP_6BYTE) (0x8799)**

	7	6	5	4	3	2	1	0
	ACP_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_6BYTE	[7:0]	861B ACP_info packet Data byte 6

5.13.135. **ACP INFO PACKET DATA BYTE 7 (PK_ACP_7BYTE) (0x879a)**

	7	6	5	4	3	2	1	0
	ACP_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_7BYTE	[7:0]	861B ACP_info packet Data byte 7

5.13.136. **ACP INFO PACKET DATA BYTE 8 (PK_ACP_8BYTE) (0x879b)**

	7	6	5	4	3	2	1	0
	ACP_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_8BYTE	[7:0]	861B ACP_info packet Data byte 8

5.13.137. **ACP INFO PACKET DATA BYTE 9 (PK_ACP_9BYTE) (0x879c)**

	7	6	5	4	3	2	1	0
	ACP_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_9BYTE	[7:0]	861B ACP_info packet Data byte 9

5.13.138. **ACP INFO PACKET DATA BYTE 10 (PK_ACP_10BYTE) (0x879d)**

	7	6	5	4	3	2	1	0
	ACP_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_10BYTE	[7:0]	861B ACP_info packet Data byte 10

5.13.139. **ACP INFO PACKET DATA BYTE 11 (PK_ACP_11BYTE) (0x879e)**

	7	6	5	4	3	2	1	0
	ACP_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_11BYTE	[7:0]	861B ACP_info packet Data byte 11

5.13.140. **ACP INFO PACKET DATA BYTE 12 (PK_ACP_12BYTE) (0x879f)**

	7	6	5	4	3	2	1	0
	ACP_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_12BYTE	[7:0]	861B ACP_info packet Data byte 12

5.13.141. **ACP INFO PACKET DATA BYTE 13 (PK_ACP_13BYTE) (0x87a0)**

	7	6	5	4	3	2	1	0
	ACP_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_13BYTE	[7:0]	861B ACP_info packet Data byte 13

5.13.142. **ACP INFO PACKET DATA BYTE 14 (PK_ACP_14BYTE) (0x87a1)**

	7	6	5	4	3	2	1	0
	ACP_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_14BYTE	[7:0]	861B ACP_info packet Data byte 14

5.13.143. **ACP INFO PACKET DATA BYTE 15 (PK_ACP_15BYTE) (0x87a2)**

	7	6	5	4	3	2	1	0
	ACP_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_15BYTE	[7:0]	861B ACP_info packet Data byte 15

5.13.144. **ACP INFO PACKET DATA BYTE 16 (PK_ACP_16BYTE) (0x87a3)**

	7	6	5	4	3	2	1	0
	ACP_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_16BYTE	[7:0]	861B ACP_info packet Data byte 16

5.13.145. **ACP INFO PACKET DATA BYTE 17 (PK_ACP_17BYTE) (0x87a4)**

	7	6	5	4	3	2	1	0
	ACP_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_17BYTE	[7:0]	861B ACP_info packet Data byte 17

5.13.146. **ACP INFO PACKET DATA BYTE 18 (PK_ACP_18BYTE) (0x87a5)**

	7	6	5	4	3	2	1	0
	ACP_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_18BYTE	[7:0]	861B ACP_info packet Data byte 18

5.13.147. **ACP INFO PACKET DATA BYTE 19 (PK_ACP_19BYTE) (0x87a6)**

	7	6	5	4	3	2	1	0
	ACP_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_19BYTE	[7:0]	861B ACP_info packet Data byte 19

5.13.148. **ACP INFO PACKET DATA BYTE 20 (PK_ACP_20BYTE) (0x87a7)**

	7	6	5	4	3	2	1	0
	ACP_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_20BYTE	[7:0]	861B ACP_info packet Data byte 20

5.13.149. **ACP INFO PACKET DATA BYTE 21 (PK_ACP_21BYTE) (0x87a8)**

	7	6	5	4	3	2	1	0
	ACP_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_21BYTE	[7:0]	861B ACP_info packet Data byte 21

5.13.150. **ACP INFO PACKET DATA BYTE 22 (PK_ACP_22BYTE) (0x87a9)**

	7	6	5	4	3	2	1	0
	ACP_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_22BYTE	[7:0]	861B ACP_info packet Data byte 22

5.13.151. **ACP INFO PACKET DATA BYTE 23 (PK_ACP_23BYTE) (0x87aa)**

	7	6	5	4	3	2	1	0
	ACP_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_23BYTE	[7:0]	861B ACP_info packet Data byte 23

5.13.152. **ACP INFO PACKET DATA BYTE 24 (PK_ACP_24BYTE) (0x87ab)**

	7	6	5	4	3	2	1	0
	ACP_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_24BYTE	[7:0]	861B ACP_info packet Data byte 24

5.13.153. **ACP INFO PACKET DATA BYTE 25 (PK_ACP_25BYTE) (0x87ac)**

	7	6	5	4	3	2	1	0
	ACP_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_25BYTE	[7:0]	861B ACP_info packet Data byte 25

5.13.154. **ACP INFO PACKET DATA BYTE 26 (PK_ACP_26BYTE) (0x87ad)**

	7	6	5	4	3	2	1	0
	ACP_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_26BYTE	[7:0]	861B ACP_info packet Data byte 26

5.13.155. **ACP INFO PACKET DATA BYTE 27 (PK_ACP_27BYTE) (0x87ae)**

	7	6	5	4	3	2	1	0
	ACP_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ACP_27BYTE	[7:0]	861B ACP_info packet Data byte 27

5.13.156. **ISRC1 INFO PACKET HEADER BYTE 0 (PK_ISRC1_0HEAD) (0x87b0)**

	7	6	5	4	3	2	1	0
	ISRC1_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_0HEAD	[7:0]	861B ISRC1_info packet Header byte 0 (= type)

5.13.157. **ISRC1 INFO PACKET HEADER BYTE 1 (PK_ISRC1_1HEAD) (0x87b1)**

	7	6	5	4	3	2	1	0
	ISRC1_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_1HEAD	[7:0]	861B ISRC1_info packet Header byte 1 (= version)

5.13.158. **ISRC1 INFO PACKET HEADER BYTE 2 (PK_ISRC1_2HEAD) (0x87b2)**

	7	6	5	4	3	2	1	0
	ISRC1_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_2HEAD	[7:0]	861B ISRC1_info packet Header byte 2 (= data length)

5.13.159. **ISRC1 INFO PACKET DATA BYTE 0 (PK_ISRC1_0BYTE) (0x87b3)**

	7	6	5	4	3	2	1	0
	ISRC1_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_0BYTE	[7:0]	861B ISRC1_info packet Data byte 0 (= checksum)

5.13.160. **ISRC1 INFO PACKET DATA BYTE 1 (PK_ISRC1_1BYTE) (0x87b4)**

	7	6	5	4	3	2	1	0
	ISRC1_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_1BYTE	[7:0]	861B ISRC1_info packet Data byte 1

5.13.161. **ISRC1 INFO PACKET DATA BYTE 2 (PK_ISRC1_2BYTE) (0x87b5)**

	7	6	5	4	3	2	1	0
	ISRC1_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_2BYTE	[7:0]	861B ISRC1_info packet Data byte 2

5.13.162. **ISRC1 INFO PACKET DATA BYTE 3 (PK_ISRC1_3BYTE) (0x87b6)**

	7	6	5	4	3	2	1	0
	ISRC1_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_3BYTE	[7:0]	861B ISRC1_info packet Data byte 3

5.13.163. **ISRC1 INFO PACKET DATA BYTE 4 (PK_ISRC1_4BYTE) (0x87b7)**

	7	6	5	4	3	2	1	0
	ISRC1_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_4BYTE	[7:0]	861B ISRC1_info packet Data byte 4

5.13.164. **ISRC1 INFO PACKET DATA BYTE 5 (PK_ISRC1_5BYTE) (0x87b8)**

	7	6	5	4	3	2	1	0
	ISRC1_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_5BYTE	[7:0]	861B ISRC1_info packet Data byte 5

5.13.165. **ISRC1 INFO PACKET DATA BYTE 6 (PK_ISRC1_6BYTE) (0x87b9)**

	7	6	5	4	3	2	1	0
	ISRC1_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_6BYTE	[7:0]	861B ISRC1_info packet Data byte 6

5.13.166. **ISRC1 INFO PACKET DATA BYTE 7 (PK_ISRC1_7BYTE) (0x87ba)**

	7	6	5	4	3	2	1	0
	ISRC1_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_7BYTE	[7:0]	861B ISRC1_info packet Data byte 7

5.13.167. **ISRC1 INFO PACKET DATA BYTE 8 (PK_ISRC1_8BYTE) (0x87bb)**

	7	6	5	4	3	2	1	0
	ISRC1_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_8BYTE	[7:0]	861B ISRC1_info packet Data byte 8

5.13.168. **ISRC1 INFO PACKET DATA BYTE 9 (PK_ISRC1_9BYTE) (0x87bc)**

	7	6	5	4	3	2	1	0
	ISRC1_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_9BYTE	[7:0]	861B ISRC1_info packet Data byte 9

5.13.169. **ISRC1 INFO PACKET DATA BYTE 10 (PK_ISRC1_10BYTE) (0x87bd)**

	7	6	5	4	3	2	1	0
	ISRC1_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_10BYTE	[7:0]	861B ISRC1_info packet Data byte 10

5.13.170. **ISRC1 INFO PACKET DATA BYTE 11 (PK_ISRC1_11BYTE) (0x87be)**

	7	6	5	4	3	2	1	0
	ISRC1_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_11BYTE	[7:0]	861B ISRC1_info packet Data byte 11

5.13.171. **ISRC1 INFO PACKET DATA BYTE 12 (PK_ISRC1_12BYTE) (0x87bf)**

	7	6	5	4	3	2	1	0
	ISRC1_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_12BYTE	[7:0]	861B ISRC1_info packet Data byte 12

5.13.172. **ISRC1 INFO PACKET DATA BYTE 13 (PK_ISRC1_13BYTE) (0x87c0)**

	7	6	5	4	3	2	1	0
	ISRC1_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_13BYTE	[7:0]	861B ISRC1_info packet Data byte 13

5.13.173. **ISRC1 INFO PACKET DATA BYTE 14 (PK_ISRC1_14BYTE) (0x87c1)**

	7	6	5	4	3	2	1	0
	ISRC1_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_14BYTE	[7:0]	861B ISRC1_info packet Data byte 14

5.13.174. **ISRC1 INFO PACKET DATA BYTE 15 (PK_ISRC1_15BYTE) (0x87c2)**

	7	6	5	4	3	2	1	0
	ISRC1_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC1_15BYTE	[7:0]	861B ISRC1_info packet Data byte 15

5.13.175. **ISRC2 INFO PACKET HEADER BYTE 0 (PK_ISRC2_0HEAD) (0x87d0)**

	7	6	5	4	3	2	1	0
	ISRC2_0HEAD							
Type	R/W							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_0HEAD	[7:0]	861B ISRC2_info packet Header byte 0 (= type)

5.13.176. **ISRC2 INFO PACKET HEADER BYTE 1 (PK_ISRC2_1HEAD) (0x87d1)**

	7	6	5	4	3	2	1	0
	ISRC2_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_1HEAD	[7:0]	861B ISRC2_info packet Header byte 1 (= version)

5.13.177. **ISRC2 INFO PACKET HEADER BYTE 2 (PK_ISRC2_2HEAD) (0x87d2)**

	7	6	5	4	3	2	1	0
	ISRC2_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_2HEAD	[7:0]	861B ISRC2_info packet Header byte 2 (= data length)

5.13.178. **ISRC2 INFO PACKET DATA BYTE 0 (PK_ISRC2_0BYTE) (0x87d3)**

	7	6	5	4	3	2	1	0
	ISRC2_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_0BYTE	[7:0]	861B ISRC2_info packet Data byte 0 (= checksum)

5.13.179. **ISRC2 INFO PACKET DATA BYTE 1 (PK_ISRC2_1BYTE) (0x87d4)**

	7	6	5	4	3	2	1	0
	ISRC2_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_1BYTE	[7:0]	861B ISRC2_info packet Data byte 1

5.13.180. **ISRC2 INFO PACKET DATA BYTE 2 (PK_ISRC2_2BYTE) (0x87d5)**

	7	6	5	4	3	2	1	0
	ISRC2_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_2BYTE	[7:0]	861B ISRC2_info packet Data byte 2

5.13.181. **ISRC2 INFO PACKET DATA BYTE 3 (PK_ISRC2_3BYTE) (0x87d6)**

	7	6	5	4	3	2	1	0
	ISRC2_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_3BYTE	[7:0]	861B ISRC2_info packet Data byte 3

5.13.182. **ISRC2 INFO PACKET DATA BYTE 4 (PK_ISRC2_4BYTE) (0x87d7)**

	7	6	5	4	3	2	1	0
	ISRC2_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_4BYTE	[7:0]	861B ISRC2_info packet Data byte 4

5.13.183. **ISRC2 INFO PACKET DATA BYTE 5 (PK_ISRC2_5BYTE) (0x87d8)**

	7	6	5	4	3	2	1	0
	ISRC2_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_5BYTE	[7:0]	861B ISRC2_info packet Data byte 5

5.13.184. **ISRC2 INFO PACKET DATA BYTE 6 (PK_ISRC2_6BYTE) (0x87d9)**

	7	6	5	4	3	2	1	0
	ISRC2_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_6BYTE	[7:0]	861B ISRC2_info packet Data byte 6

5.13.185. **ISRC2 INFO PACKET DATA BYTE 7 (PK_ISRC2_7BYTE) (0x87da)**

	7	6	5	4	3	2	1	0
	ISRC2_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_7BYTE	[7:0]	861B ISRC2_info packet Data byte 7

5.13.186. **ISRC2 INFO PACKET DATA BYTE 8 (PK_ISRC2_8BYTE) (0x87db)**

	7	6	5	4	3	2	1	0
	ISRC2_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_8BYTE	[7:0]	861B ISRC2_info packet Data byte 8

5.13.187. **ISRC2 INFO PACKET DATA BYTE 9 (PK_ISRC2_9BYTE) (0x87dc)**

	7	6	5	4	3	2	1	0
	ISRC2_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_9BYTE	[7:0]	861B ISRC2_info packet Data byte 9

5.13.188. **ISRC2 INFO PACKET DATA BYTE 10 (PK_ISRC2_10BYTE) (0x87dd)**

	7	6	5	4	3	2	1	0
	ISRC2_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_10BYTE	[7:0]	861B ISRC2_info packet Data byte 10

5.13.189. **ISRC2 INFO PACKET DATA BYTE 11 (PK_ISRC2_11BYTE) (0x87de)**

	7	6	5	4	3	2	1	0
	ISRC2_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_11BYTE	[7:0]	861B ISRC2_info packet Data byte 11

5.13.190. **ISRC2 INFO PACKET DATA BYTE 12 (PK_ISRC2_12BYTE) (0x87df)**

	7	6	5	4	3	2	1	0
	ISRC2_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_12BYTE	[7:0]	861B ISRC2_info packet Data byte 12

5.13.191. **ISRC2 INFO PACKET DATA BYTE 13 (PK_ISRC2_13BYTE) (0x87e0)**

	7	6	5	4	3	2	1	0
	ISRC2_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_13BYTE	[7:0]	861B ISRC2_info packet Data byte 13

5.13.192. **ISRC2 INFO PACKET DATA BYTE 14 (PK_ISRC2_14BYTE) (0x87e1)**

	7	6	5	4	3	2	1	0
	ISRC2_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_14BYTE	[7:0]	861B ISRC2_info packet Data byte 14

5.13.193. **ISRC2 INFO PACKET DATA BYTE 15 (PK_ISRC2_15BYTE) (0x87e2)**

	7	6	5	4	3	2	1	0
	ISRC2_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_15BYTE	[7:0]	861B ISRC2_info packet Data byte 15

5.13.194. **ISRC2 INFO PACKET DATA BYTE 16 (PK_ISRC2_16BYTE) (0x87e3)**

	7	6	5	4	3	2	1	0
	ISRC2_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_16BYTE	[7:0]	861B ISRC2_info packet Data byte 16

5.13.195. **ISRC2 INFO PACKET DATA BYTE 17 (PK_ISRC2_17BYTE) (0x87e4)**

	7	6	5	4	3	2	1	0
	ISRC2_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_17BYTE	[7:0]	861B ISRC2_info packet Data byte 17

5.13.196. **ISRC2 INFO PACKET DATA BYTE 18 (PK_ISRC2_18BYTE) (0x87e5)**

	7	6	5	4	3	2	1	0
	ISRC2_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_18BYTE	[7:0]	861B ISRC2_info packet Data byte 18

5.13.197. **ISRC2 INFO PACKET DATA BYTE 19 (PK_ISRC2_19BYTE) (0x87e6)**

	7	6	5	4	3	2	1	0
	ISRC2_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_19BYTE	[7:0]	861B ISRC2_info packet Data byte 19

5.13.198. **ISRC2 INFO PACKET DATA BYTE 20 (PK_ISRC2_20BYTE) (0x87e7)**

	7	6	5	4	3	2	1	0
	ISRC2_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_20BYTE	[7:0]	861B ISRC2_info packet Data byte 20

5.13.199. **ISRC2 INFO PACKET DATA BYTE 21 (PK_ISRC2_21BYTE) (0x87e8)**

	7	6	5	4	3	2	1	0
	ISRC2_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_21BYTE	[7:0]	861B ISRC2_info packet Data byte 21

5.13.200. **ISRC2 INFO PACKET DATA BYTE 22 (PK_ISRC2_22BYTE) (0x87e9)**

	7	6	5	4	3	2	1	0
	ISRC2_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_22BYTE	[7:0]	861B ISRC2_info packet Data byte 22

5.13.201. **ISRC2 INFO PACKET DATA BYTE 23 (PK_ISRC2_23BYTE) (0x87ea)**

	7	6	5	4	3	2	1	0
	ISRC2_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_23BYTE	[7:0]	861B ISRC2_info packet Data byte 23

5.13.202. **ISRC2 INFO PACKET DATA BYTE 24 (PK_ISRC2_24BYTE) (0x87eb)**

	7	6	5	4	3	2	1	0
	ISRC2_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_24BYTE	[7:0]	861B ISRC2_info packet Data byte 24

5.13.203. **ISRC2 INFO PACKET DATA BYTE 25 (PK_ISRC2_25BYTE) (0x87ec)**

	7	6	5	4	3	2	1	0
	ISRC2_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_25BYTE	[7:0]	861B ISRC2_info packet Data byte 25

5.13.204. **ISRC2 INFO PACKET DATA BYTE 26 (PK_ISRC2_26BYTE) (0x87ed)**

	7	6	5	4	3	2	1	0
	ISRC2_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_26BYTE	[7:0]	861B ISRC2_info packet Data byte 26

5.13.205. **ISRC2 INFO PACKET DATA BYTE 27 (PK_ISRC2_27BYTE) (0x87ee)**

	7	6	5	4	3	2	1	0
	ISRC2_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Description
ISRC2_27BYTE	[7:0]	861B ISRC2_info packet Data byte 27

5.14. HDMI Rx HDCP Registers

Only a few a listed here. The others can be referred to HDCP spec. For register 0x88_XX, please refer to HDCP register 0xXX. For example: For register 0x88_08 → HDCP Ri'0 Data.

5.14.1. **HDCP BCAPS Register (BCAPS) (0x8840)**

	7	6	5	4	3	2	1	0
	HDMI_RSVD	Repeater	Ready	FastI2C	Reserved		1.1Fea	Fast_ReAu
Type	R/W	R/W	R/W	R/W	RO		R/W	R/W
Default	1	0	0	0	0	0	0	0

Register Field	Bit	Description
HDMI_RSVD	7	0: automatic move to HDMI mode is not performed.
Repeater	6	1: HDCP Repeter
Ready	5	KSVFiFo is Ready for 2nd Authentication
FastI2C	4	1: 400 kHz Supported
1.1Fea	1	Fixed at '0'
Fast_ReAu	0	Fast re-authentication

5.14.2. **HDCP Rx BSTAUS0 Register (BSTATUS0) (0x8841)**

	7	6	5	4	3	2	1	0
	MAX_DEVS_ EXCEEDED	DEVICE_COUNT						
Type	R/W	R/W						
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MAX_DEVS_EXCEEDED	7	If later stage connection devices number is 17 or more, set to “1”.
DEVICE_COUNT	[6:0]	Later stage connection device number (not including self)

5.14.3. **HDCP Rx BSTAUS1 Register (BSTATUS1) (0x8842)**

	7	6	5	4	3	2	1	0
	Reserved		HDMI_RSVD	HDMI_MODE	MAX_EXCED	DEPTH		
Type	RO		R/W	R/W	R/W	R/W		
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
HDMI_RSVD	5	V' value calculation state machine reset 1: Reset (Auto clear)
HDMI_MODE	4	HDMI mode setting 0: DVI mode 1: HDMI mode
MAX_EXCED	3	Topology error indicator. When set to one, more than seven levels of the repeater have been cascaded together.
DEPTH	[2:0]	Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology.

5.14.4. **KSVFIFO Register (KSVFIFO) (0x8843)**

	7	6	5	4	3	2	1	0
	KSVFIFO							
Type	R/W							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
KSVFIFO	[7:0]	Total 80Byte for 16Devices, DDC Address: 0x74, Offset 0x43

5.15. VIDEO Output Format Registers

5.15.1. **VIDEO OUTPUT FORMAT REGISTER (VOUT_FMT) (0x8A00)**

	7	6	5	4	3	2	1	0
	Reserved			422_SEL	Reserved		VOUT_SEL	
Type	RO			RW	RO		RW	
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
422_SEL	4	4:2:2 format setting 0: Normal Format Y[11:0] data are outputted from Y_o[15:4] ports. CB/CR[11:0] data are outputted from CB_o[15:4] ports. 1: HDMI through format Y[11:4] data are outputted from Y_o[15:8] ports. Y[3:0] data are outputted from CB_o[11:8] ports. CB/CR[11:4] data are outputted from CR_o[15:8] ports. CB/CR[3:0] data are outputted from CB_o[15:12] ports.
VOUT_SEL	[1:0]	VIDEO Output Format setting 00: 444/RGB video output mode 01: 422 video output mode 1x: Through mode (Output Format = Input Format)

5.15.2. **VIDEO 422/444 Conversion REGISTER (VOUT_FIL) (0x8A01)**

	7	6	5	4	3	2	1	0
	Reserved			444FIL_SEL	Reserved	422FIL_SEL		
Type	RO			R/W	RO	R/W		
Default	0	0	0	1	0	0	1	0

Register Field	Bit	Description
444FIL_SEL	4	422to444 conversion characteristic setting. 0: Color pixel is repeated twice at the time of 422 input. 1: 2tap linear interpolation is used at the time of 422 input. Note) 422to444 conversion is bypassed at the time of 444 inputs.
422FIL_SEL	[2:0]	444to422 conversion characteristic setting. 000: 2tap filter is always used. 001: 3tap filter is always used. 010: filter is not used . 011: 2tap filter is used at the time of 444 input, and filter is not used at the time of 422 input. 100: 3tap filter is used at the time of 444 input, and filter is not used at the time of 422 input. 101: 2tap filter is used at the time of 444 input or CSC_on, and filter is not used at the time of 422 input and CSC_off. 11x: 3tap filter is used at the time of 444 input or CSC_on, and filter is not used at the time of 422 input and CSC_off

5.15.3. **VIDEO OUTPUT SYNC MODE REGISTER 0 (VOUT_SYNC0) (0x8A02)**

	7	6	5	4	3	2	1	0
	M3_VSIZE		M3_HSIZE		Reserved		VOUT_MODE	
Type	R/W		R/W		RO		R/W	
Default	0	1	0	0	0	0	1	0

Register Field	Bit	Description
M3_VSIZE	[7:6]	The active period setup of VD_o in Mode3. **Note) Invalid at the time of Mode2**
M3_HSIZE	[5:4]	The active period setup of HD_o in Mode3. **Note) Invalid at the time of Mode2**
VOUT_MODE	[1:0]	Video Sync output mode setting. 00: Not use (for TEST) 01: Not use (for TEST) 10: Mode2 = VD_o and DE_o output timing is almost the same as the timing of inputted HD, VD and DE. 11: Mode3 = VD_o and DE_o are re-generated on the basis of active edge of inputted DE.

5.15.4. **VIDEO OUTPUT SYNC MODE REGISTER 1 (VOUT_SYNC1) (0x8A03)**

	7	6	5	4	3	2	1	0
	Reserved			VOut_Dly				
Type	RO			R/W				
Default	0	0	0	0	1	1	0	0

Register Field	Bit	Description
VOut_Dly	[4:0]	DE_o, DV_o, Y_o, CB_o, CR_o and CBCR_o Output Delay setting in Mode3 00000: With no delay 00001: Delay time is 1 cycle of EN_o 00010: Delay time is 2 cycle of EN_o to 01111: Delay time is 15 cycle of EN_o 1xxxx: Delay time is 16 cycle of EN_o **Note: The maximum delay is 16 cycle of EN_o** **Note: When EN_o is constant H, they are delayed by the cycle of PXCLK.** **Note: Invalid at the time of Mode2**

5.15.5. **VIDEO COLOR SPACE CONVERSION REGISTER (VOUT_CSC) (0x8A08)**

	7	6	5	4	3	2	1	0
	Reserved	VOUT_COLOR_SEL			Reserved		CSC_Mode	
Type	RO	R/W			RO		R/W	
Default	0	0	1	1	0	0	0	0

Register Field	Bit	Description
VOUT_COLOR_SEL	[6:4]	Video output color setting 000: RGB Full 001: RGB Limited 010: 601YCbCr Full 011: 601 YCbCr Limited 100: 709 YCbCr Full 101: 709 YCbCr Limited 110: Range conversion (Full→Limited) 111: Range conversion (Limited→Full) **Note) This setup becomes effective only when CSC_MODE is set as 2 'b01 or 2' b10.**
CSC_Mode	[1:0]	CSC setting 00: CSC is turned OFF 01: CSC is turned ON (Built-in coefficient used) 10: CSC ON/OFF auto select (for Toshiba DTV-SoC) When xvYCC or sYCC, or Adobe YCC601 input, CSC is turned off. When an input is except the above, CSC is turned ON (Built-in coefficient used) 11: CSC is turned ON (Host setting coefficient used)

5.15.6. **SCLK FREQUENCY for CSC controller REGISTER 0 (SCLK_CSC0) (0x8A0C)**

	7	6	5	4	3	2	1	0
	SYS_FREQ[7:0]							
Type	R/W							
Default	1	0	0	0	1	0	0	0

5.15.7. **SCLK FREQUENCY for CSC controller REGISTER 1 (SCLK_CSC1) (0x8A0D)**

	7	6	5	4	3	2	1	0
	SYS_FREQ[15:8]							
Type	R/W							
Default	1	0	0	0	1	0	0	0

Register Field	Bit	Description
SYS_FREQ	[15:0]	System clock frequency setting Set System clock frequency setting ÷10000 integer Initial Value: system clock at 50 MHz, 5000 =16'h1388 Ex.) When system clock at 42 MHz, 4200 =16'h1068 **Note: Set up the same value as Address 0x8540 and 0x8541**

5.15.8. **VIDEO CSC Packet Limit REGISTER (CSC_LIMIT) (0x8AB0)**

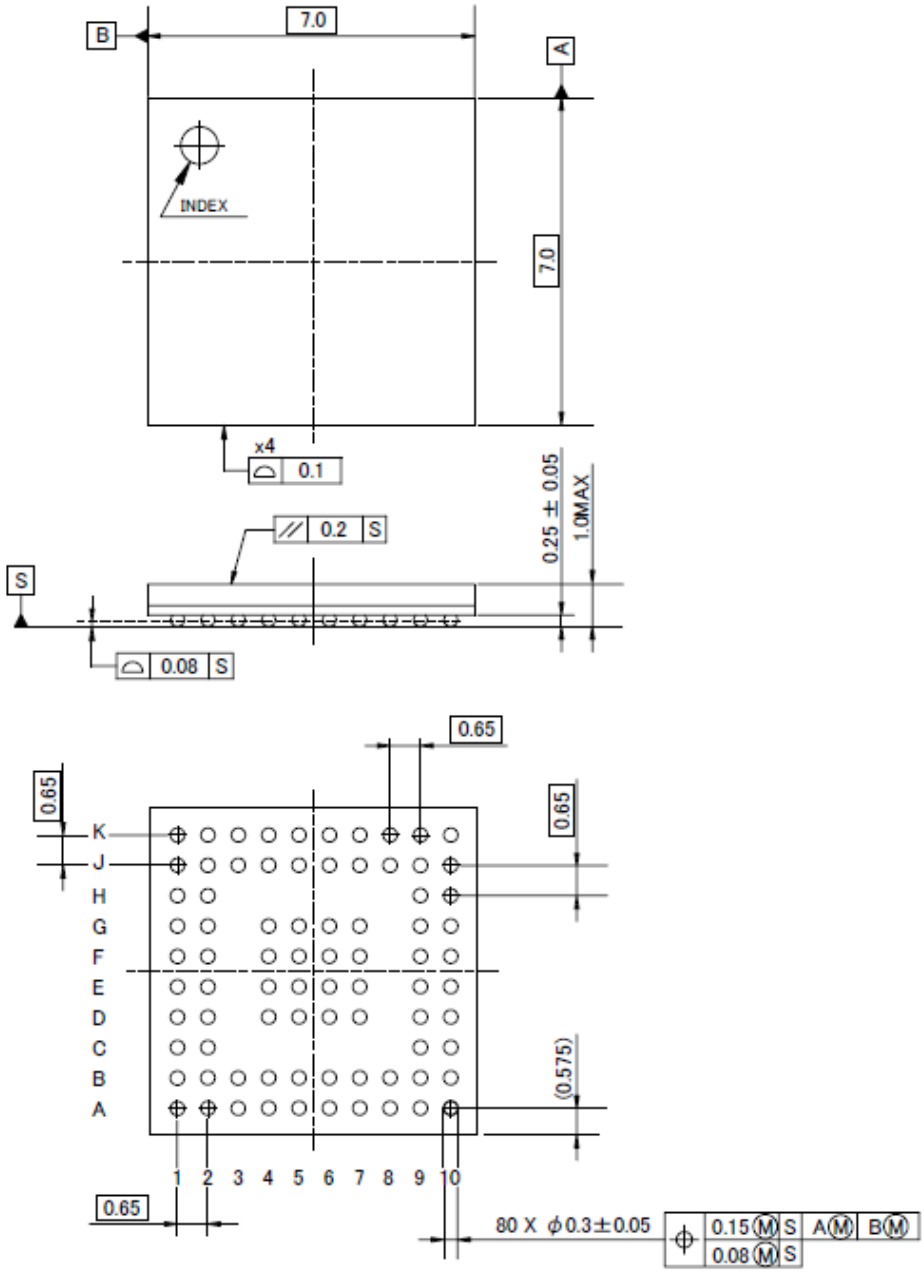
	7	6	5	4	3	2	1	0
	NO_VS_LIMIT2				NO_AVI_LIMIT2			
Type	R/W				R/W			
Default	0	0	1	1	1	1	0	0

Register Field	Bit	Description
NO_VS_LIMIT2	[7:4]	When no VS packet is received during setting value*80ms period, it is judged that VS packet transmission stopped. Note: At 4'b0000 setting, Judgment operation is OFF. **Note: Set up the same value as Address 0x870E [7:4].**
NO_AVI_LIMIT2	[3:0]	When no AVI packet is received during setting value*80ms period, it is judged that AVI packet transmission stopped. Note: At 4'b0000 setting, Judgment operation is OFF. **Note: Set up the same value as Address 0x870B [3:0].**

6. Package

The 80-pin package for TC358870XBG is described in the figures below.

(Unit: mm)



Weight: 67.1 mg (Typ.)

Figure 6.1 TC358870XBG package (P-VFBGA80-0707-0.65-001)

The mechanical dimension of BGA80 package is listed below.

Table 6.1 Mechanical Dimension

Package	Solder Ball Pitch	Solder Ball Height	Package Dimension	Package Height
80-Pin	0.65 mm	0.25 mm	7.0 × 7.0 mm^2	1.0 mm

7. Power Consumption During Typical Operations

- ✧ 1920×1080 @60 fps: 420 mW (Single D-PHY link)
- ✧ 2560×1600 @60 fps: 504 mW (Dual D-PHY link)
- ✧ 3840×2160 @30 fps: 520 mW (Dual D-PHY link)

		VDDC11	VDDIO33	VDDIO18	VDD12_MIPI	VDD33_HDMI	VDD11_HDMI	Total Power	Unit
		1.15	3.3	1.8	1.2	3.3	1.15		
1920x1080 @60Frames	Current (mA)	36	19	1	25	63	68	420	mW
	Power (W)	41	61	2	30	208	78		
2560x1600 @60fps	Current (mA)	60	19	1	50	63	90	504	mW
	Power (mW)	69	62	2	60	207	104		
4Kx2k @30Frames	Current (mA)	70	19	1	52	63	92	520	mW
	Power (mW)	81	62	2	62	207	106		
Power on Reset	Current (mA)	3.8	0.2	3.7	0.3	5.3	36.7	72	mW
	Power (mW)	4.4	0.7	6.6	0.4	17.5	42.2		
Power Reset and Turn Off HDMI Rx PHY*1	Current (mA)	4.0	0.2	3.8	0.3	0	0.3	13	mW
	Power (mW)	4.6	0.7	6.8	0.4	0	0.3		

*1: By clearing register bit 0x8412[6]

Note:

- ✧ Attention about ESD. This product is weak against ESD. Please handle it carefully.
- ✧ TC358870XBG does not perform YCbCr ⇔ YUV conversion. In this document, YCbCr HDMI terminology, is used to describe color space.

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

VSS= 0V reference

Item	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO18	-0.3 to +3.9	V
Supply voltage (3.3V - Digital IO)	VDDIO33	-0.3 to +3.9	V
Supply voltage (1.1V – Digital Core)	VDDC11	-0.3 to +1.8	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD12_MIPI	-0.3 to +1.8	V
Supply voltage (3.3V – HDMIRX Phy)	VDD33_HDMI	-0.3 to +3.9	V
Supply voltage (1.1V – HDMIRX Phy)	VDD11_HDMI	-0.3 to +1.8	V
Input voltage (DSI IO)	V_{IN_DSI}	-0.3 to VDD12_MIPI+0.3	V
Output voltage (DSI IO)	V_{OUT_DSI}	-0.3 to VDD12_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO18+0.3 -0.3 to VDDIO33+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO18+0.3	V
Junction temperature	Tj	125	^{o}C
Storage temperature	Tstg	-40 to +125	^{o}C

8.2. Operating Condition

VSS= 0V reference

Item	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 – Digital IO)	VDDIO18 [note]	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO33	3.0	3.3	3.6	V
Supply voltage (1.1V – Digital Core)	VDDC11	1.1	1.15	1.2	V
Supply voltage (3.3V – HDMIRX PHY)	VDD33_HDMI	3.135	3.3	3.465	V
Supply voltage (1.1V – HDMIRX PHY)	VDD11_HDMI	1.1	1.15	1.2	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD12_MIPI0 VDD12_MIPI1	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	+25	+70	°C
Supply Noise Voltage	V_{SN}	-	-	100	mV_{pp}

Note: VDDIO18 can be used at 1.8V or 3.3V.

8.3. DC Electrical Specification

Standard IO

Item	Symbol	Min	Max	Unit
Input voltage, High level input Note1	V_{IH}	0.70 VDDIO18 Note2	VDDIO18 Note2	V
		0.61 VDDIO18 Note3	VDDIO18 Note3	
		0.61 VDDIO33 Note4	VDDIO33 Note4	
Input voltage, Low level input Note1	V_{IL}	0	0.30 VDDIO18 Note2	V
			0.25 VDDIO18 Note3	
			0.25 VDDIO33 Note4	
Input voltage High level CMOS Schmitt Trigger Note1	V_{IHS}	0.70 VDDIO18 Note2	VDDIO18 Note2	V
		0.61 VDDIO18 Note3	VDDIO18 Note3	
		0.61 VDDIO33 Note4	VDDIO33 Note4	
Input voltage Low level CMOS Schmitt Trigger Note1	V_{ILS}	0	0.30 VDDIO18 Note2	V
			0.25 VDDIO18 Note3	
			0.25 VDDIO33 Note4	
Output voltage High level Note1	V_{OH}	VDDIO18-0.45 Note2	-	V
		VDDIO18-0.6 Note3		
		VDDIO33-0.6 Note4		
Output voltage Low level Note1	V_{OL}	-	0.45 Note2	V
			0.4 Note3 Note4	
Input leak current, High level (Condition: VIN = +VDDIO, VDDIO = 3.6V)	I_{ILH1}	-10	10	μA
Input leak current, Low level (Condition: VIN = 0V, VDDIO = 3.6V)	I_{ILL1}	-10	10	μA

Note1: Each power source is operating within recommended operation condition.

Note2: For IOs related to VDDIO18 and operated at 1.8V range.

Note3: For IOs related to VDDIO18 and operated at 3.3V range.

Note4: For IOs related toVDDIO33.

HDMI DDC Slave IO (DDC_SDA, DDC_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	3.1	5.25	V
Input voltage, Low level input	V_{IL}	0	1.7	V
Output voltage Low level(I_{OL}=8mA)	V_{OL}	-	0.4	V
Input leak current, High level (VIN=VDDIO33)	I_{IH}	-10	10	μA
Input leak current, Low level(VIN=VSS)	I_{IL}	-10	10	μA

HDMI CEC IO (CEC terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	2	VDDIO33	V
Input voltage, Low level input	V_{IL}	0	0.8	V
Output voltage Low level(I_{OL}=8mA)	V_{OL}	-	0.4	V
Input leak current, High level(VIN=VDDIO33)	I_{IH}	-10	10	μA
Input leak current, Low level(VIN=VSS)	I_{IL}	-10	10	μA

I2C IO (I2C_SDA, I2C_SCL terminal)

Item	Symbol	Min	Max	Unit
Input voltage, High level input	V_{IH}	0.7VDDIO18	VDDIO18	V
Input voltage, Low level input	V_{IL}	0	0.3VDDIO18	V
Output voltage Low level (VDDIO18 used at 1.8V,I_{OL}=3mA)	V_{OL}	-	0.2VDDIO18	V
Output voltage Low level (VDDIO18 used at 3.3V,I_{OL}=3mA)		-	0.4	V

9. Timing Definitions

9.1. REFCLK Input Requirement

Clock Requirement

Item	Min	Typ.	Max	Unit
Frequency		40 – 50		MHz
Duty Cycle	40	50	60	%
Jitter	-100	0	100	ppm

9.2. MIPI DSI Timings

Timing specification below has been ported from Draft MIPI Alliance specification for D-PHY version 1.1. Timing defined in Draft MIPI Alliance specification for D-PHY version1.1 has precedence over timing described in the sections below.

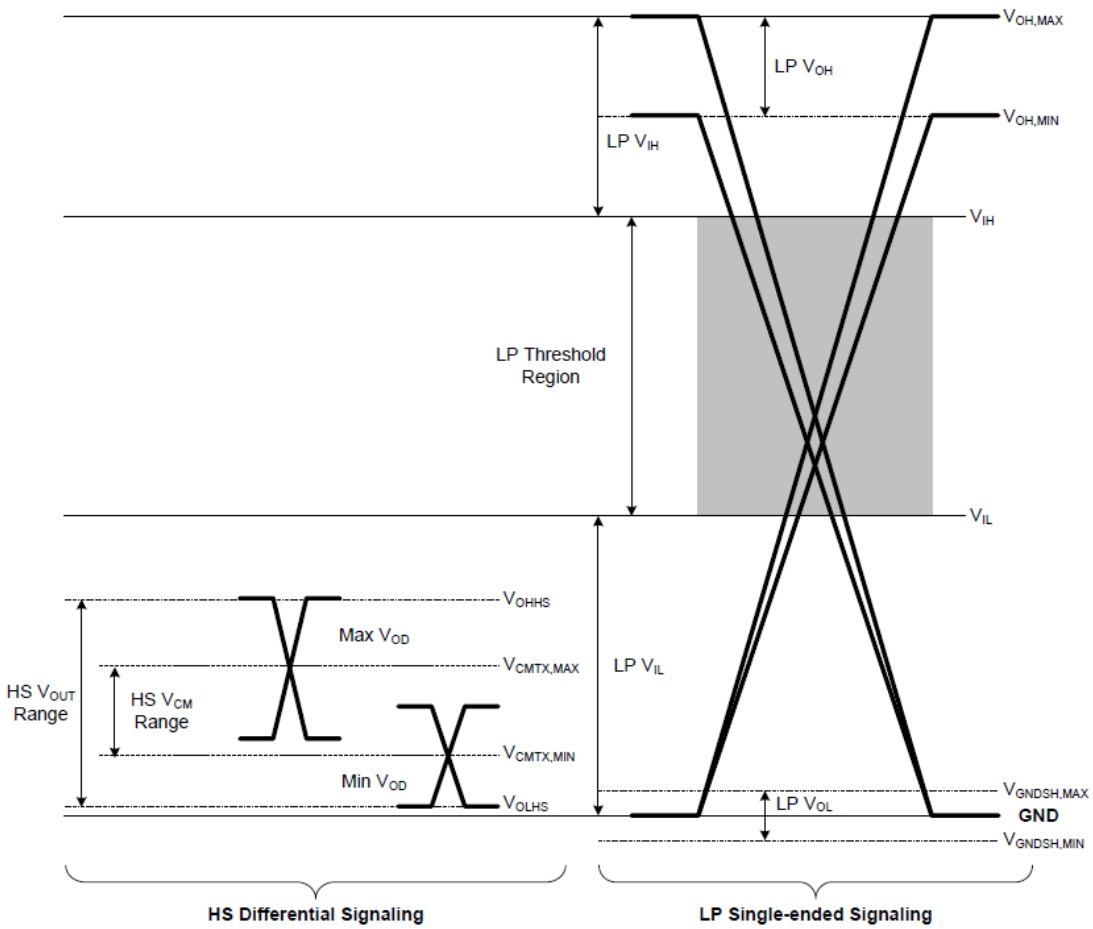


Figure 9.1 D-PHY Signaling Levels

HS Transmitter DC Specifications

Description	Parameter	Min	Typ.	Max	Unit	Notes
HS transmit static common-mode voltage	V_{CMTX}	150	200	250	mV	-

V_{CMTX} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{CMTX(1,0)}\|$	-	-	5	mV	1
HS transmit differential voltage	$\|V_{OD}\|$	140	200	270	mV	-
V_{OD} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{OD}\|$	-	-	14	mV	1
HS output high voltage	V_{OHHS}	-	-	360	mV	-
Single ended output impedance	Z_{OS}	40	50	62.5	Ω	-
Single ended output impedance mismatch	ΔZ_{OS}	-	-	10	%	-

Notes:

1. A transmitter should minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation, and optimize signal integrity.

<< comment >>

These specs are defined only within Link0 or Link1.

Any DC or AC specs of inter-link (between link0 and link1) are not defined.

HS Transmitter AC Specifications

Description	Parameter	Min	Typ.	Max	Unit	Notes
Common-level variations above 450MHz	$\Delta V_{CMTX(HF)}$	-	-	15	mV_{RMS}	-
Common-level variation between 50-450MHz	$\Delta V_{CMTX(LF)}$	-	-	25	mV_{PEAK}	-
20%-80% rise time and fall time	t_R and t_F	-	-	0.3	UI	1
		100	-	-	ps	2

Notes:

1. UI is equal to 1/(2*fh).
2. Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤1 Gbps (UI ≥1 ns), should not use values below 150 ps.

LP Transmitter DC Specifications

Description	Parameter	Min	Typ.	Max	Unit	Notes
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V	-
Thevenin output low level	V_{OL}	-50	-	50	mV	-
Output impedance of LP transmitter	Z_{OLP}	110	-	-	Ω	1

Notes:

1. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.

LP Transmitter AC Specifications

Description		Parameter	Min	Typ.	Max	Unit	Notes
15%-85% rise time and fall time		T_{RLP}/T_{FLP}	-	-	25	ns	1
30%-85% rise time and fall time		T_{REOT}	-	-	35	ns	1, 5, 6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	4
	All other pulses		20	-	-	ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90	-	-	ns	-
Slew rate @ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	-	-	500	mV/ns	1, 3, 7, 8
Slew rate @ C_{LOAD} = 5pF			-	-	300	mV/ns	1, 3, 7, 8
Slew rate @ C_{LOAD} = 20pF			-	-	250	mV/ns	1, 3, 7, 8
Slew rate @ C_{LOAD} = 70pF			-	-	150	mV/ns	1, 3, 7, 8
Slew rate @ C_{LOAD} = 0 to 70pF(Falling Edge Only)			30	-	-	mV/ns	1, 2, 3
Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)			30	-	-	mV/ns	1, 3, 9
Slew rate @ C_{LOAD} = 0 to 70pF(Rising Edge Only)			30 – 0.075 *($V_{O,INST}$ – 700)	-	-	mV/ns	1, 3, 10, 11
Load capacitance		C_{LOAD}	0	-	70	pF	1

Notes:

1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0 and 60 pF on the termination center tap at RX side of the Lane
7. This value represents a corner point in a piecewise linear curve.
8. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
9. When the output voltage is between 400 mV and 700 mV.
10. Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts.
11. When the output voltage is between 700 mV and 930 mV.

LP Receiver DC specifications

Description	Parameter	Min	Typ.	Max	Unit	Notes
Logic 1 input voltage	V_{IH}	880	-	-	mV	1
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	1
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	-
Input hysteresis	V_{HYST}	25	-	-	mV	-

Notes:

1 of 2 calibration process below is required to satisfy this specification.

Calibration process (1)
1)Set ***[Stx0/1_flprx_cal_cntl]*** of ***STX0/1_dsiphy_ctrl0 (0x0590/0x05D0)*** to "0".
2)Set counter value in ***[AutoCalCnt]*** of ***PPI_DPHY_LPRXCALCNTRL (0x0248/0x0448)***.
3)Set ***[D0S_CUTRSEL]*** of PPI***_DPHY_LPRX_THSLD (0x0244/0x0444)]*** ="1".
4)Clear ***[AutoCalDone]*** of ***INIT_INT_STAT (0x0160/0x0360)*** by writing "1".
5)If interrupt is used, write "0" to ***[Mask_LineInitDone]*** of ***INIT_INT_MASK (0x0164/0x0364)***.
6)Start auto calibration by setting "1" to ***[AutoCalStrt]*** of ***PPI_DPHY_LPRXAUTOCALST (0x024C/0x044C)***.
7)Wait until ***[AutoCalDone]*** of ***INIT_INT_STAT (0x0160/0x0360)*** is "1".
8)Read the value from ***[CUTR_LPRXVTHLOW]*** of ***PPI_DPHY_MON (0x0250/0x0450)***.
9)Write the read value of ***[CUTR_LPRXVTHLOW]*** to ***[D0S_LPRXVTHLOW]*** of ***PPI_DPHY_LPRX_THSLD (0x0244/0x0444)***.

Calibration process (2)
1)Set ***[Stx0/1_flprx_cal_cntl]*** of ***STX0/1_dsiphy_ctrl0 (0x0590/0x05D0)*** to "1".
2)Set counter value in ***[AutoCalCnt]*** of ***PPI_DPHY_LPRXCALCNTRL (0x0248/0x0448)***.
3)Start auto calibration by setting "1" to ***[AutoCalStrt]*** of ***PPI_DPHY_LPRXAUTOCALST (0x024C/0x044C)***.
4)Wait more than three times of ***[AutoCalCnt]*** and 16 cycles of **REFCLK** until calibration is completed by internal logic.
5)Read the value from ***[CUTR_LPRXVTHLOW]*** of ***PPI_DPHY_MON (0x0250/0x0450)***.
6)Write the read value of ***[CUTR_LPRXVTHLOW]*** to ***[D0S_LPRXVTHLOW]*** of ***PPI_DPHY_LPRX_THSLD (0x0244/0x0444)***.

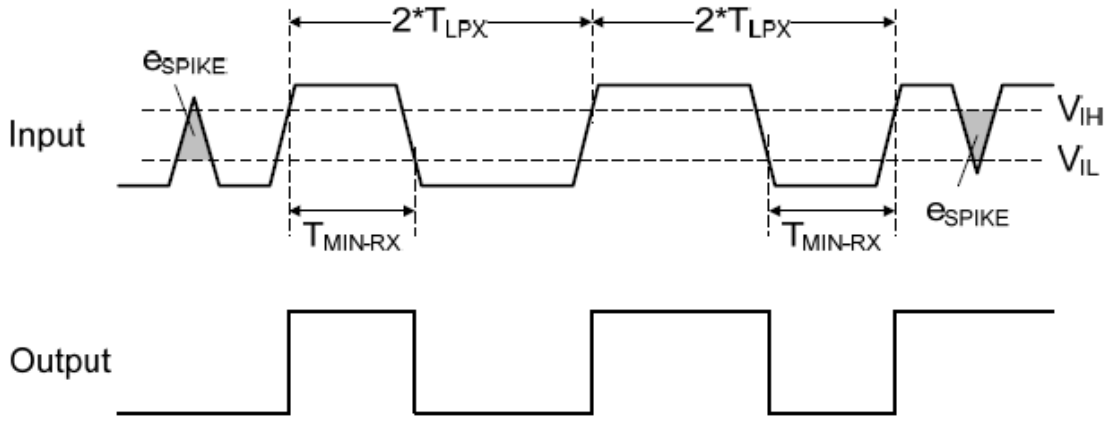


Figure 9.2 Input Glitch Rejection of Low-Power Receivers

LP Receiver AC Specifications

Description	Parameter	Min	Typ.	Max	Unit	Notes
Input pulse rejection	e_{SPIKE}	-	-	300	V·ps	1, 2, 3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	4
Peak interference amplitude	V_{INT}	-	-	200	mV	-
Interference frequency	f_{INT}	450	-	-	MHz	-

Notes:

1. Time-voltage integration of a spike above VIL when being in LP-0 state or below V_{IH} when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF interferers.
4. An input pulse greater than this shall toggle the output.

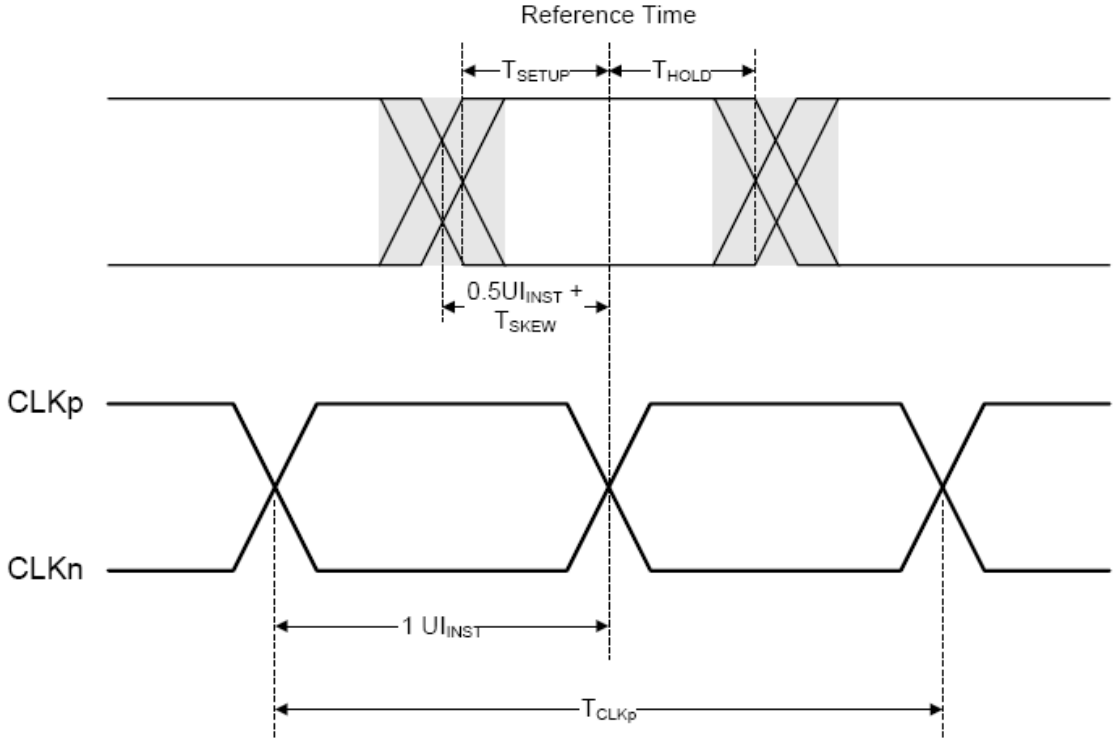


Figure 9.3 Data to clock timing reference

Data-Clock timing specification

Item	Symbol	Min	Typ.	Max	Unit	Notes
Data to clock skew measured at the transmitter	T_{SKEW}	-0.15	-	0.15	UI_{INST}	-
Data to clock setup time at receiver	T_{SETUP}	0.15	-	-	UI_{INST}	-
clock to data hold time at receiver	T_{HOLD}	0.15	-	-	UI_{INST}	-
1 Data bit time (instantaneous)	UI_{INST}	-	-	12.5	ns	-
Period of dual data rate clock	T_{CLKp}	2	2	2	UI_{INST}	-

9.3. I²C Timings

I2C timing specification

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	2	MHz

9.4. HDMI-RX Input

HDMI RX timing specification

Item	Symbol	Min	Typ.	Max	unit	Comment
HDMI Clock Frequency	FIN	25	-	297	MHz	-
HDMI minimum Amplitude	VMIN	150	-	-	mVpp	297 MHz at TP2 Compliance test (TestID 8-5)

9.5. I2S/TDM Timings

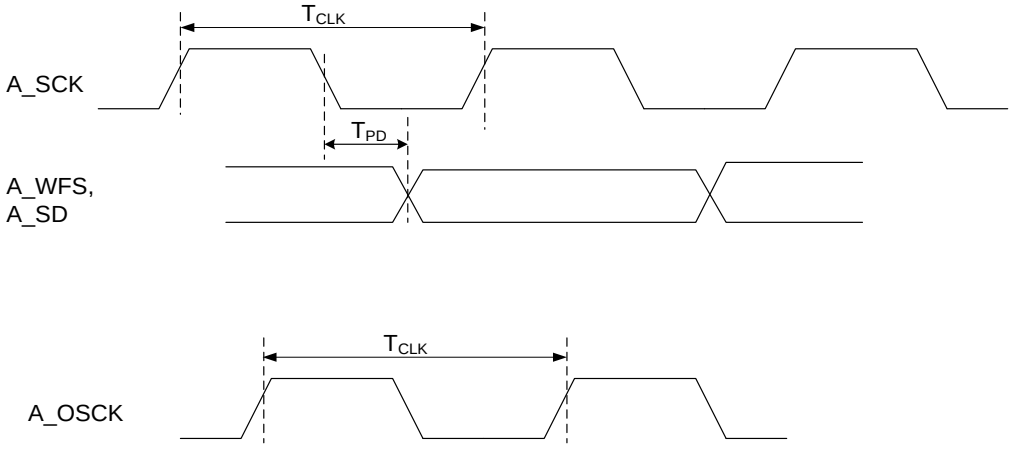


Figure 9.4 I2S/TDM Timing Diagram

I2S/TDM timing specification

Item	Symbol	Min	Typ.	Max	Unit
Propagation Output Delay	T_{PD}	0	-	6	ns
Clock Period	T_{CLK}	20	-	-	ns

Notes: Above timing are for 15pf load on all I2S/TDM signals

10. External Circuit Recommendation

10.1. I2C Slave address definition

INT terminal is multiplexed with configuring function of I2C Slave address. During **RESET** asserted, **INT** becomes input and detects the polarity. After reset deasserted it becomes **INT** function (output) automatically. Pull up or pull down this terminal by 10kohm resister externally.

If pulled up, then I2C Slave address becomes 0x1F

If pulled down then I2C Slave address becomes 0x0F

10.2. HDMI

DDC_SDA and **DDC_SCL** are pulled up to +5V power line and +5V power line is also pulled down for **DDC_SDA** and **DDC_SDL** to be fixed low when +5V power is disabled.

Below figure illustrates example DDC interface connections.

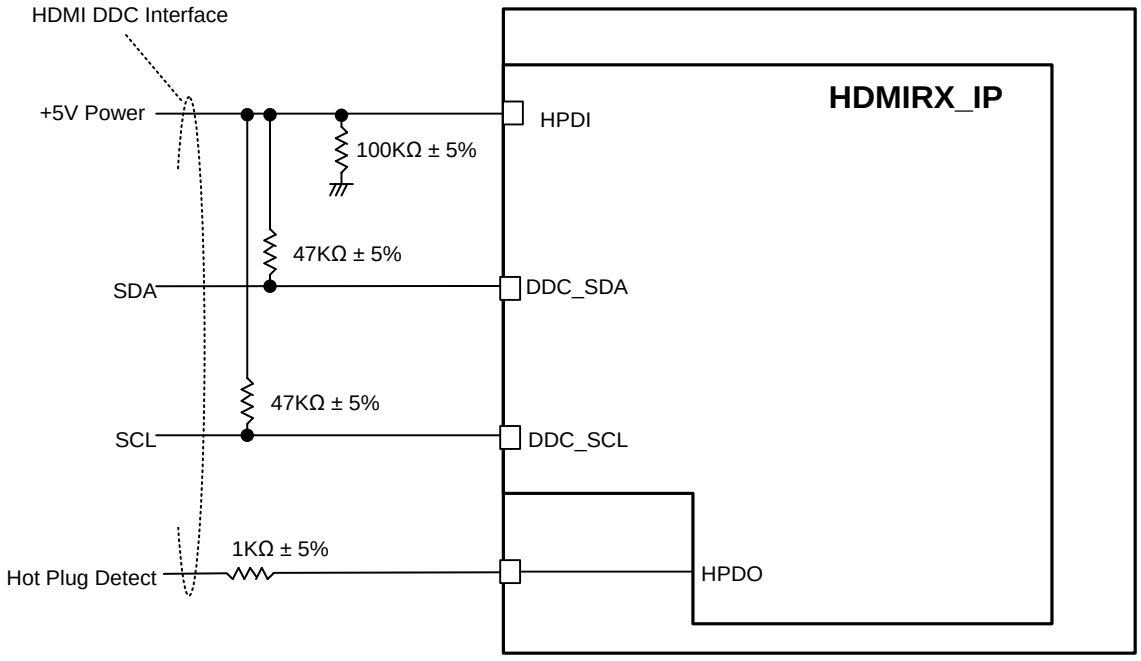


Figure 10.1 Example of DDC I/F Connection

The automatic adjustment function of terminus resistance is attached to HDMI-Rx.

Therefore, connect 2kΩ±1% of reference resistance between **VDD33_HDMI** and **REXT**.

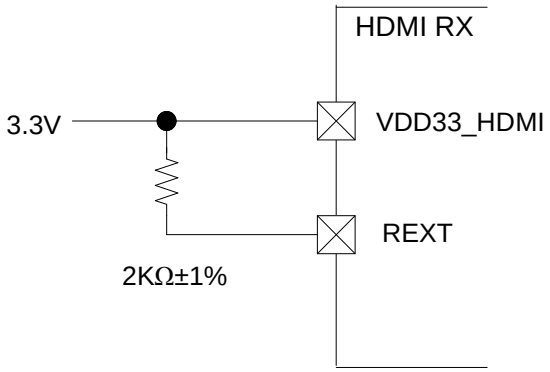


Figure 10.2 Connection of REXT resistance

10.3. Audio PLL

The Audio PLL external terminal connections used in the Audio clock generation are shown in the Figure below.

In **DAOUT** output (PLL input), a low pass filter is installed in the LSI external area.

In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

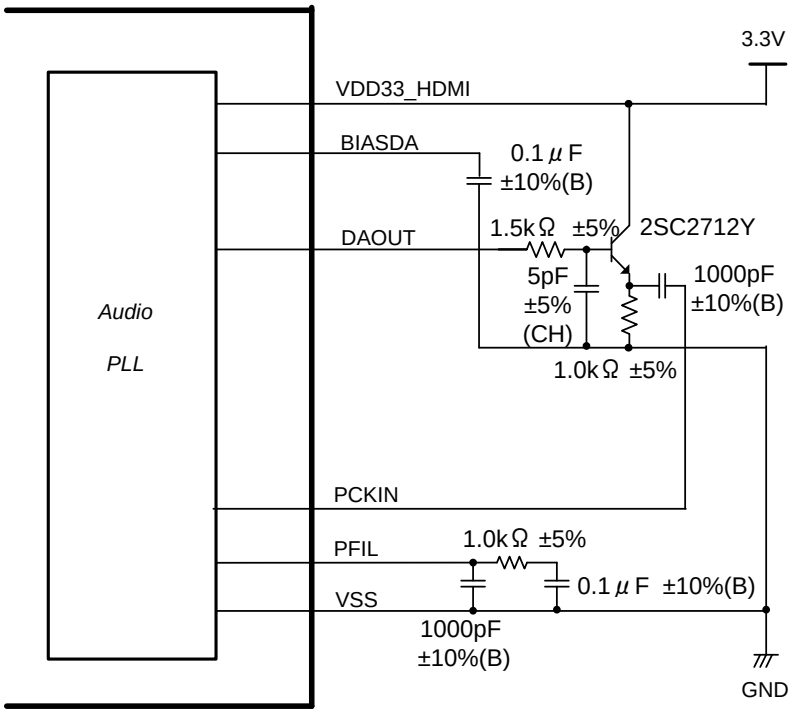


Figure 10.3 Audio Clock External LPF circuit block diagram

10.4. Recommended power supply circuit

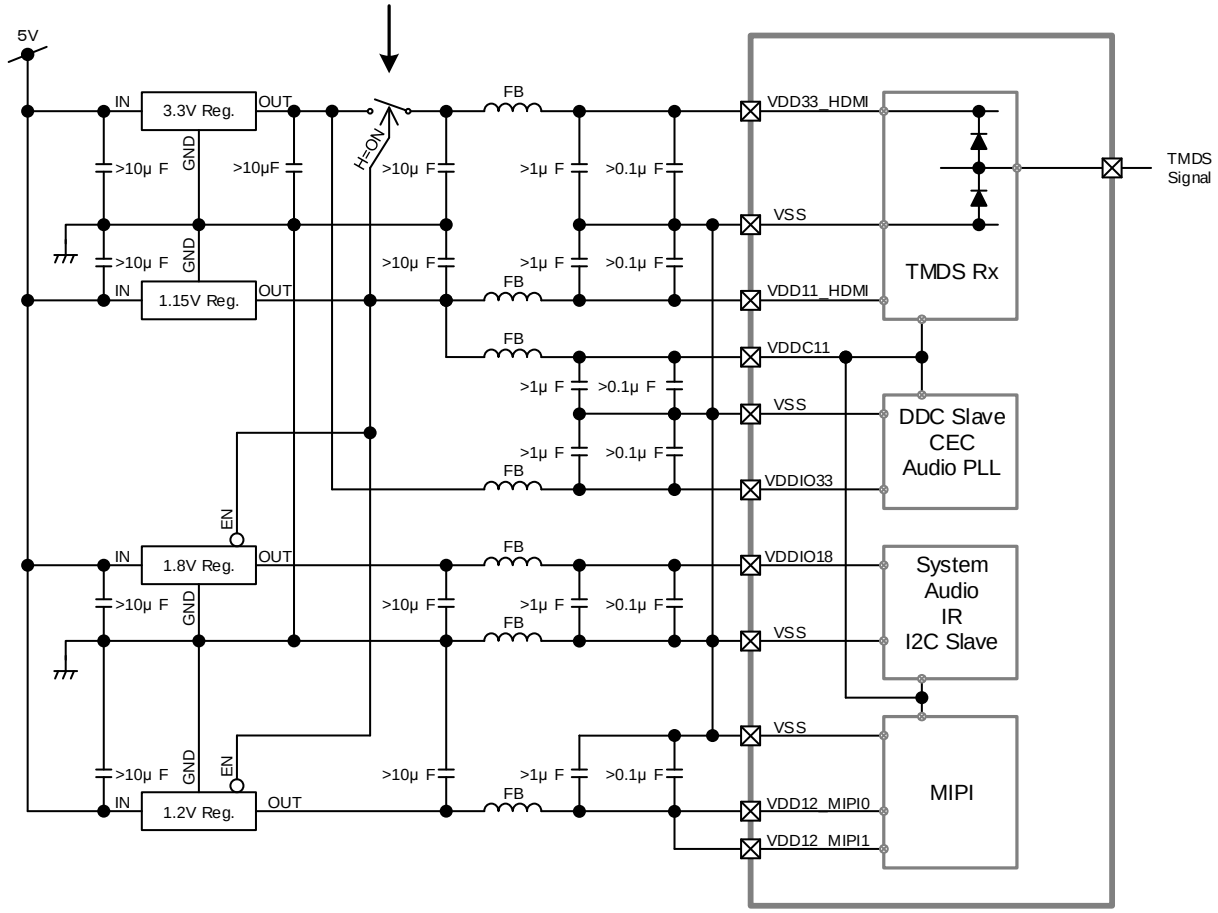
Since the ESD protection diode is attached to the TMDS input pin between a power supply/GND, current may flow backwards HDMI-Rx from source apparatus at the time of power supply OFF.

And also VDD33_HDMI power supply should be isolated from another 3.3V power supplies because this backward current also damages them. Below figure is recommend attaching a back flow prevention circuit.

Case (1) External switch circuit

Attach the adverse current prevention switch from a TMDS differential signal.

Since reverse current also gives damage to VDDIO33, this switch shall separate VDD33_HDMI and VDDIO33.

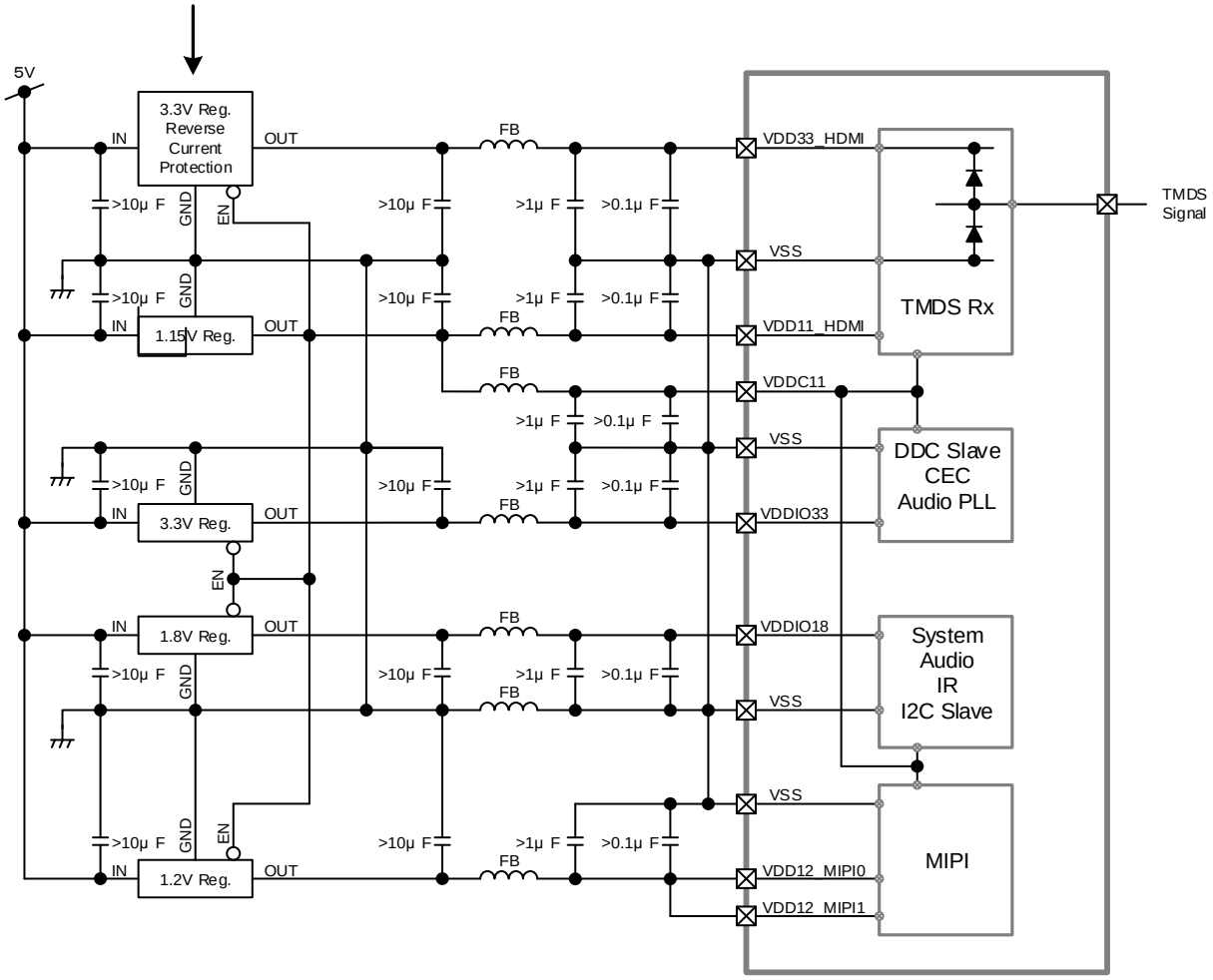


All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

Figure 10.4 Recommended power supply circuit with external switch

Case (2) Regulator with reverse current protection

Apply a current protection regulator to VDD33_HDMI.



All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

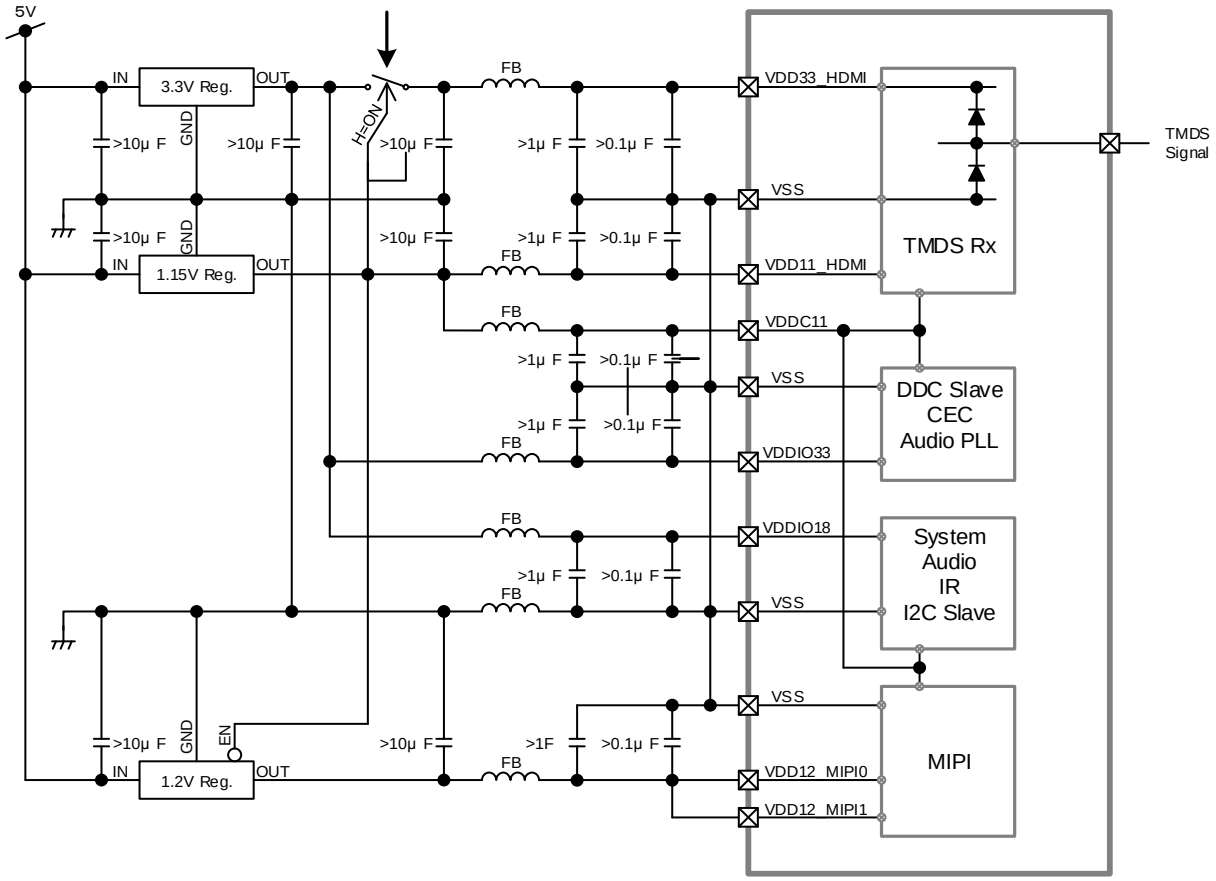
Figure 10.5 Recommended power supply circuit with current protection regulator

Case (3) Use of VDDIO18 at 3.3V range

If VDDIO is applied at 3.3V range, Common regulation is available among VDD33_HDMI, VDIO33 and VDDIO18.

Attach the adverse current prevention switch from a TMDS differential signal.

Since reverse current also gives damage to VDDIO33 and VDDIO18, this switch shall separate VDD33_HDMI and VDDIO33/VDDIO18.



All TC358870 VSSs should be separated at AC level from regulators' VSS with FB(ferrite bead) or another method to attenuate EMI.

Figure 10.6 Recommended power supply circuit at VDDIO18 = 3.3V

11. Revision History

Table 11.1 Revision History

Revision	Date	Description
1.0	2014-08-01	New
1.1	2014-09-18	Remove registers 0x5008 and 0x5088 which are not used Remove Supply Noise Voltage, V_{SN}, from Operation Condition table in section 8.2 Typo fixed 0x04_10 => 0x8410 Add more descriptions for 0x025C, 0x026C, NCO_48F, NCO_44F Remove “address 0x85_0F” and adding note
1.2	2015-01-09	Modify explanation of Figure 3.4 DSI Command Transmission Timing Modify descriptions of Sleep mode in 4 Clock and System Correct 1080p/60fps condition from dual D-PHY to single DPHY in 7 Power Consumption During Typical Operations Add address 0x85C5 (HV_STATUS), 0x85C6 (FV_MIN), 0x85C8 (FV_MAX) 0x85CA (FH_MIN), 0x85CC (FH_MAX) 0x861A (LAYOUT_MONI) 0x8690 (AOUTSEL0), 0x8691 (AOUTSEL1)
1.3	2015-01-28	Remove register 0x870F which is not used Modify description of 0x7000 bit[3] register.

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