Spartan®-6 LX150T Development Kit Hardware Co-Simulation Reference Design User Guide

Preliminary

Version 0.8



Revision History

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Introduction

Xilinx System Generator provides hardware co-simulation, making it possible to incorporate a design running in an FPGA directly into a Simulink simulation. "Hardware Co-Simulation" compilation targets automatically create a bitstream and associate it to a block. When the design is simulated in Simulink, results for the compiled portion are calculated in hardware. This allows the compiled portion to be tested in actual hardware and can speed up simulation dramatically.

The Avnet hardware co-simulation compilation targets provide co-simulation support for Avnet boards using a raw Ethernet connection (called Point-to-point Ethernet in Xilinx System Generator). Point-to-point Ethernet co-simulation provides a straightforward high-performance co-simulation environment using a direct, point-to-point Ethernet connection between a PC and FPGA platform.

Requirements

The software and hardware requirements for this kit are described in the following sections.

Software

The software required to use and run the demonstrations is:

- WindowsXP 32-bit
- Xilinx ISE Design Suite 11.4 : DSP Edition or System Edition[1]
- MathWorks software Release 2009b:

Hardware

The additional hardware required to run these demonstrations is:

- Computer with a minimum of 950 MB to complete a design[2]
- Xilinx® Spartan®-6 LX150T PCI Express Development Kit
- 12V AC/DC adapter
- Xilinx Platform Cable USB II (or equivalent)
- Ethernet cable

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[1] All Xilinx Service Packs are available at www.xilinx.com/download
[2] Refer to www.xilinx.com/ise/products/memory.htm

Setup

Perform the following steps to setup the hardware for running hardware co-simulation.

Connecting the Xilinx Platform Cable USB-II JTAG programming cable

Connect the USB-B end of the cable to the Xilinx Platform Cable USB-II. Connect the flat cable to the Spartan-6 LX150T development board's J9 connector as shown in Figure 1.

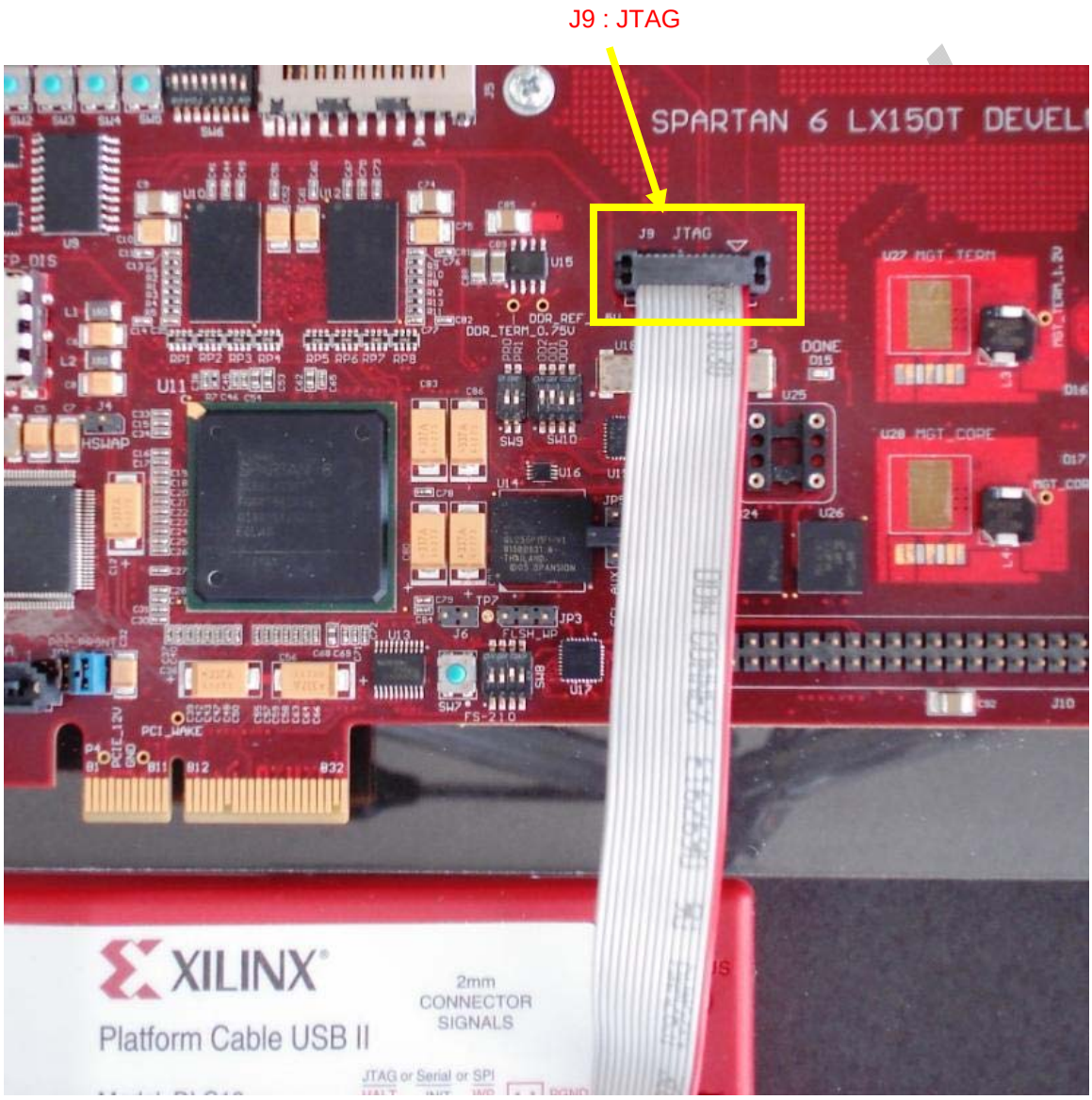

Figure 1 – Setup - Connecting the Xilinx Platform Cable USB-II

Connecting the Ethernet Cable

Connect the Ethernet cable into the Spartan-6 LX150T carrier board's J1 connector as shown in Figure 2. Connect the other end of the end of the Ethernet cable to the PC.

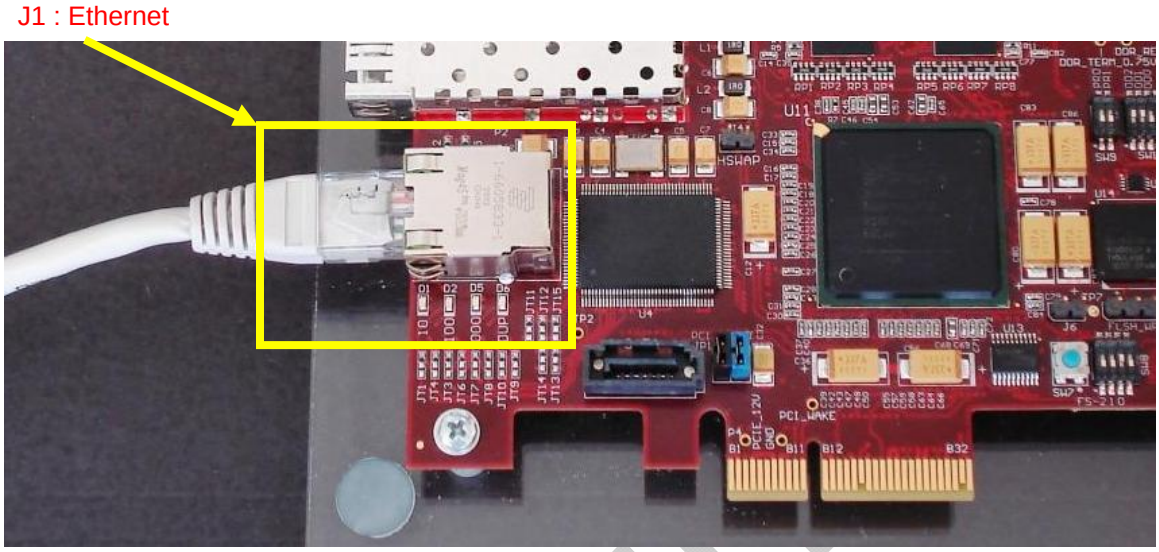

Figure 2 – Setup - Connecting the Ethernet Cable

Connecting the 12V Power Supply

Plug in the 12V power adapter to the local AC power. Ensure that the power switch SW11 is in the off position. Plug the 12V power jack into the Spartan-6 LX150T carrier board's J16 connector. Turn on the power by switching the SW11 to the "ON" position.

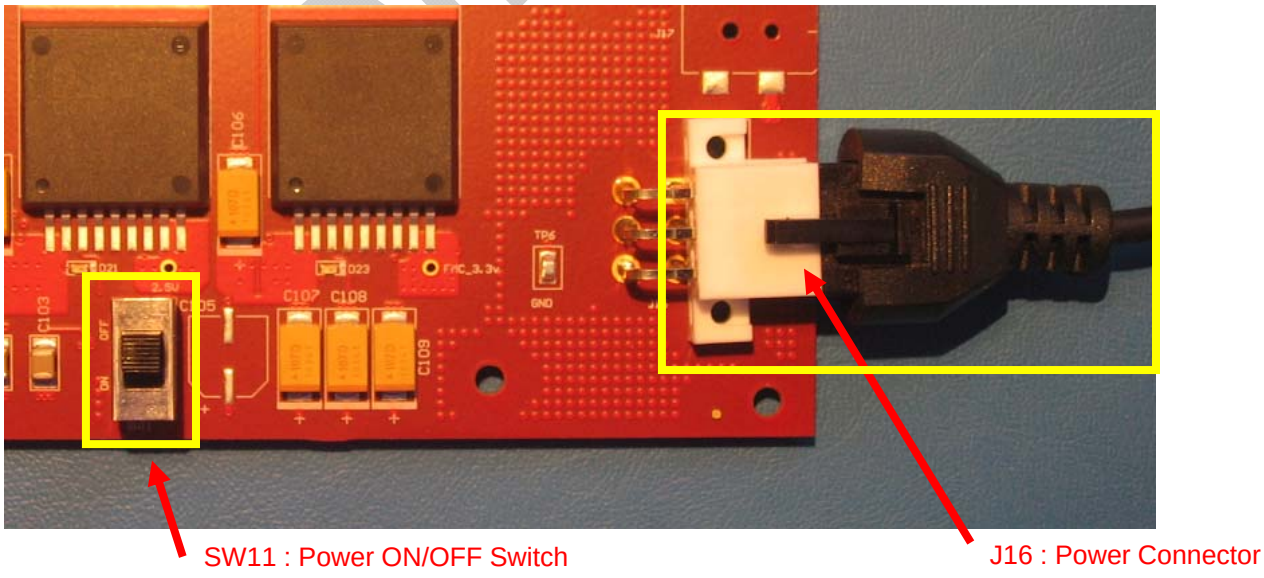

Figure 3 – Setup – Connecting the 12V power supply

Ethernet NIC Configuration

To achieve the maximum bandwidth during hardware co-simulation, your NIC (Network Interface Card) must be configured properly.

Not all NIC manufacturers display their configuration GUI the same way. For this reason, several examples will be shown on how to configure the NIC settings.

To configure the settings of your NIC, perform the following steps:

1) From the **Start** menu, select **Control Panel**, then select **Network Connections**

2) Right-click on your **Local Area Connection**, then select **Properties**.

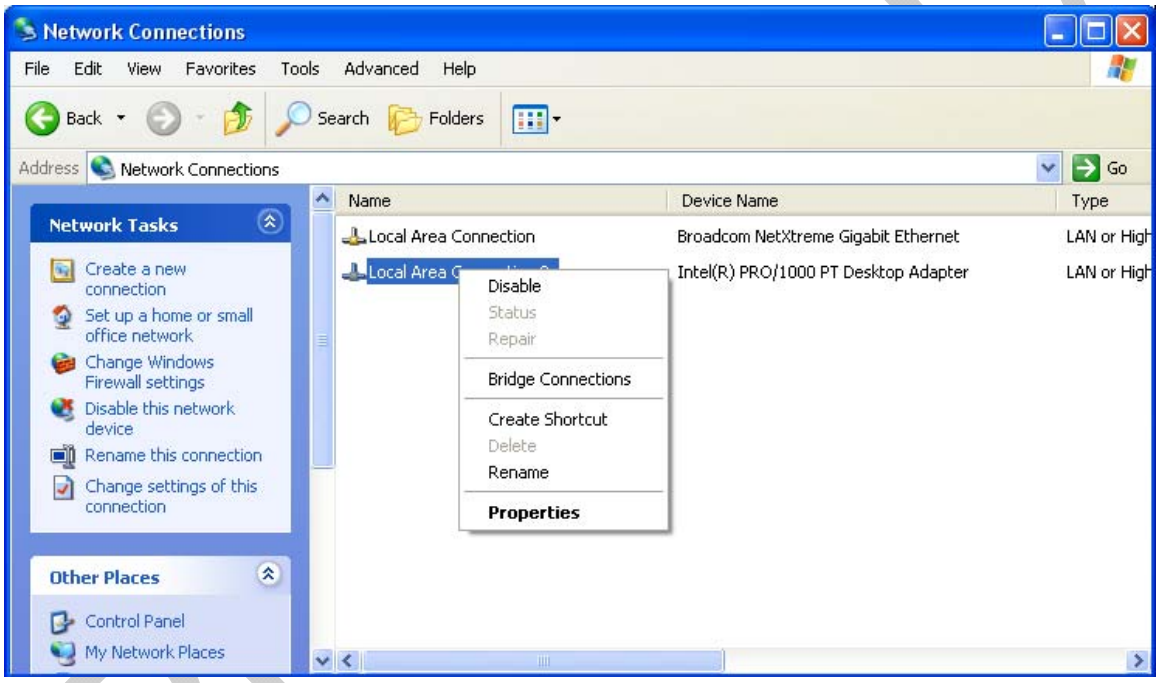

Figure 4 – Network Connections – Local Area Connection Properties

3) Click on the **Configure** button to access the NIC manufacturer's configuration GUI

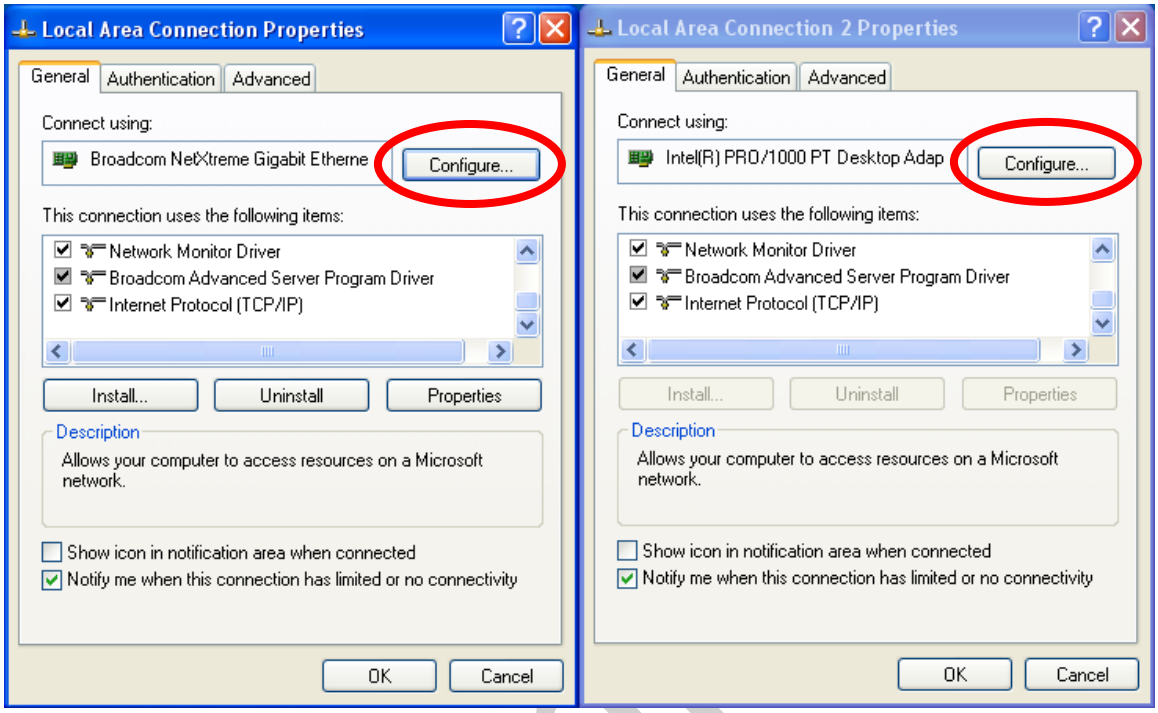

Figure 5 – Accessing the NIC manufacturer's configuration GUI

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4) Xilinx recommends setting **Flow Control** to **Auto**

a. Under the **Advanced** tab, select **Flow Control** and select **Auto** as shown below

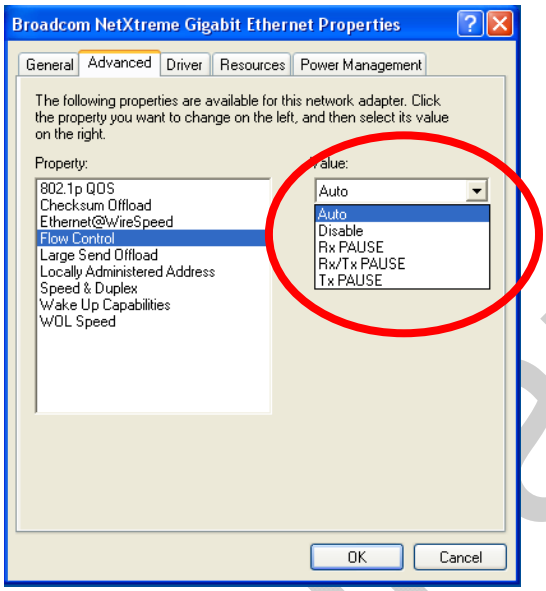

Figure 6 – Flow Control – Auto

b. If you don't have any **Auto** choice available, as shown in the following examples, then select **Generate & Respond**

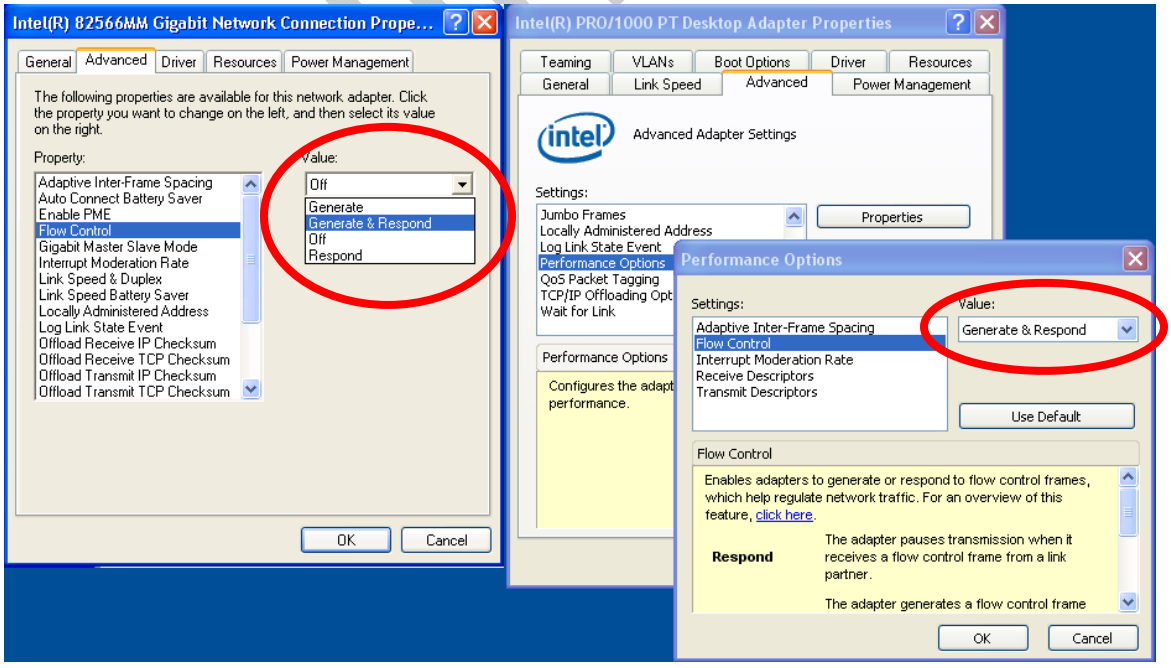

Figure 7 – Flow Control – Generate & Respond

5) Xilinx recommends setting **Speed & Duplex** to **Auto**

   a. Under the **Advanced** tab, select **Speed & Duplex** and select **Auto** as shown in the first example. This setting could also be found in the **Link Speed** tab as shown in the second example.

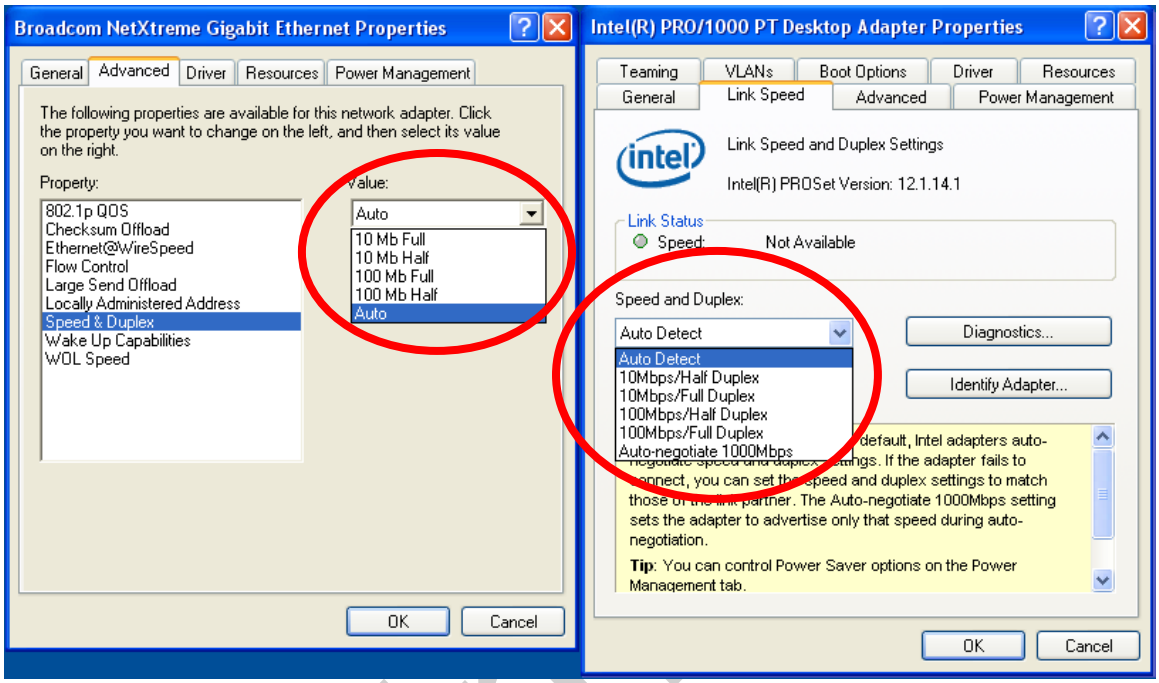

Figure 8 – Speed & Duplex – Auto

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6) For boards which support 1Gbps bandwidth, enabling the **Jumbo Frames** setting is strongly recommended to maximize the bandwidth usage

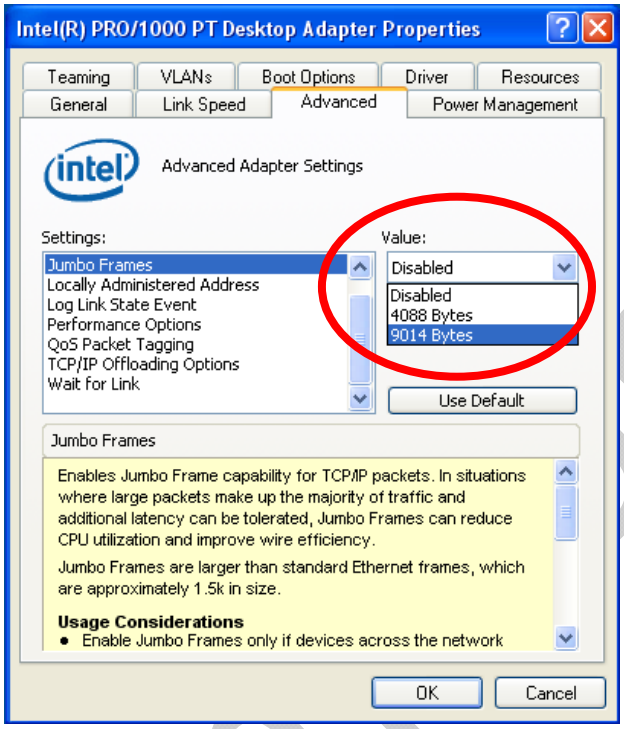

Figure 9 – Jumbo Frames – Enabled

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What is Xilinx System Generator ?

"System Generator is a DSP design tool from Xilinx that enables the use of The Mathworks model-based design environment Simulink for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies is not required when using System Generator. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file."[3]

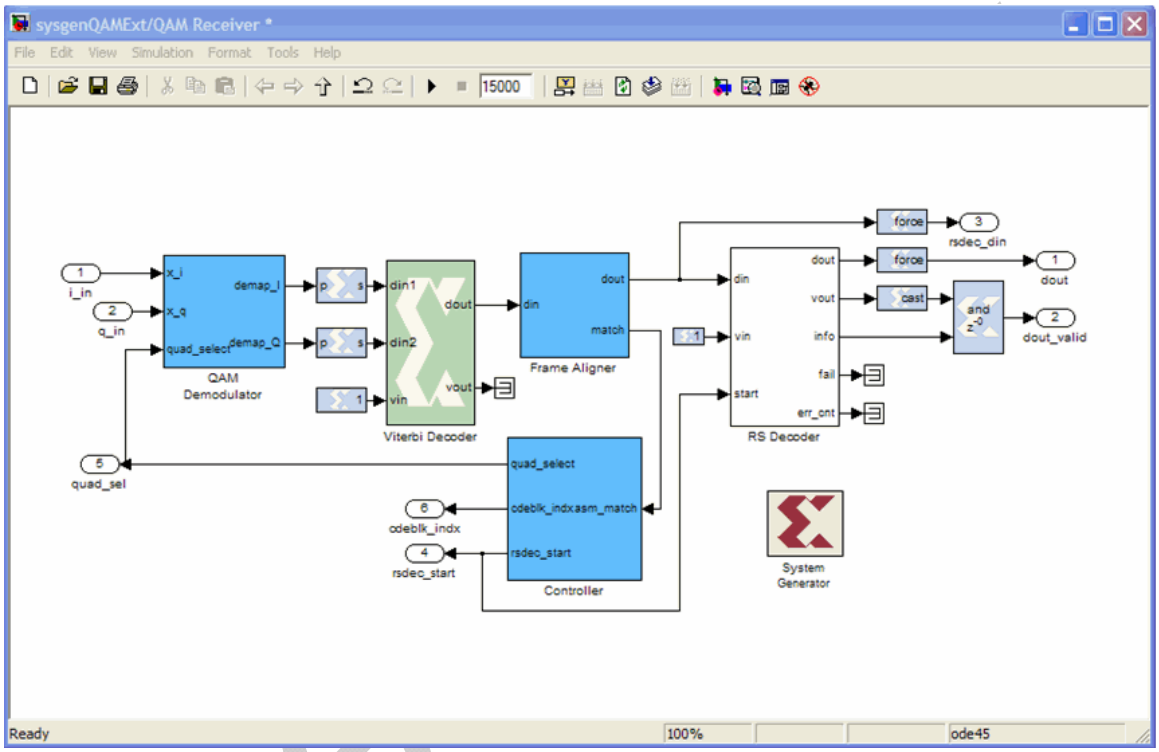

Figure 10 – Xilinx System Generator – design example

For more information on Xilinx System Generator, consult the dedicated page on the Xilinx web site:

http://www.xilinx.com/ise/optional_prod/system_generator.htm

[3] Excerpt from "System Generator for DSP – Getting Started Guide", Release 10.1.3 September, 2008

What is Hardware Co-Simulation ?

"System Generator provides accelerated simulation through hardware co-simulation. System Generator will automatically create a hardware simulation token for a design captured in the Xilinx DSP blockset that will run on one of over 20 supported hardware platforms. This hardware will co-simulate with the rest of the Simulink system to provide up to a 1000x simulation performance increase."[4]

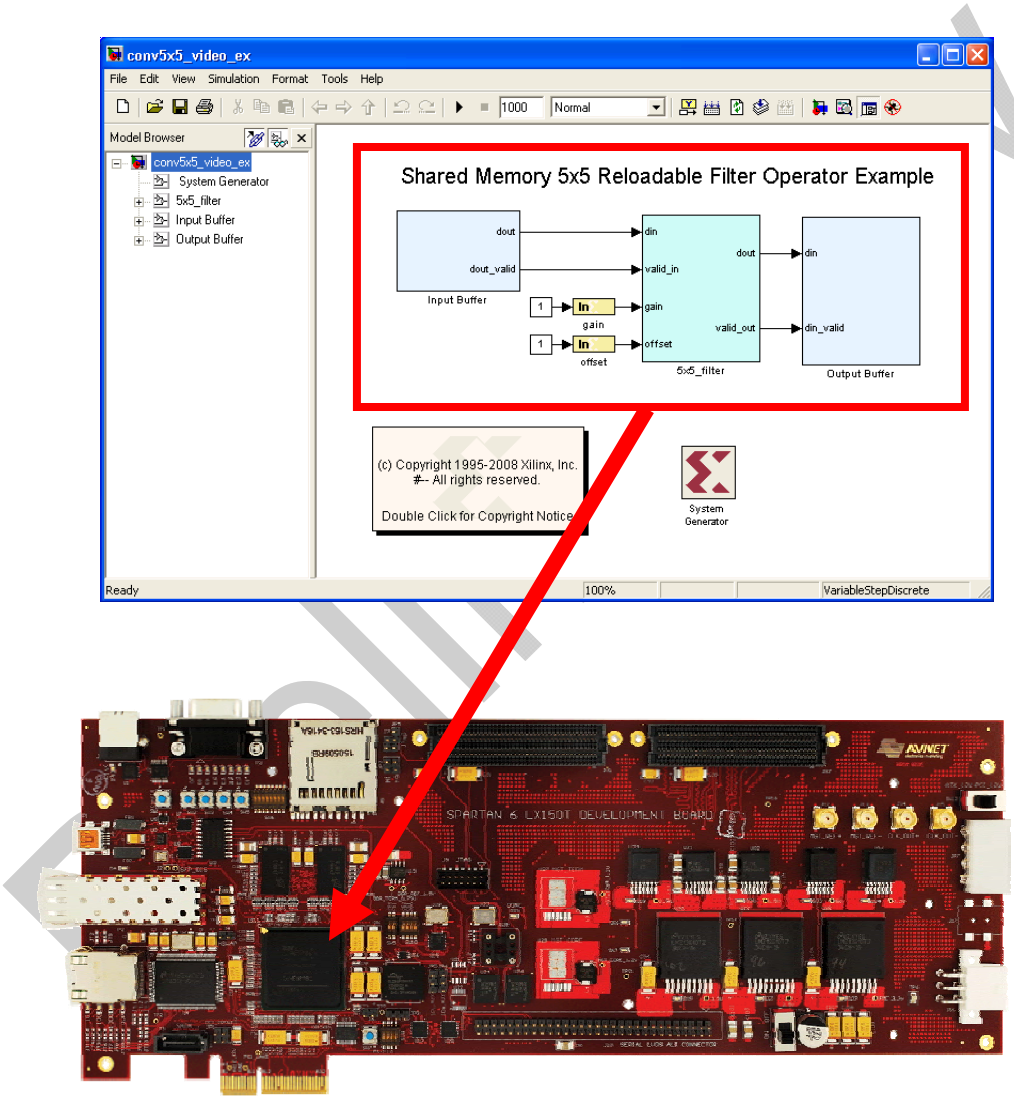

Figure 11 – Hardware Co-Simulation

[4] Excerpt from "System Generator for DSP – Getting Started Guide", Release 10.1.3 September, 2008

What is the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target ?

The Avnet Spartan-6 LX150T hardware co-simulation compilation target provides co-simulation support for the Avnet Spartan-6 LX150T Base Kit using either of the following connections:

- JTAG connection
- raw Ethernet connection (called Point-to-point Ethernet in Xilinx System Generator)

Point-to-point Ethernet co-simulation provides a straightforward high-performance co-simulation environment using a direct, point-to-point Ethernet connection between a PC and FPGA platform.

Once installed, this compilation target will appear in the Xilinx System Generator token as shown below …

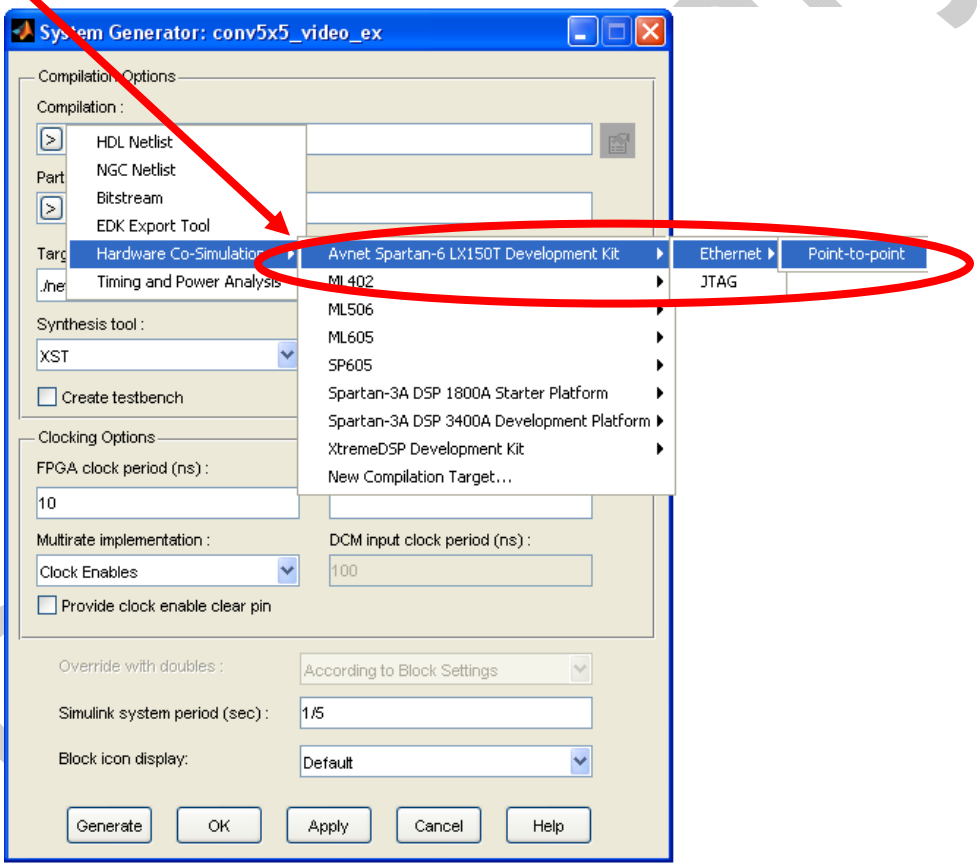

Figure 12 – Hardware Co-Simulation Compilation Targets

How do I install the Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target ?

The Avnet Spartan-6 LX150T Hardware Co-Simulation Compilation Target does not ship with the Xilinx software and must therefore be installed.

In order to install this plug-in, open Matlab and change directory to the following location:

{Installation directory}\HWCOSIM_Installation\

You should see something like the following:

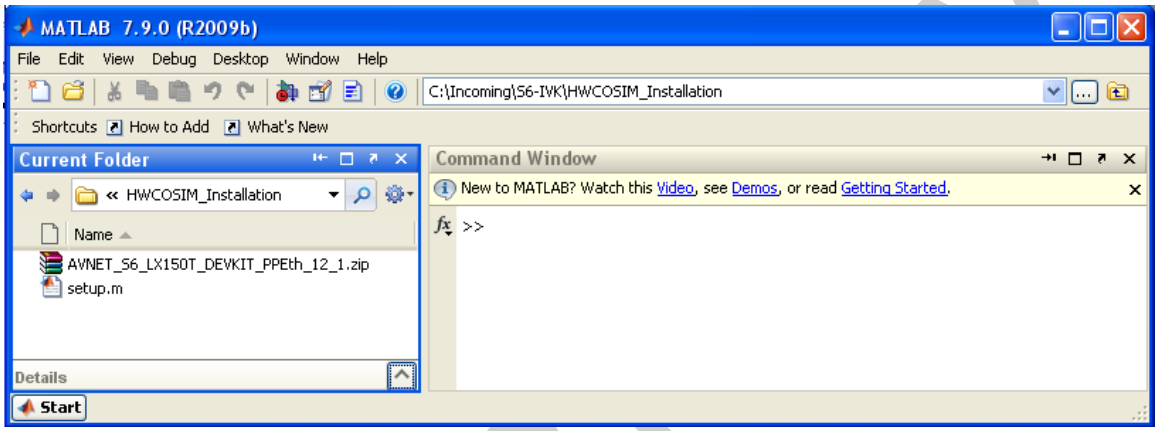

Figure 13 – Hardware Co-Simulation Installation – Contents of directory

Type the “setup” command which will call the “setup.m” script. This will install the hardware co-simulation compilation target for each of the supported Avnet boards.

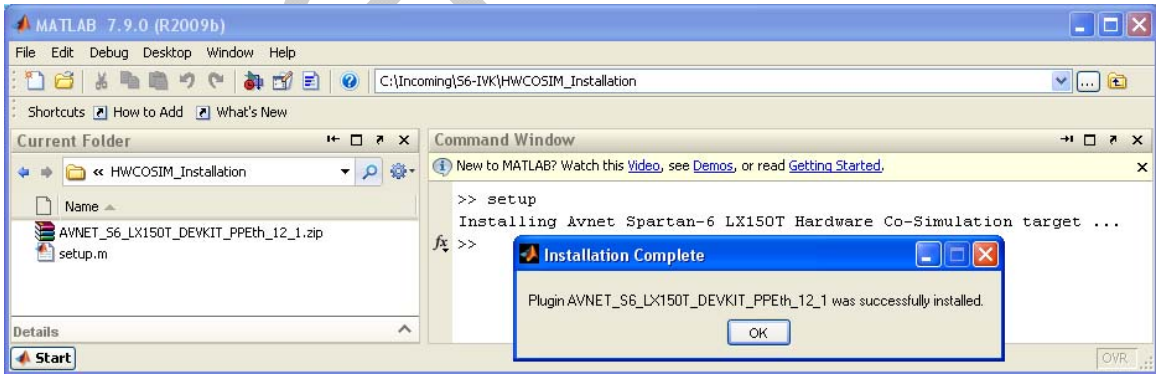

Figure 14 – Hardware Co-Simulation Installation – Executing setup.m script

Using Hardware Co-Simulation to Validate a 5x5 Video Filter Kernel

This section assumes that the hardware has been correctly setup:

- JTAG connected to the S6-LX150T carrier's J9 connector
- Ethernet connected to the S6-LX150T carrier's J1 connector

Refer to the Getting Started Guide [Ref **Error! Reference source not found.**] for information on setting up the IVK hardware. If the demo fails to run, see the Error! Reference source not found. Appendix.

Now that the hardware co-simulation target is installed, we will demonstrate how to use it to validate a 5x5 video filter kernel.

Open Matlab and change directory to the following directory:

{XILINX}\DSP_Tools\nt\sysgen\examples\shared_memory\hardware_cosim\conv5x5_video
where {XILINX} is the location where Xilinx was installed (ie. C:\Xilinx\11.1)

Open the **conv5x5_video_ex.mdl** model.

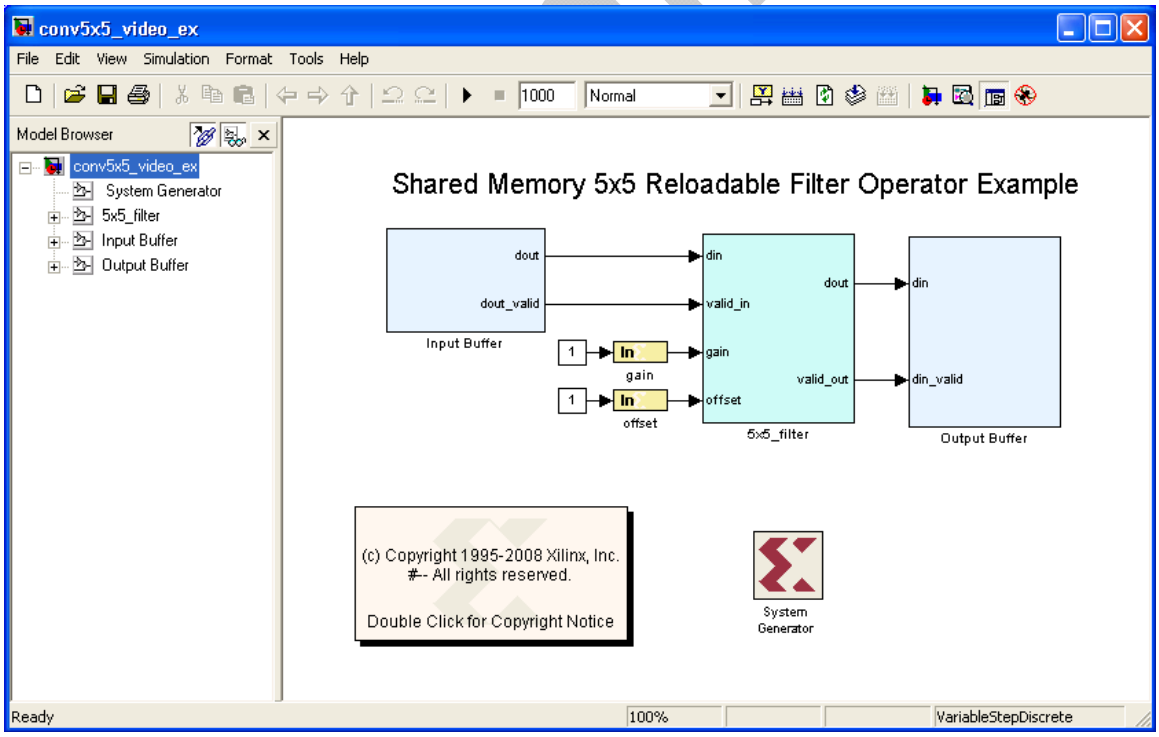

Figure 15 – 5x5 Video Filer Kernel – Opening the model

Double-click on the System Generator block and select one of the Avnet Hardware Co-Simulation compilation targets as show below …

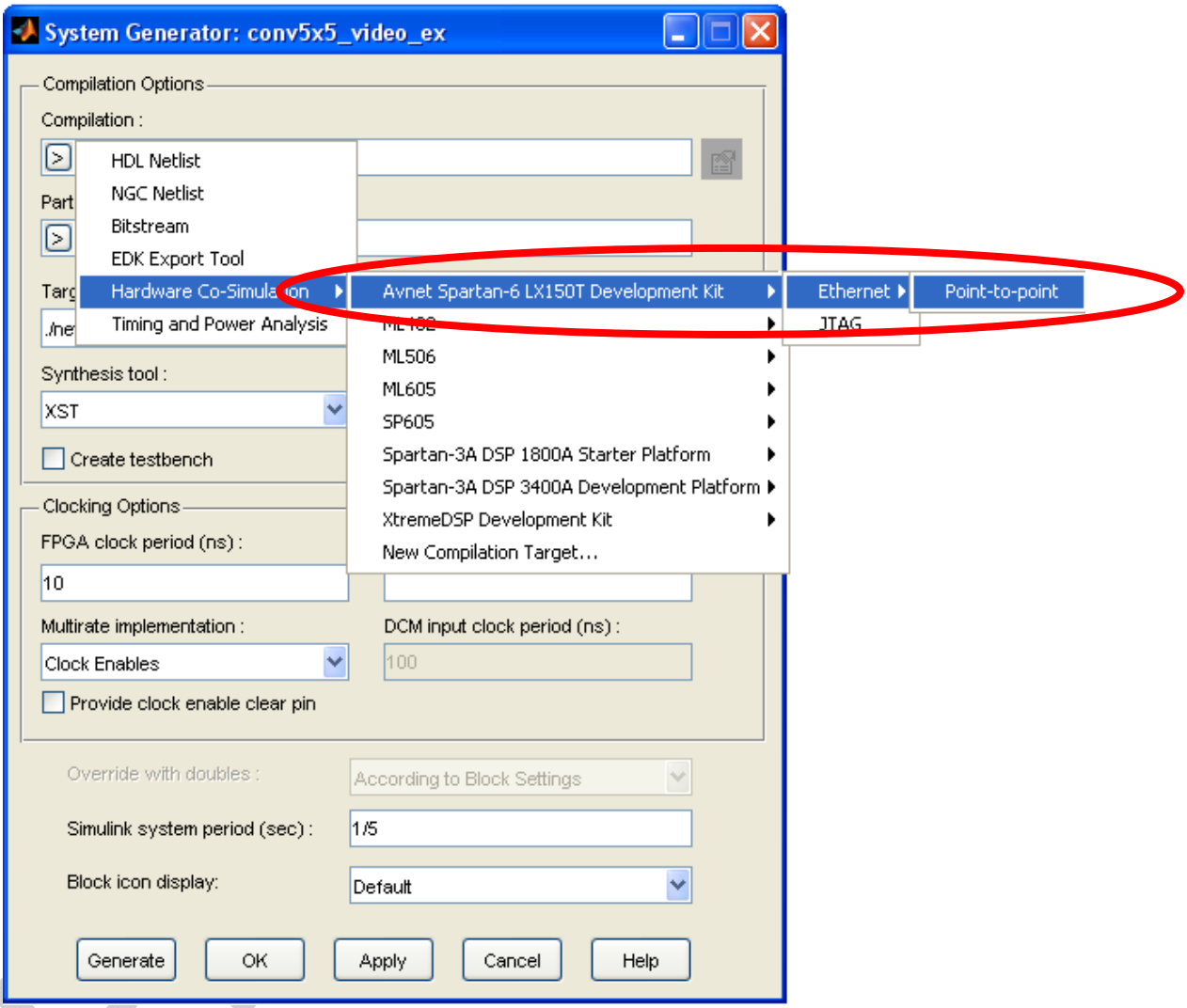

Figure 16 – 5x5 Video Filer Kernel – Selecting the Avnet S6-LX150T target

Note : The Point-to-Point Ethernet hardware co-simulation target will only work with version 12.1 of the Xilinx tools. If you don't have this version yet, select the JTAG hardware co-simulation target instead.

Click on Generate to build the design for hardware co-simulation … this will take a while, so be patient …

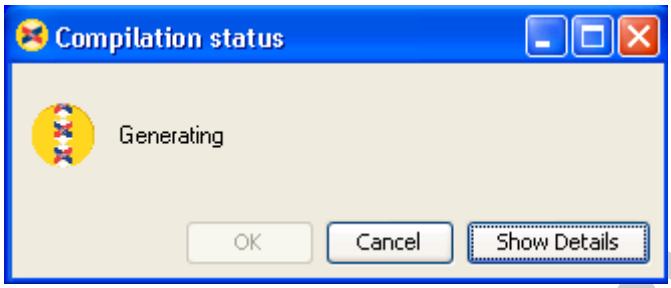

Figure 17 – 5x5 Video Filer Kernel – Generating

When the build process completes, a hardware co-simulation block will appear in a new conv5x5_video_ex_hwcosim_lib.mdl library. Do not close the hwcosim library. Click on the OK button in the Compilation status dialog box.

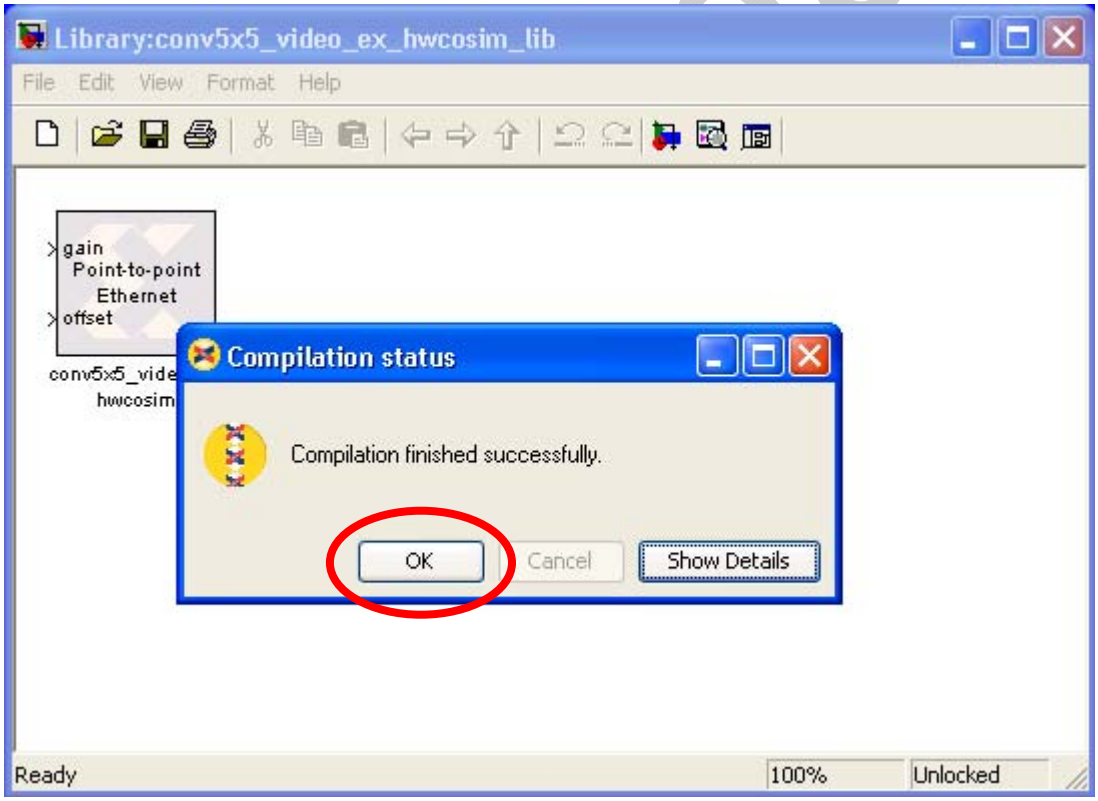

Figure 18 – 5x5 Video Filer Kernel – Hardware Co-Simulation Library

Open the conv5x5_video_testbench.mdl model and drag the “conv5x5_video_ex hwcosim” block into the testbench model as show below …

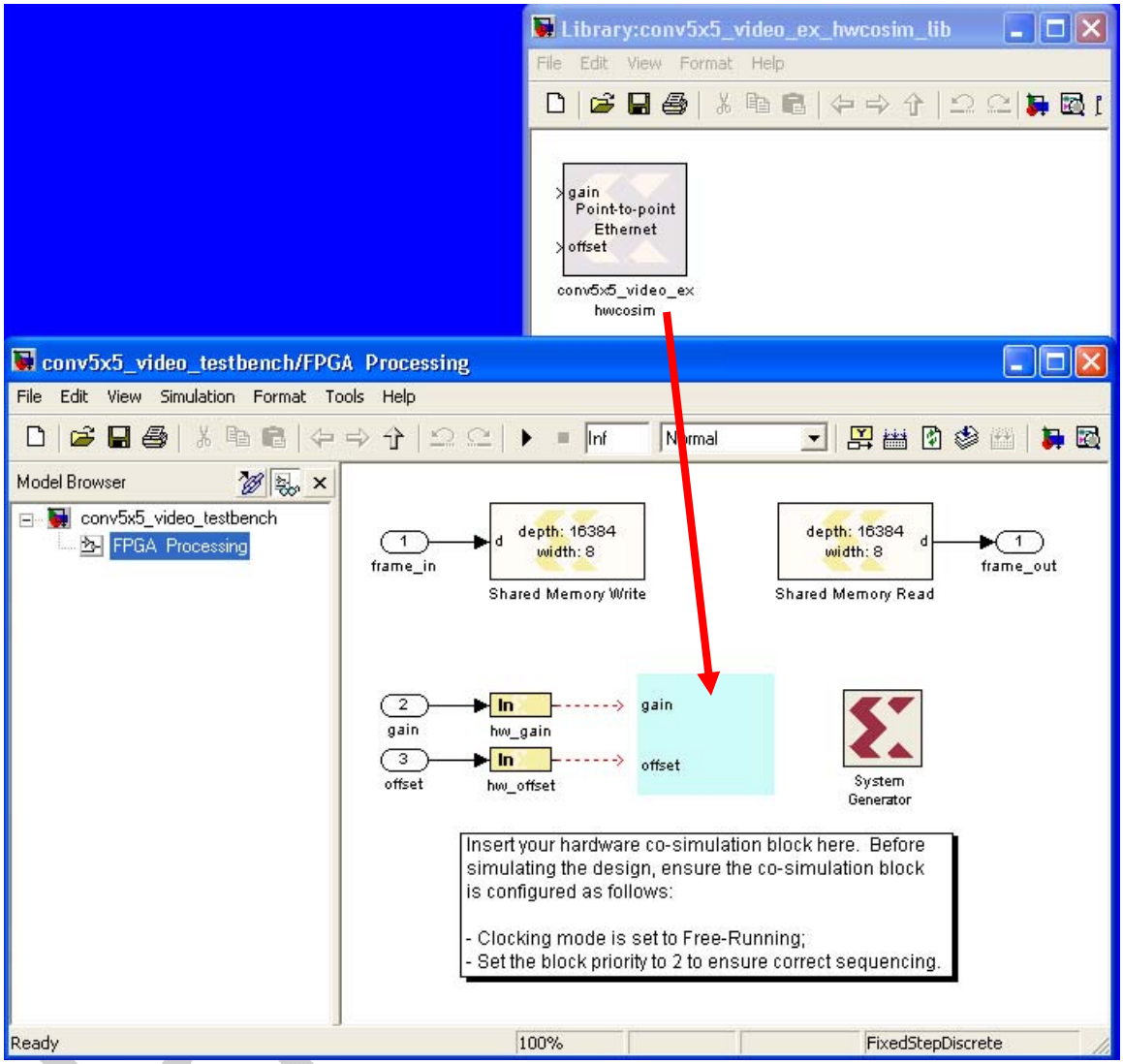

Figure 19 – 5x5 Video Filer Kernel – Instantiating the Hardware Co-Simulation block

Double-click on the “conv5x5_video_ex hwcosim” block, select the **Basic** tab, and set the Clock source to “**Free running**”

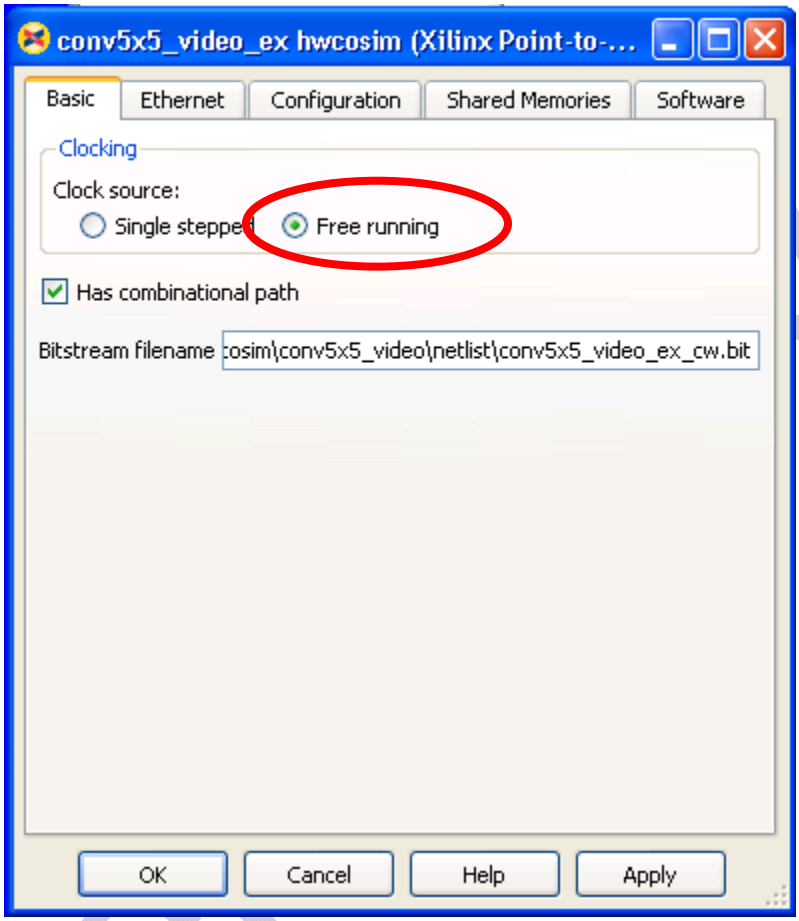

Figure 20 – 5x5 Video Filer Kernel – Basic Configuration

Pre

If you are using JTAG hardware co-simulation, skip this step and proceed to the next page.

If you are using the Point-to-Point Ethernet hardware co-simulation, you need to configure the Ethernet connection.

Select the **Ethernet** tab, and select your PC's Ethernet connection from the **Host interface** drop down list.

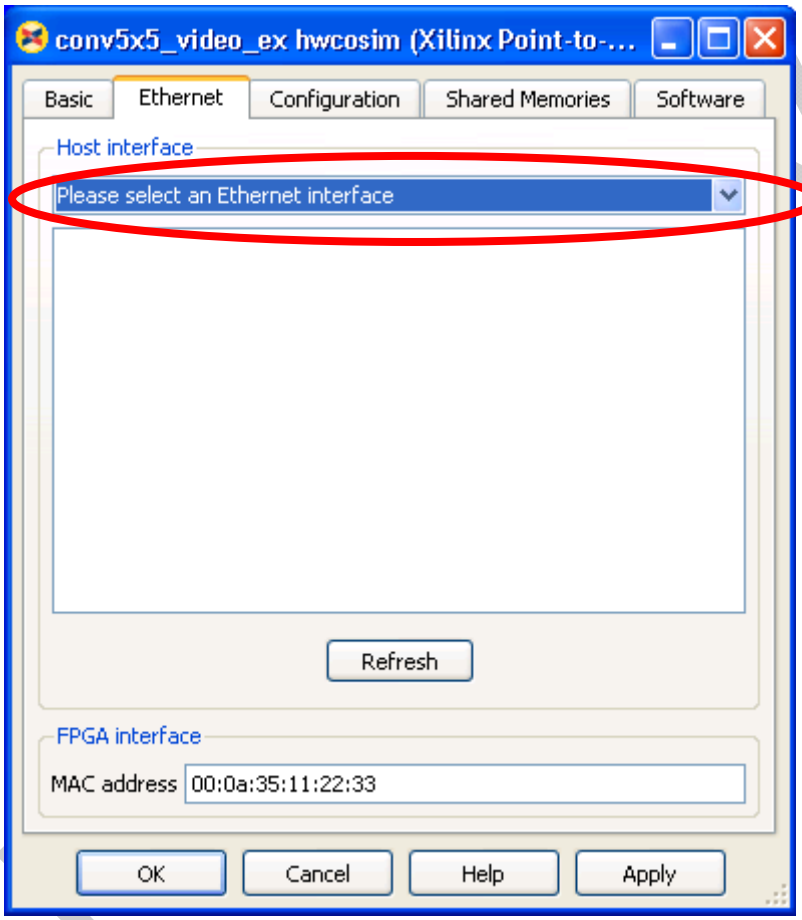

Figure 21 – 5x5 Video Filer Kernel – Ethernet Configuration

Select the **Configuration** tab, and select your Xilinx JTAG cable from the available choices

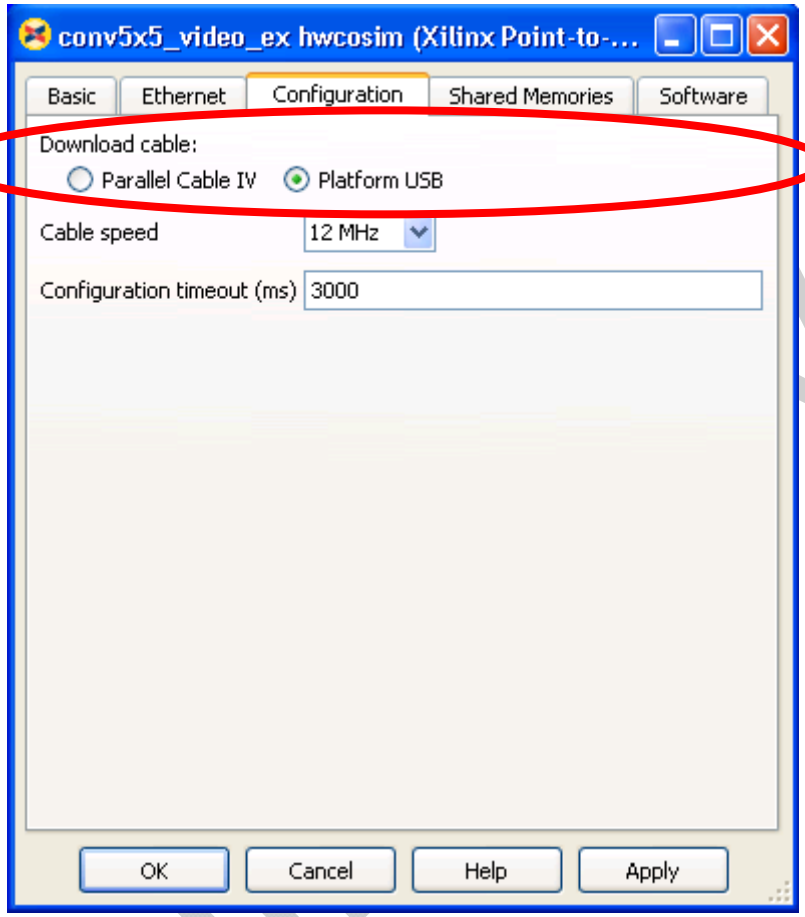

Figure 22 – 5x5 Video Filer Kernel – JTAG Configuration

Click OK to close the “conv5x5_video_ex hwcosim” parameters dialog blox.

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Press the play button to start the hardware co-simulation

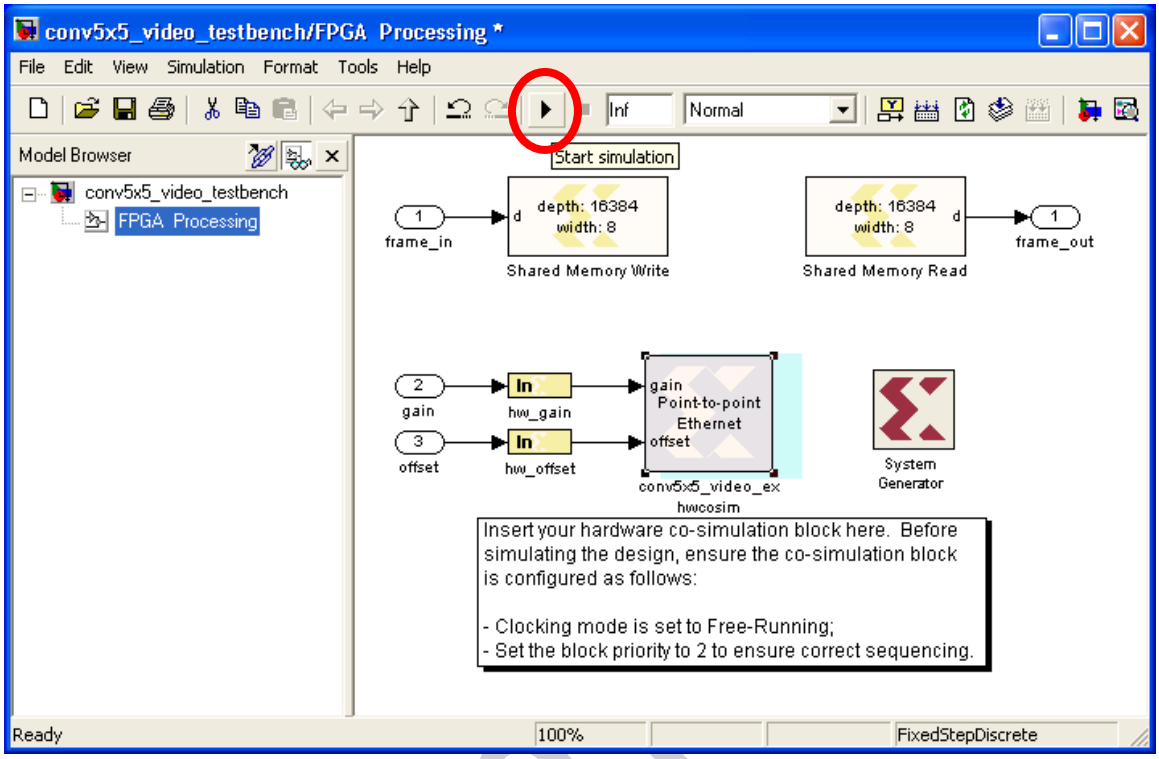

Figure 23 – 5x5 Video Filer Kernel – Starting Co-Simulation

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The simulink model will first download the bitstream via JTAG, then it will establish a link with the FPGA design via Ethernet or JTAG.

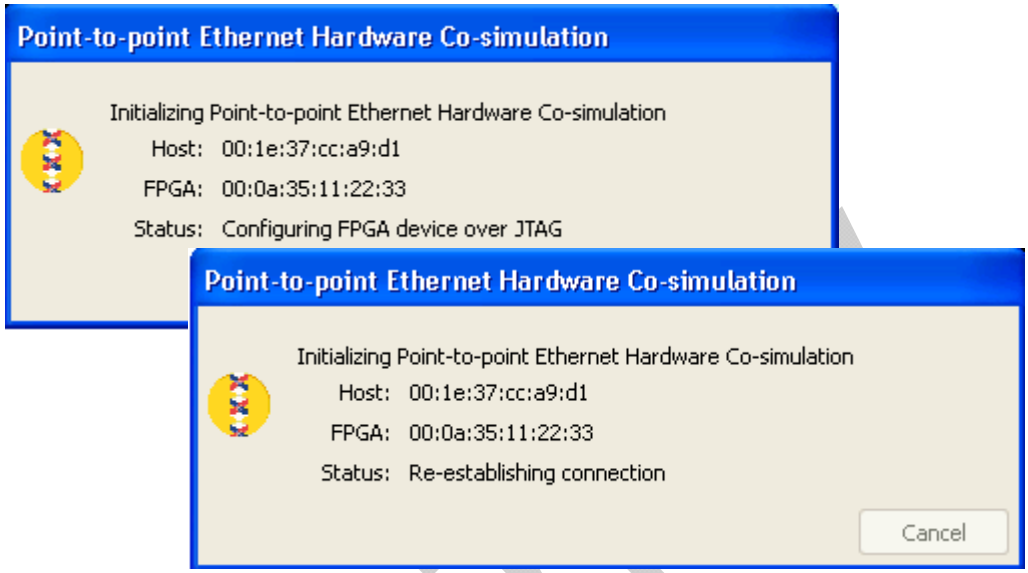

Figure 24 – 5x5 Video Filer Kernel – Initialization Phase

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The model will run the FPGA in the loop co-simulation until the user stops the simulation.

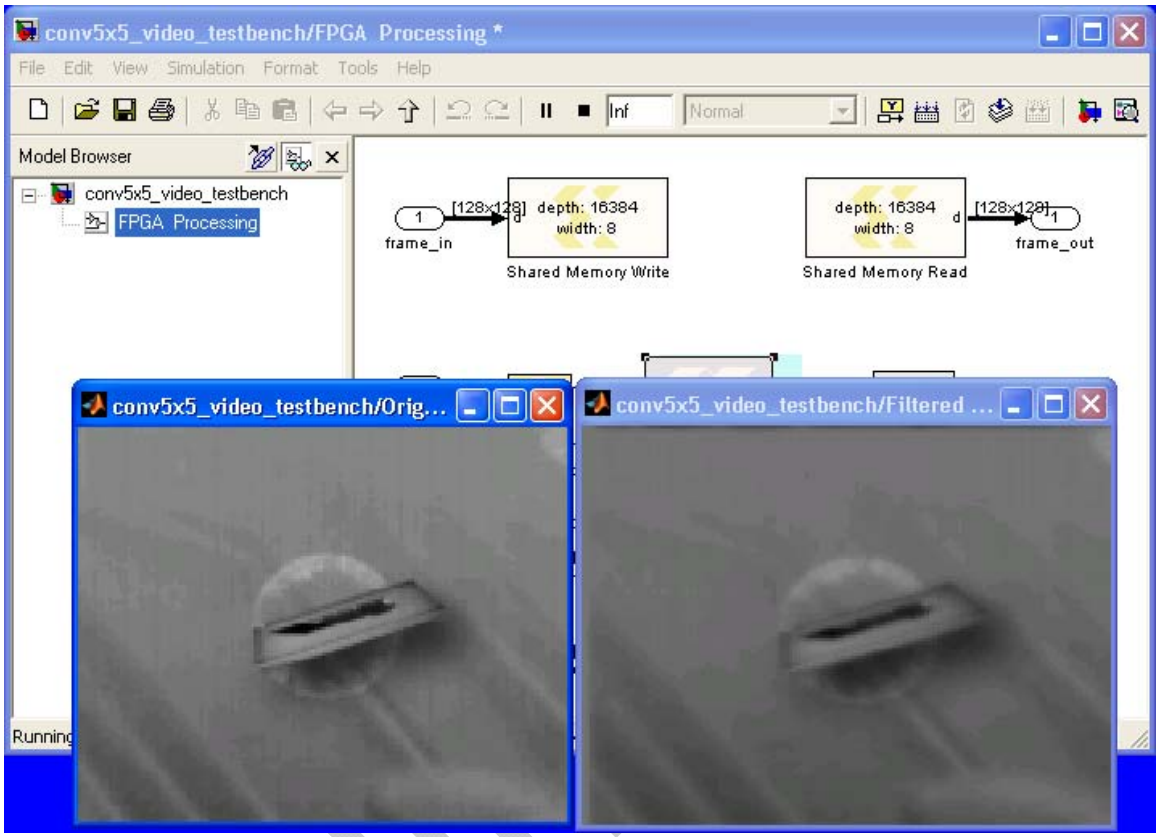

Figure 25 – 5x5 Video Filer Kernel – Co-Simulation Results

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For more information …

For more information on Xilinx System Generator hardware co-simulation, consult the System Generator documentation. This documentation can be accessed in two ways:

From MATLAB,
type the “xlDoc” command to launch the System Generator Help System

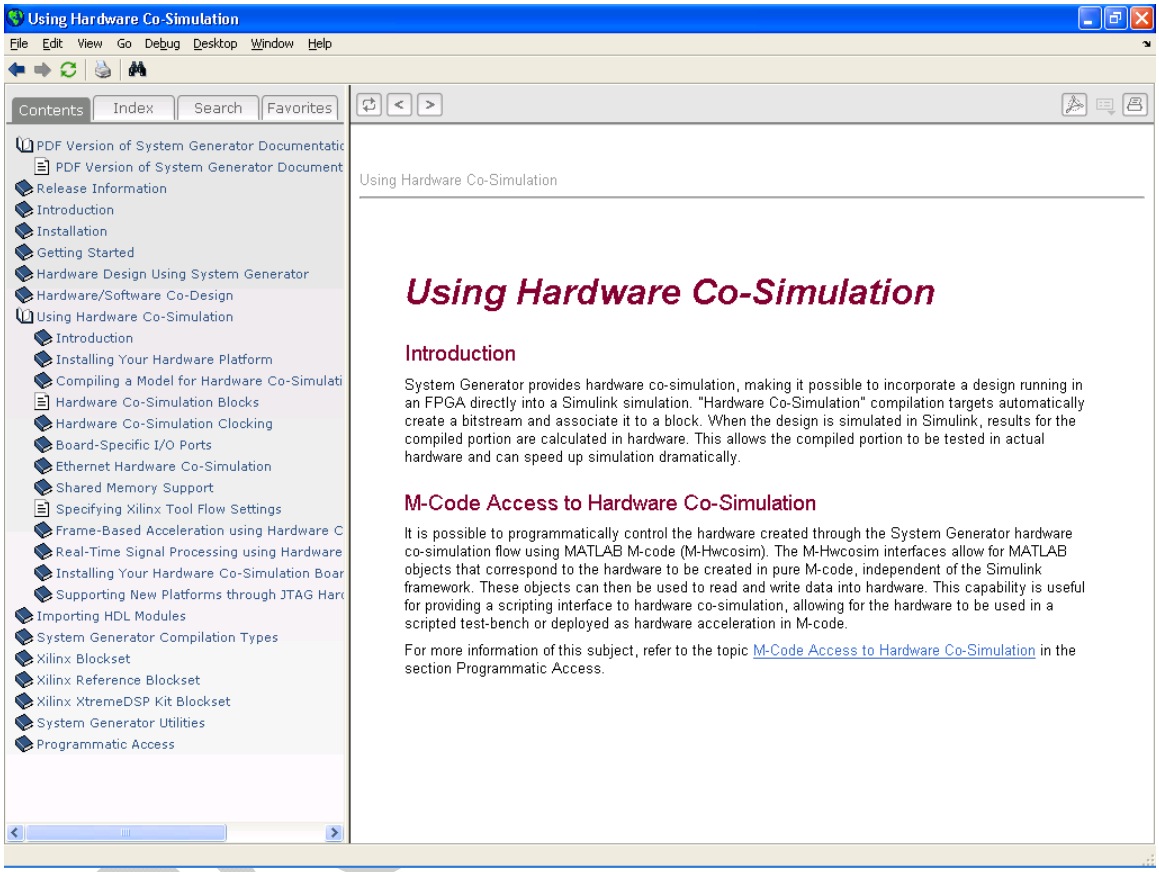

Figure 26 – xlDoc – System Generator Help System

From the Windows Start Menu,
select Programs => Xilinx ISE 11.1 Design Suite => DSP Tools => Documentation
click on the “Xilinx System Generator Manual” to access an index of all System Generator documents

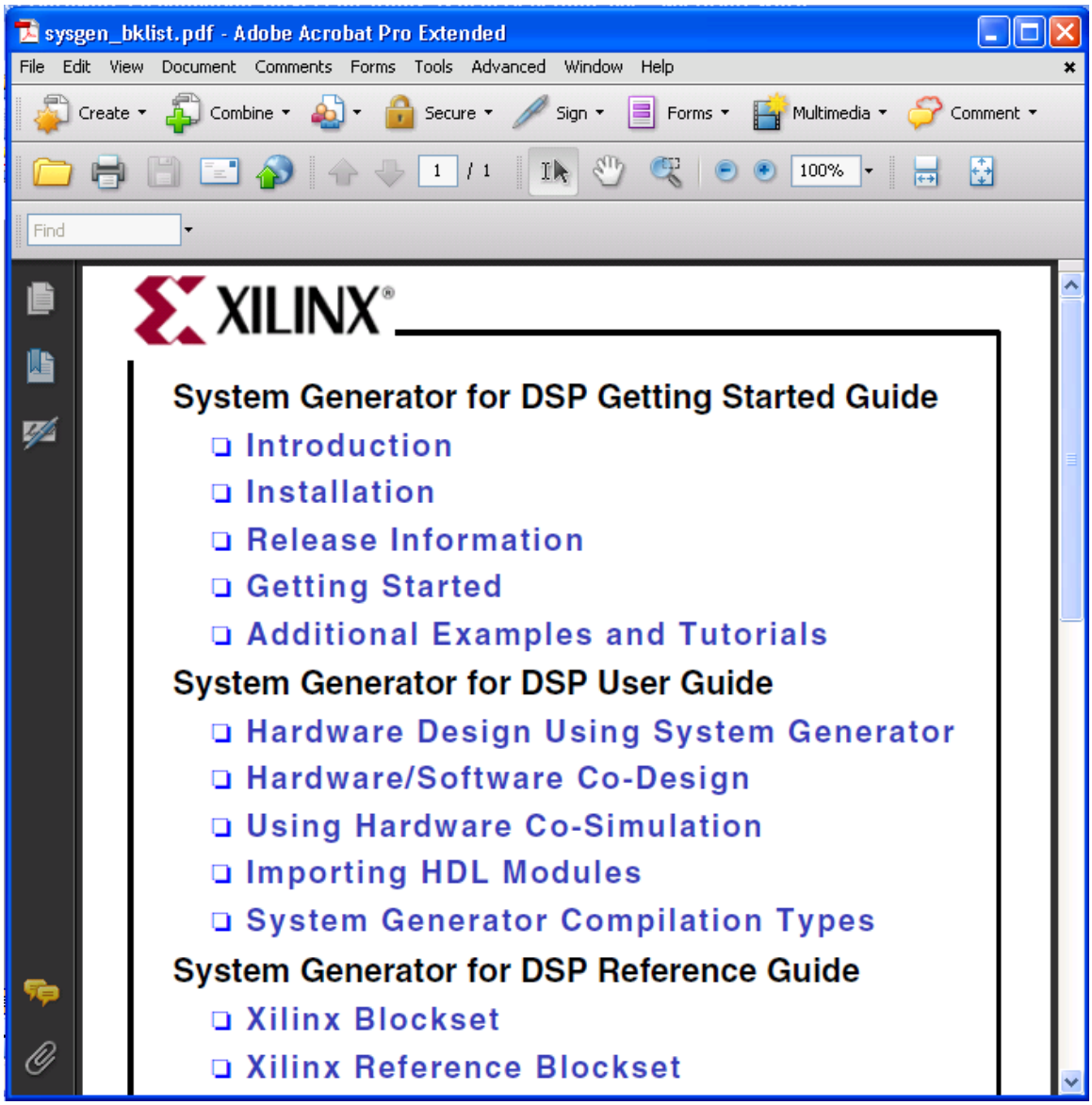

Figure 27 – PDF Documentation – System Generator Book List