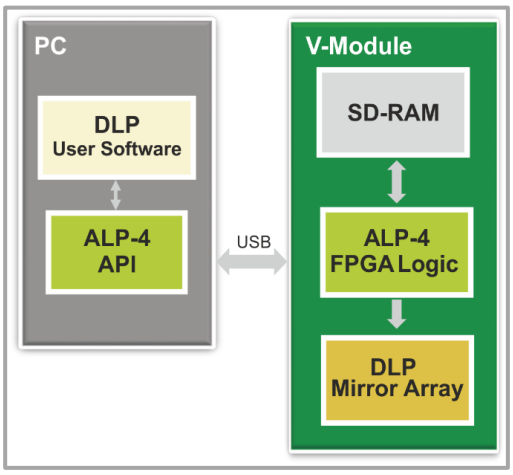
ALP-4 Controller Suite

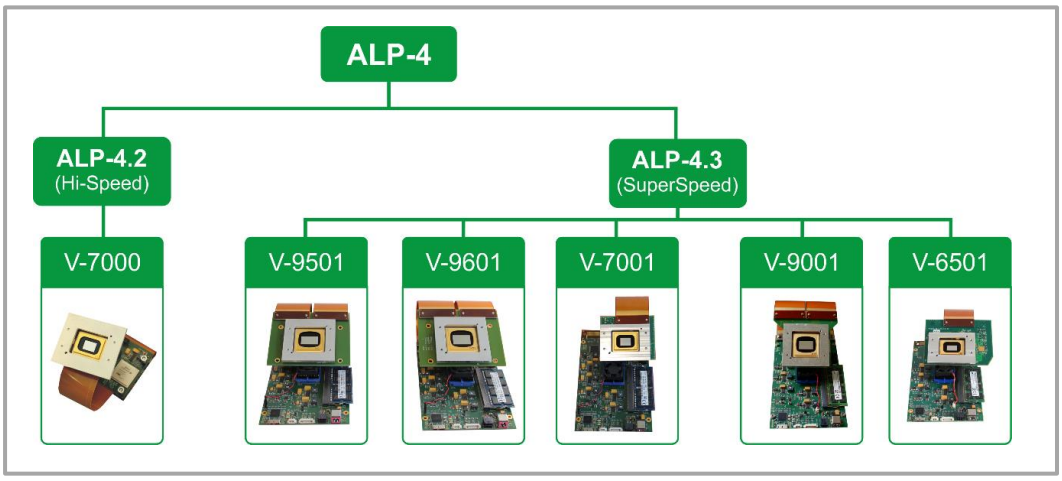
High-Performance Programming Tool for Texas Instruments DLP® Technology



The ALP-4 Controller Suite is a universal platform enabling advanced control of DLP micromirror systems. Application development is facilitated by an extensive set of library functions designed for use in industry, medicine, research and development.

ViALUX developed the ALP-4 Controller Suite starting with TI's first Discovery™ chipsets on the market. The whole line of FPGA based DLP chipsets has been supported over the years maintaining full compatibility of the application programming interface of ALP-4. Customers using ALP-4 can rapidly launch product design without the need of time consuming developments for software, firmware and high-frequency FPGA logic code.

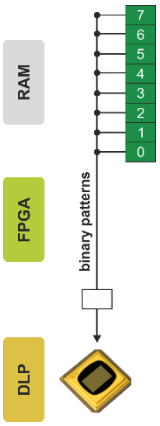
The scheme of control and data flow is shown in the block diagram. The principle of operation is completely different from standard multimedia projection. Sequences of patterns are generated in the PC and uploaded to on-board memory via compressed USB transfer. Highly sophisticated FPGA logic is applied for processing and streaming the data to the micromirror array. The ALP-4 Controller Suite is included in all V-Modules and is also available as an accessory for Discovery™ 4100 Development Kits.



The ALP-4 application programming interface (API) provides high-level DLP control and is a proven tool supporting a wide variety of use cases from proof of concept to product development and serial products. The API is realized in a portable DLL and it can be used in C++, C#, Visual Basic, .NET, LabVIEW, and MATLAB, Python running on a Microsoft Windows operating system.*

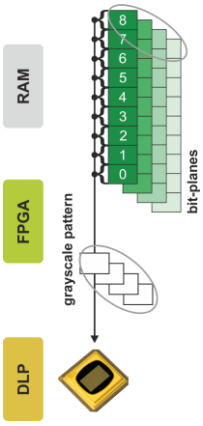
The broad usability of the ALP-4 Controller Suite is powered by the high flexibility in pattern control. Pattern sequences can be customized to meet respective requirements and four different modes of operation are available.

*DLP is a registered trademark of Texas Instruments. Microsoft, Windows, C++, C#, Visual Basic, .NET are registered trademarks of Microsoft Cooperation. MATLAB is a registered trademark of MathWorks.



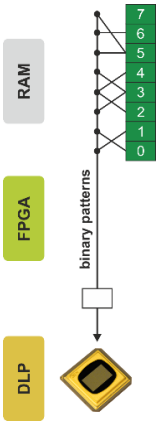
Binary Patterns

Binary pattern sequences are defined in the application program and uploaded into the on-board RAM. The timing parameters for the sequence display can be precisely controlled. ALP-4 offers high flexibility in picture time ranging from 20 µs up to several seconds. That means, mirrors can be kept still without any movement or can be switched with up to 50 kHz. A comprehensive trigger facility enables the synchronization with external devices in both master or slave mode. Multiple sequences are organized in a queue for convenient parallel upload and display and are concatenated for a gapless display.



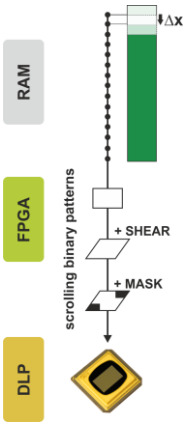
Grayscale Patterns

By design, the DMD is only capable to display a binary pattern at a given moment in time. To project a grayscale image, multiple binary frames have to be time controlled accordingly. ALP-4 generates patterns of gray values with the digital precision of FPGA timing. The maximum bit depth is 12 bit; lower resolution can be selected. Using a synchronized detector yields perfect grayscale linearity of 10ppm as it is typically needed in metrology applications of DLP. The grayscale pattern sequence contains the specified number of bit-planes and an efficient algorithm of pulse-width modulation (PWM) is implemented in ALP-4 that results in 260-300 fps (8bit) for various DLP chipsets. The whole grayscale image is subject to the trigger facility so that cameras can be easily synchronized. Flex-PWM is an advanced mode of operation where the user has free control over the bit-plane timing by external trigger.



Pattern Sequence Composition

ALP-4 supports indirect frame selection by the use of a frame look-up table (FLUT). The output display sequence is composed from the patterns stored in the RAM using the FLUT entries that point to the corresponding frames. In this way the user has a maximum of flexibility in generating display sequences and can modify them by just changing the FLUT content. Repeated display of the same pattern is made possible without storing multiple copies in the RAM so that FLUT operation saves upload time and memory capacity. One of the FLUT applications is grayscale encoding by a delta-sigma approach.



Pattern Scrolling

A moving DLP exposure head is state-of-the-art in industrial exposure applications like lithography and 3D-printing. Such approach requires that the patterns slide through the micromirror array with the same velocity. That is efficiently realized by uploading the stripe of pattern data to the RAM and stepping through it line by line. In this way a new DLP pattern is generated in each step by adding one line and dropping another. A significant data reduction is achieved for the upload from PC to on-board RAM. More sophisticated use cases demand for a sliding display of rotated patterns; that has been solved by additional shear operations applied on the flight. Permanent pixel masks are supported enabling modifications of the resulting pattern exposure level on the target.

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