DLP5500, DLPC200, DLPA200
DLP® 0.55 XGA Chipset

Data Manual

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: DLPZ004B
June 2010–Revised February 2012

Contents

1 Introduction **7**
1.1 Applications 7
1.2 Purpose 7
1.3 Related Documents 8
2 Glossary **9**
3 Device Description **9**
4 Application Programming Interface (API) **12**
5 System Input Interfaces **12**
5.1 Data Port 1 12
5.2 Data Port 2 12
5.3 Universal Serial Bus (USB) 13
5.4 Input Triggers 14
5.5 PWR_GOOD and $\overline{\text{RESET}}$ 14
5.5.1 System Power-Up Procedure 14
5.5.2 System Power-Down Procedure 15
6 System Output Interfaces **17**
6.1 Illumination Driver Control Interface 17
6.2 SYNC Outputs 17
7 System Support Interfaces **18**
7.1 Synchronous DRAM (SDRAM) 18
7.2 User Programmable Nonvolatile Flash and DLPC200 Program SRAM 18
7.3 DLPC200 Serial Configuration Flash PROM 19
7.4 DLPC200 Reference Clock 19
8 Component-to-Component Interfaces **20**
8.1 DLPC200-to-DLP5500 Digital Data and Control Interface 20
8.2 DLPC200-to-DLPA200 Micromirror Driver Control Interface 20
8.3 DLPA200 to DLP5500 Micromirror Driver Clock Pulses 21
9 Terminal Interconnection **22**
10 Printed Circuit Board (PCB) System Design **48**
10.1 Printed Circuit Layer Stack-Up
10.2 Trace Impedance, Width and Spacing, Device Placement
10.2.1 Impedance Requirements
10.2.2 Trace Width and Trace Spacing
10.2.2.1 General Design Rules for Trace Width and Spacing
10.2.2.2 Special Design Rules for Trace Width and Spacing
10.2.3 Device Placement
11 PCB Electrical Specifications
11.1 Power Planes
11.1.1 Ground Rings
11.2 Mini-Planes
11.3 Placement and Routing for Decoupling Capacitors
11.4 Signal Layers
11.5 Critical Signals and Routing Priority
11.5.1 DDR2 (SDRAM) Memory Signals – Highest Priority
11.5.2 Routing Constraints for Differential/LVDS/TMDS Signals – Next Highest Priority
11.5.3 Timing Critical Signals

Copyright © 2010–2012, Texas Instruments Incorporated

Revision History

Copyright © 2010–2012, Texas Instruments Incorporated

List of Figures

3-1 Chipset Block Diagram 10
3-2 System Block Diagram 11
5-1 Power-Up Procedure 15
5-2 Power-Down Procedure 16

Copyright © 2010–2012, Texas Instruments Incorporated

List of Tables

5-1 Active Signals – Port 1 12
5-2 Active Signals – Port 2 13
5-3 Active Signals – USB 2.0 Interface 13
5-4 Active Signals – Port 1 and Port 2 Syncs 14
6-1 Active Signals – Illumination Driver Control Interface 17
6-2 Active Signals – SYNC Outputs 17
7-1 Active Signals – Synchronous DRAM (SDRAM) 18
7-2 Active Signals – User Programmable Nonvolatile Flash and DLPC200 Program SRAM 19
7-3 Active Signals – DLPC200 Serial Configuration Flash PROM 19
8-1 Active Signals – DLPC200 to DLP5500 Digital Data and Control Interface 20
8-2 Active Signals – DLPC200 to DLPA200 Micromirror Driver Control Interface 20
8-3 Active Signals – DLPA200 to DLP5500 Micromirror Driver Clock Pulses 21
9-1 Terminal Interconnection 23
10-1 Layer Stack-Up 48
10-2 Special Impedance Requirements 48
10-3 Special Trace Widths, Spacing Requirements 49
11-1 Mini-Planes Requirement 51
11-2 Routing Priority 52
11-3 Differential Signals Routing Constraints 53
11-4 Timing Critical Signals 54

Copyright © 2010–2012, Texas Instruments Incorporated

Copyright © 2010–2012, Texas Instruments Incorporated

DLP® 0.55 XGA Chipset

Check for Samples: DLP5500, DLPC200, DLPA200

1 Introduction

- Two 24-Bit Input Ports (RGB888) With Pixel
  - Port 1 Supports HDMI Input
  - Port 2 Supports Input via an Expansion Card
  - Input Image Size 1024 × 768 (XGA), Up to 80 MHz
- Two Options for Device Control Interface
  - USB 2.0, 48 MHz
  - Serial Peripheral Interface (SPI), 5 MHz
- Structured Light Pattern Mode
  - Stores up to 960 Binary Patterns
  - Up to 5000 Hz for Binary Pattern Frame Rate
  - Up to 700-Hz 8-Bit Grayscale Frame Rate
- Input and Output Syncs and Triggers
  - Supports Three Output Syncs
  - Supports Two Inputs for External Triggers
- User-Programmable Flash and In-Field Remote Upgrade Capability
  - Serial FLASH Interface, DLPC200 Configuration
  - Parallel FLASH Interface for User-Defined Configurations
- Solid-State Illumination Interface (LED):
  - Programmable LED Current and Sync Control
  - Supports Four Independent Channels, e.g. Red, Green, Blue, and Infrared LED
- Integrated Micromirror Driver Circuitry to Simplify System Design:
  - Generates the Micromirror Clocking Pulses Required by the DLP Digital Micromirror Device (DMD)
  - Generates Specialized Voltage Levels Required for Micromirror Clocking-Pulse Generation
- Enables High-Performance Optical Imaging With DMD
  - 0.55-inch Micromirror Array Diagonal
  - 1024 × 768 Array of Aluminum, 10.8-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle
  - High On-Screen Lumens, > 2000 Lumens (Large Thermal Area: 18 mm by 12 mm for Heat Dissipation)
  - Highly Efficient in Visible Light (420 nm–700 nm):
    - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
    - Micromirror Reflectivity, 88%
    - Array Diffraction Efficiency, 86%
    - Array Fill Factor, 92%

1.1 Applications

- 3D Machine Vision
- 3D Optical Measurement
- Industrial and Medical Imaging
- Medical Instrumentation
- Digital Exposure Systems

1.2 Purpose

This document provides a description of the 0.55 XGA chipset components and function, interconnect information for the individual chipset components, and system-level design guidelines to ensure proper function of the 0.55 XGA chipset components.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DaVinci, OMAP are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Insturments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010–2012, Texas Instruments Incorporated

1.3 Related Documents

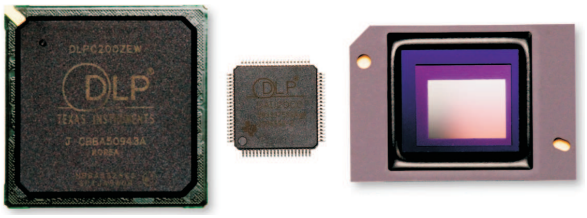
DOCUMENT	TI LITERATURE NUMBER
DLP5500 0.55 XGA Series 450 DMD Datasheet	DLPS013
DLPC200 Digital Controller for the DLP5500 Datasheet	DLPS014
DLPA200 DMD Micromirror Driver Datasheet	DLPS015
DLPC200 API Reference Manual	DLPA024
DLPC200 API Programmer's Guide	DLPA014
DMD Series 450 Thermal and Mechanical Application Note	DLPA015
DMD Series 4xx Physical Handling Application Note	DLPA019
DMD Series 4xx Glass Cleaning Application Note	DLPA025
Single-Panel DLP™ Projection System Optics Application Note	DLPA002

Copyright © 2010–2012, Texas Instruments Incorporated

2 Glossary

DDR	Double data rate
LVDS	Low-voltage differential signaling
TMDS	Transition minimized differential signaling
DLP®	Digital light processing
DMD	Digital micromirror device
DVI	Digital video interface
HVGA	Half VGA (video graphics array), 480 × 320 resolution
XGA	Extended graphics array, 1024 × 768 resolution
PROM	Programmable read-only memory
PWM	Pulse-width modulation
SDRAM	Synchronous dynamic random-access memory
SRAM	Synchronous random-access memory (verify that this is what we are using)
SPI	Serial peripheral interface
USB	Universal serial bus
I^2C	Inter-Integrated Circuit bus, multi-master serial communication bus invented by Philips
EDID	Extended Defiinition Identification Bus

3 Device Description



The DLP 0.55 XGA chipset consists of three individual components:

- DLP5500 – 0.55 XGA Series 450 DMD
- DLPA200 – DMD Micromirror Driver
- DLPC200 – DLP5500 Controller

A detailed specification for each component can be found in the data sheet for that individual component.

Figure 3-1 illustrates the connectivity between the individual components in the chipset, which includes the following internal chipset interfaces:

- DLPC200 to DLP5500 data and control interface (DMD pattern data)
- DLPC200 to DLP5500 micromirror drive control interface
- DLPA200 to DLP5500 micromirror drive interface (provides micromirror clock pulses)
- DLPC200 configuration interface (interface to configure DLPC200)

Copyright © 2010–2012, Texas Instruments Incorporated

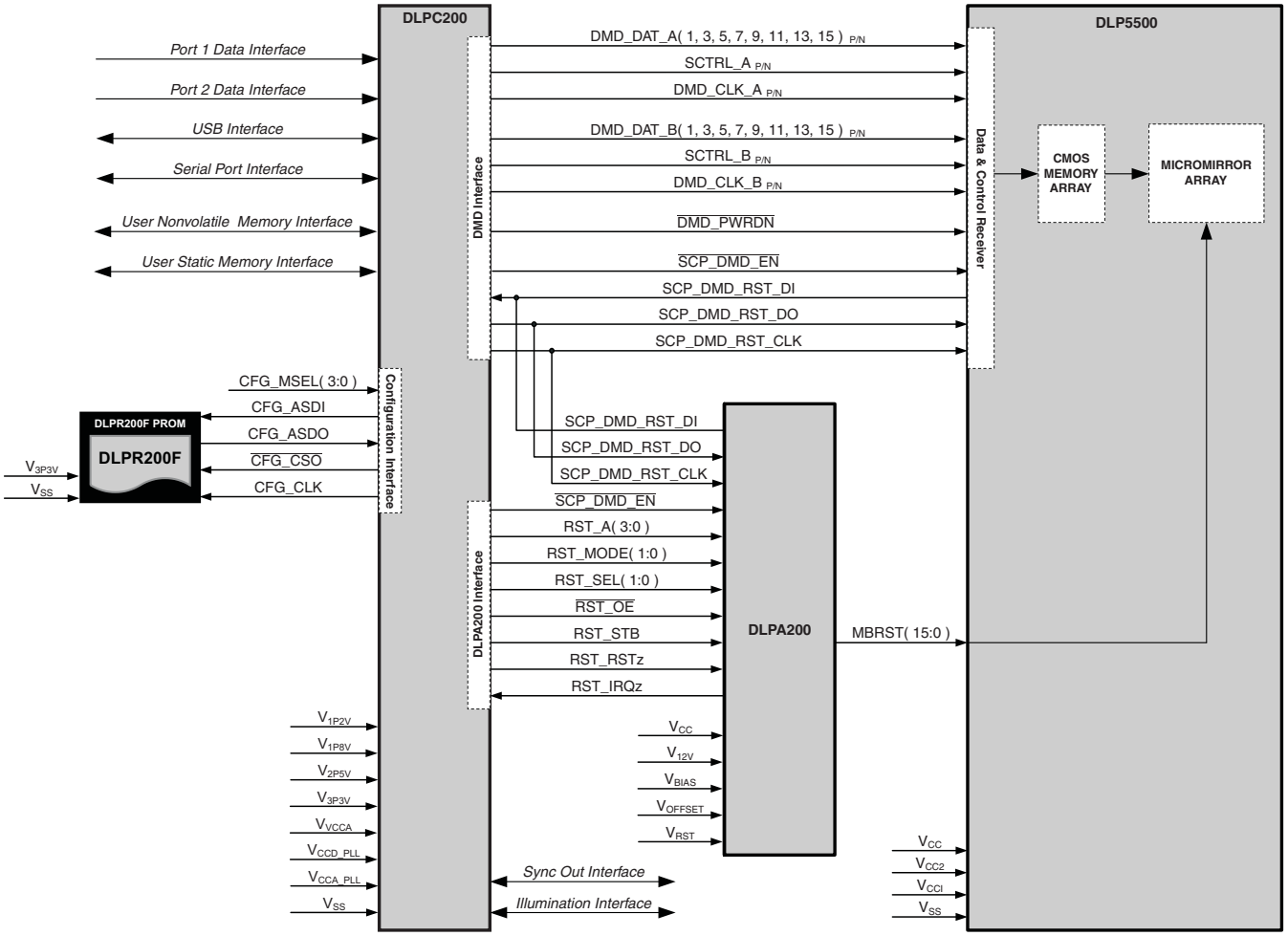


Figure 3-1. Chipset Block Diagram

Figure 3-2 illustrates the connectivity between the chipset and other key system-level components, and includes the following external chipset interfaces:

- Data port 1, consisting of:
  - 24-bit data bus
  - Vertical sync signal (VSYNC)
  - Horizontal sync signal (HSYNC)
  - Data-valid signal (IVALID)
  - Data clock signal
  - I^2C bus, intended for use with an EDID PROM
- Data port 2, consisting of signals similar to data port 1, plus an SPI bus
- USB transceiver interface (designed specifically for a Cypress CY7C68013)
- SDRAM interface (DDR2)
- Combined flash (EEPROM) and SRAM interface
- Illumination driver control interface
- Three user-programmable output signals
- System power-good signal
- System reset signal

Copyright © 2010–2012, Texas Instruments Incorporated

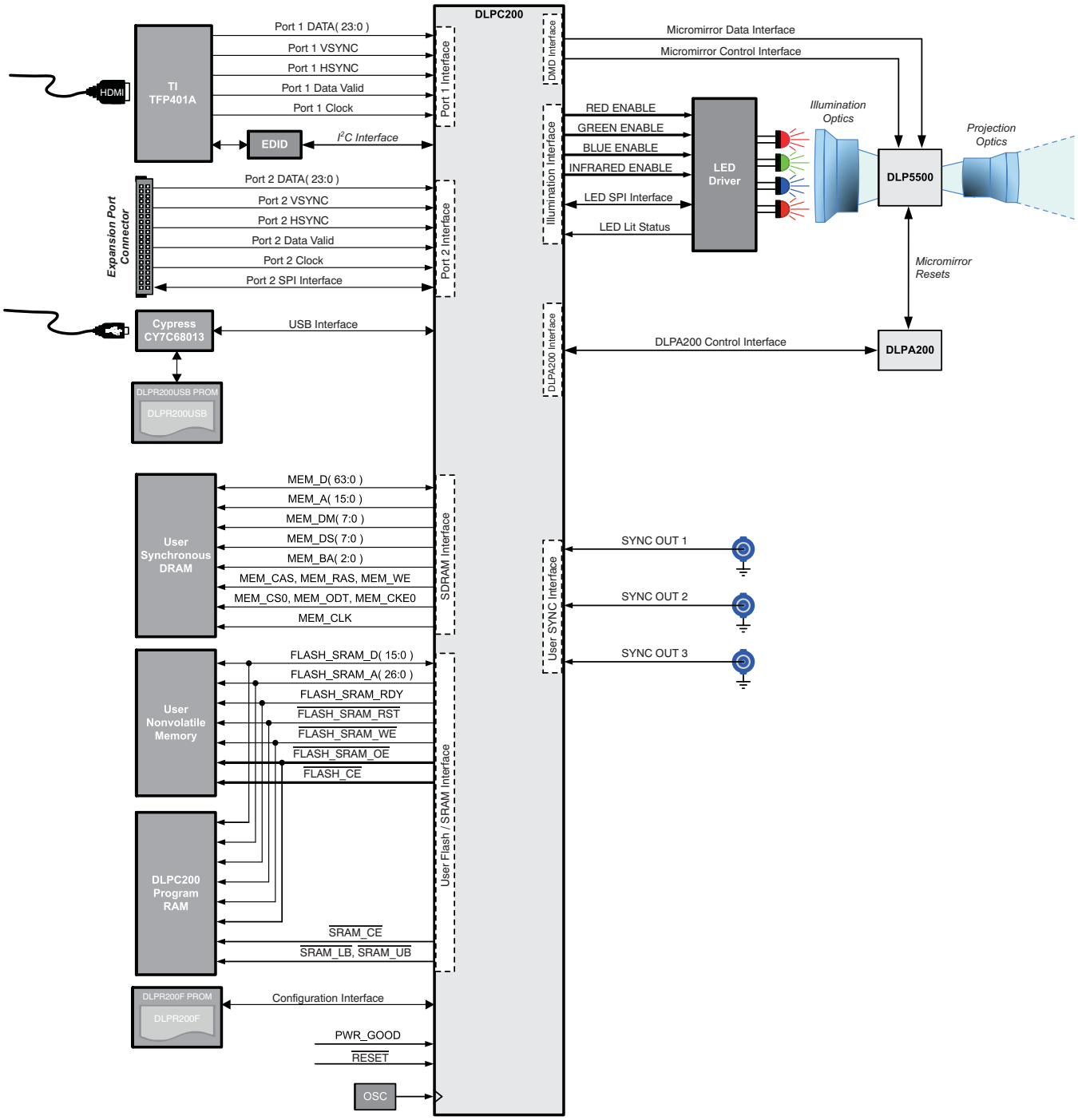


Figure 3-2. System Block Diagram

4 Application Programming Interface (API)

The 0.55 XGA chipset is supported by application programming interface (API) software (SW). The API software provides a functional interface allowing users to control in real-time or configure the 0.55 XGA chipset. For example, the API has functions to set the LED drive current or allow the user to configure patterns to be stored in flash memory. The API software is provided on www.ti.com; search keyword *DLPR200*. The API SW is provided as a complete dynamically linked library (DLL) that can be compiled into the user's custom application.

For more details about the specific functions and features, see the API reference manual and the API user's guide. These documents are listed in Section 1.3.

5 System Input Interfaces

The 0.55 XGA chipset supports multiple system inputs to allow flexible system design. These include data port 1, data port 2, USB, SPI, and input triggers. Additionally, the system input also requires that inputs POWERGOOD and $\overline{\text{RESET}}$ be set properly to ensure reliable operation.

See the DLPC200 data sheet for detailed specifications for each of the following interfaces.

5.1 Data Port 1

Data port 1 is primarily designed as a digital video input port with a 24-bit RGB and has a nominal I/O voltage of 3.3 V. As shown in Figure 3-2 (system block diagram), data port 1 can be configured to connect to an HDMI-style input, which is commonly used by a personal computer (PC). Support for an extended display identification data (EDID) PROM is also provided. The EDID PROM is checked and updated (if necessary) by the DLPC200 at power up to configure the EDID PROM to reflect the proper input resolution for the 0.55 XGA chipset. This configuration is set to a resolution of 1024 × 768 (XGA) with a refresh rate of 60 Hz. The DLPR200 API that is associated with this chipset provides functionality enabling the end user to update the manufacturing information of the EDID configuration or reprogram the data entirely.

Table 5-1 provides a description of the signals associated with data port 1.

Table 5-1. Active Signals – Port 1

SIGNAL NAME	DESCRIPTION
PORT1_D(0:23)	24-bit data inputs (8 bits for each red, green, and blue channel)
PORT1_CLK	Port 1 reference clock; all input signals on port 1 are synchronized with this clock.
PORT1_VSYNC	Vertical sync
PORT1_HSYNC	Horizontal sync
PORT1_IVALID	Input data valid
EDID_I2C_SCL, EDID_I2C_SDA	Master IIC signals used to configure the EDID PROM

Maximum and minimum input timing specifications are provided in the DLPC200 data sheet. The mapping of the red, green, and blue channel data bits is shown in Table 9-1.

5.2 Data Port 2

Data port 1 is primarily designed as a digital video input port with 24-bit RGB and has a nominal I/O voltage of 1.8 V, which is more compatible with embedded system controllers. As shown in Figure 3-2 (system block diagram), data port 2 is connected to an *expansion port connector*, allowing the system design to interface to a variety of embedded system controllers including, TI DaVinci™ DM365 and OMAP™ 35 processors.

Copyright © 2010–2012, Texas Instruments Incorporated

Support for a serial peripheral interface (SPI) is also provided, allowing for real-time system control and configuration from the *expansion port*.

Table 5-2 provides a description of the signals associated with data port 2.

Table 5-2. Active Signals – Port 2

SIGNAL NAME	DESCRIPTION
PORT2_D(0:23)	24-bit data inputs (8 bits for each red, green, and blue channel)
PORT2_CLK	Port 1 reference clock; all input signals on port 1 are synchronized with this clock.
PORT2_VSYNC	Vertical sync
PORT2_HSYNC	Horizontal sync
PORT2_IVALID	Input data valid
SLAVE_SPI_CLK	SPI clock
SLAVE_SPI_MISO	Output data port from SLAVE (DLPC200)
SLAVE_SPI_MOSI	Input data port to SLAVE (DLPC200)
$\overline{\text{SLAVE_SPI_ACK}}$	SLAVE acknowledge, allows SLAVE to hold off new transactions until slave completes processing
$\overline{\text{SLAVE_SPI_CS}}$	SLAVE (DLPC200) chip select

Maximum and minimum input timing specifications for port 2 and the SPI interface are provided in the DLPC200 data sheet. The port-2 input port is configured to accept a resolution of 1024 × 768 (XGA) with a refresh rate of 60 Hz. Mapping of the red-, green-, and blue-channel data bits is shown in Table 9-1. The SPI interface operates at a frequency of 5 MHz, nominally.

5.3 Universal Serial Bus (USB)

The 0.55 XGA chipset supports a USB 2.0 transceiver interface designed and tested specifically with a Cypress CY7C68013. The control interface allows many operations to transpire between the 0.55 XGA chipset and USB host controller (typically a PC): downloading binary pattern information to local flash or SDRAM, configuring the DLPC200, reprogramming the user configurable flash PROM, or other real-time operations such as LED driver current settings or system status. See the DLPC200 API programmer's guide (TI literature number DLPA014) and the DLPC200 API Reference Manual (TI Literature number DLPA024) for detailed information about these operations.

The Cypress USB transceiver is configured by a serial EEPROM that configures it specifically for use with the 0.55 XGA chipset. This configuration binary file can be downloaded from www.ti.com; search for key word *DLPR200*.

Table 5-3 provides a description for active signals used by the DLPC200 to support the USB 2.0 interface.

Table 5-3. Active Signals – USB 2.0 Interface

SIGNAL NAME	DESCRIPTION
USB_CLK	USB clock, nominal frequency is 48 MHz
USB_CTRL0	USB interface FIFO (first-in, first-out buffer) programmable level
USB_CTRL1	USB interface FIFO full flag
USB_CTRL2	USB interface FIFO empty flag
USB_CTRL(3:5)	Reserved for future use
USB_FD(0:15)	USB 16-bit data bus
USB_PA02	USB interface output enable for read operations
USB_PA04	USB interface address 0

Copyright © 2010–2012, Texas Instruments Incorporated

Table 5-3. Active Signals – USB 2.0 Interface (continued)

SIGNAL NAME	DESCRIPTION
USB_PA05	USB interface address 1
USB_PA06	USB interface packet end trigger
USB_RDY0	USB interface FIFO read enable
USB_RDY1	USB interface FIFO write enable
USB_RDY2	Reserved for future use
USB_RSVD14	Reserved for future use

5.4 Input Triggers

Port 1 and port 2 input triggers are provided to enable the system developer to synchronize patterns (binary or grayscale) in time according to the system timeline. For example, in some applications it may be desirable to synchronize the structured light patterns projected from the digital micromirror device (DMD) DLP5500 to the system input sensor (or camera). This can be accomplished by configuring the 0.55 XGA chipset via the API, and then applying the proper input trigger signal(s) to the DLPC200. Note: See the DLPC200 API Reference Manual (TI Literature number DLPA024) for details about all of the available input triggers and configuration.

Table 5-4. Active Signals – Port 1 and Port 2 Syncs

SIGNAL NAME	DESCRIPTION
PORT1_TRIG_IN	Input trigger associated with port 1 (3.3-V nominal I/O level)
PORT2_TRIG_IN	Input trigger associated with port 2 (1.8-V nominal I/O level)

5.5 PWR_GOOD and $\overline{\text{RESET}}$

The 0.55 XGA chipset provides two critical system features that are required for proper power up and power down of the 0.55 XGA chipset. The following sections describe the purpose and relationship of PWR_GOOD and $\overline{\text{RESET}}$. The exact timing requirements for the PWR_GOOD and $\overline{\text{RESET}}$ signals are defined in the DLPC200 data sheet.

5.5.1 System Power-Up Procedure

Figure 5-1 illustrates the power-up procedure for the power rails (1.2 V, 1.8 V, 2.5 V, 3.3 V and 12 V), $\overline{\text{RESET}}$, and PWR_GOOD that should be followed to ensure reliable system operation.

CAUTION

Not adhering to the procedures shown here and the timing specified in the DLPC200 data sheet (TI Literature number DLPS014) may cause permanent damage to the micromirrors of the DMD and/or unreliable system operation.

Copyright © 2010–2012, Texas Instruments Incorporated

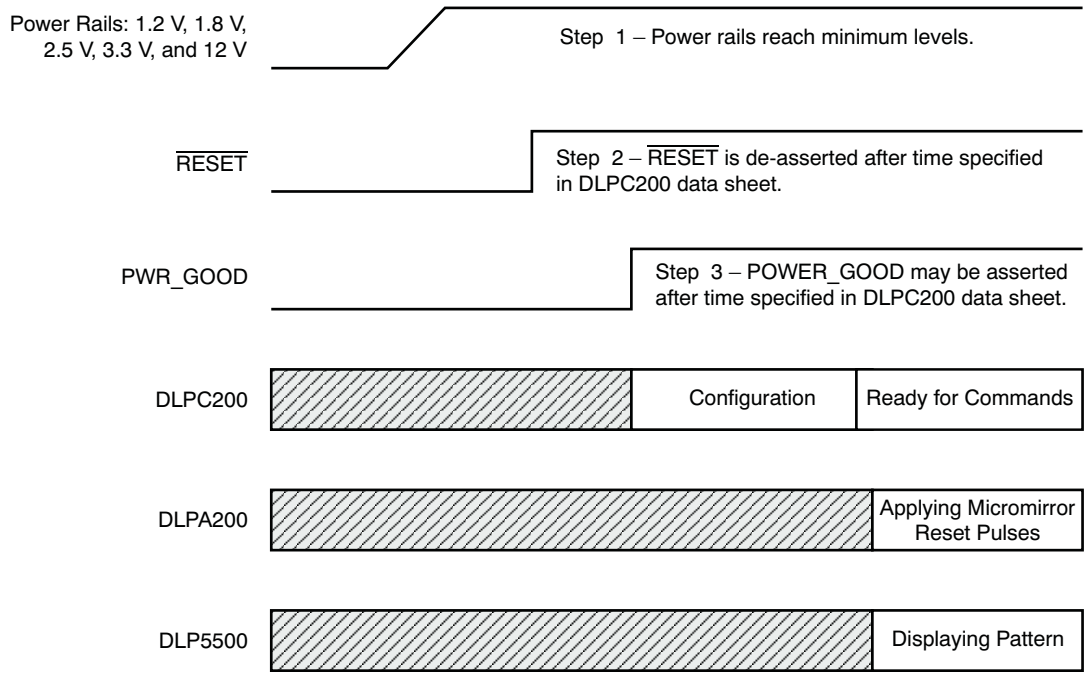


Figure 5-1. Power-Up Procedure

5.5.2 System Power-Down Procedure

Figure 5-2 illustrates the proper power-down procedures for PWR_GOOD and the associated system power rails.

CAUTION

Not adhering to the procedures shown here and the timing specified in the DLPC200 datasheet (TI Literature number DLPS014) may cause permanent damage to the micromirrors of the DMD and/or unreliable system operation.

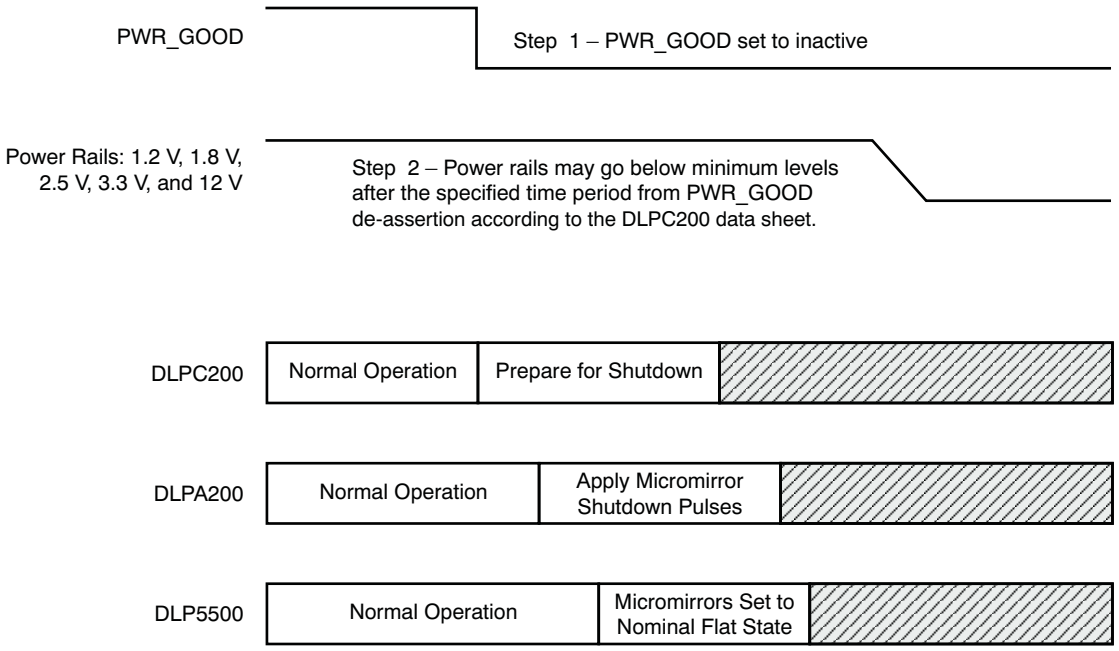


Figure 5-2. Power-Down Procedure

Copyright © 2010–2012, Texas Instruments Incorporated

6 System Output Interfaces

There are two primary output interfaces: illumination driver control interface and sync outputs.

6.1 Illumination Driver Control Interface

An illumination driver control interface is provided that supports up to a four-channel LED driver. The 0.55 chipset has been verified with the OSRAM RAPCUR F4515AIR light-emitting diode (LED) driver designed to operate red, green, and blue PT54 series Luminus LEDs, and an OSRAM OSTAR SFH4750 infrared LED (850 nm).

The illumination driver interface provides signals that support: driver enable, LED channel enable signals, serial peripheral interface for configuration, LED status, and synchronization. Table 6-1 describes the active signals for the illumination driver control interface.

Table 6-1. Active Signals – Illumination Driver Control Interface

SIGNAL NAME	DESCRIPTION
$\overline{\text{LED_EN}}$	LED driver enable
$\overline{\text{LED_LIT}}$	Indication from LED driver that LEDs are enabled (*LIT*)
LED_SYNCEN	Output signal inverted from $\overline{\text{LED_LIT}}$, Not used for LED driver interface
LED_IR_EN	Output strobe from DLPC200 to turn on the IR LED channel
LED_RED_EN	Output strobe from DLPC200 to turn on the red LED channel
LED_GRN_EN	Output strobe from DLPC200 to turn on the green LED channel
LED_BLU_EN	Output strobe from DLPC200 to turn on the blue LED channel
LED_SUBFRAME	Synchronization signal provided to the LED driver
LED_SPI_CLK	SPI clock signal
LED_SPI_DIR	LED SPI master driver direction
LED_SPI_MISO	LED SPI master input data signal
LED_SPI_MOSI	LED SPI master output data signal
$\overline{\text{LED_SPI_CS}}$	LED SPI master chip select

6.2 SYNC Outputs

Three SYNC outputs are provided to enable the system to synchronize external systems or components to the pattern being displayed on the DMD. For example, an application may be intended to trigger an in-system camera to capture an image after a certain pattern is projected from the DMD. In this case, one of the three output SYNCs can be configured to provide a pulsed signal just after the pattern is set on the DMD, thus enabling the camera to capture the projected DMD pattern. These outputs are programmable (delay, pulse duration, polarity) via the DLPC200 API, and can be updated in real-time.

Table 6-2. Active Signals – SYNC Outputs

SIGNAL NAME	DESCRIPTION
SYNC_(0:2)	Three output synchronization signals

Copyright © 2010–2012, Texas Instruments Incorporated

7 System Support Interfaces

There are multiple system support interfaces provided by the 0.55 XGA chipset, including:

- Synchronous DRAM (SDRAM)
- User programmable nonvolatile flash (NOR flash)
- DLPC200 program SRAM
- DLPC200 serial configuration flash PROM
- System reference clock

7.1 Synchronous DRAM (SDRAM)

The 0.55 XGA Chipset relies on the use of SDRAM to store DMD formatted patterns. The SDRAM interface is a 64-bit wide bus and nominally operates at a frequency of 133.33 MHz. This enables DMD patterns to be refreshed with frequency rates up to 5000 Hz binary and over 700 Hz in 8-bit gray scale.

The SDRAM interface has been designed and verified with four Micron MT47H32M16HR-3, 512 M DDR2 devices. The single 16-bit address bus is from the DLPC200 to each device, where each address pin connects to all four devices. The data bus is routed in a point-to-point fashion between the DLPC200 and each device, where each data line only makes a single connection between the DLPC200 and the SDRAM device.

Table 7-1 describes the signals for the SDRAM interface.

Table 7-1. Active Signals – Synchronous DRAM (SDRAM)

SIGNAL NAME	DESCRIPTION
MEM_A(0:15)	16-bit address bus routed in series from the
MEM_BA(0:2)	Bank select signals
MEM_CKE	Clock enable
$\overline{\text{MEM_CAS}}$	Column address strobe
$\overline{\text{MEM_RAS}}$	Row address strobe
$\overline{\text{MEM_CS0}}$	Chip select
$\overline{\text{MEM_WE}}$	Write enable
MEM_ODT	On-die termination
MEM_DM(0:7)	Input data mask
MEM_DS(0:7)	Output read strobe
MEM_D(0:63)	64-bit data bus
MEM_CLK_N(0:3)	Each memory device has a dedicated differential clock pair; MEM_CLK_N is the negative signal of the clock pair.
MEM_CLK_P(0:3)	Each memory device has a dedicated differential clock pair; MEM_CLK_P is the positive signal of the clock pair.

7.2 User Programmable Nonvolatile Flash and DLPC200 Program SRAM

The 0.55 XGA chipset supports using a common address and data bus, a user-programmable parallel flash PROM, and DLPC200 program SRAM.

The user-programmable flash PROM (NOR flash) stores the system design configuration default settings of the 0.55 XGA chipset. This interface supports 1 Gb of memory, allowing up to 960 binary patterns or 120 8-bit gray scale patterns to be stored in flash. The 0.55 XGA chipset has been designed and verified to support the following component: JS28F00AP30BF manufactured by Numonyx.

The DLPC200 program SRAM is required by the DLPC200, and is used by the DLPC200 internal processor. The 0.55 XGA chipset has been designed and verified to support the following component: CY7C1011DV33 manufactured by Cypress.

Copyright © 2010–2012, Texas Instruments Incorporated

Table 7-2 describes the signals used to support the programmable flash and SRAM interface described previously.

Table 7-2. Active Signals – User Programmable Nonvolatile Flash and DLPC200 Program SRAM

SIGNAL NAME	DESCRIPTION
FLASH_SRAM_A(1:26)	26-bit address bus (lower 16 bits are used by the SRAM)
FLASH_SRAM_D(0:15)	16-bit data bus used by both NOR flash and SRAM
$\overline{\text{FLASH_CE}}$	Chip enable for NOR flash
$\overline{\text{FLASH_SRAM_OE}}$	Output enable used by both NOR flash and SRAM
$\overline{\text{FLASH_SRAM_RST}}$	Flash reset
$\overline{\text{FLASH_SRAM_WE}}$	Flash and SRAM write enable
FLASH_SRAM_RDY	Flash ready
$\overline{\text{SRAM_CE}}$	SRAM chip enable
$\overline{\text{SRAM_LB}}$	SRAM lower-byte enable
$\overline{\text{SRAM_UB}}$	SRAM upper-byte enable

7.3 DLPC200 Serial Configuration Flash PROM

The DLPC200 requires configuration information to be available at each system power up. The actual configuration binary file can be downloaded from www.ti.com; search for keyword *DLPR200F*. The DLPC200 uses a 64-Mbit serial flash PROM to house the DLPR200F configuration code. The DLPC200 has been designed and verified with the following two serial flash components:

PART NUMBER	MANUFACTURER
M25P64	Numonyx
W25Q64BV	Winbond

Table 7-3 describes the signals used to support this interface.

Table 7-3. Active Signals – DLPC200 Serial Configuration Flash PROM

SIGNAL NAME	DESCRIPTION
CFG_ASDO	Serial configuration flash data output (from DLPC200 to flash)
CFG_ASDI	Serial configuration flash data input (from flash to DLPC200)
CFG_CLK	Serial configuration flash clock
$\overline{\text{CFG_CSO}}$	Serial configuration flash chip select
CFG_DONE	Configuration complete. This signal goes high when the DLPC200 configuration is complete.

SeeTable 9-1 for detailed connection between the DLPC200 and serial flash PROM.

7.4 DLPC200 Reference Clock

The DLPC200 requires a 50-MHz 3.3-V TTL input from an oscillator. This is the 0.55 XGA chipset reference clock from which the majority of interfaces derive their clock including: SDRAM and DMD interfaces.

See the DLPC200 datas heet (TI literature number DLPS014) for reference clock specifications.

Copyright © 2010–2012, Texas Instruments Incorporated

8 Component-to-Component Interfaces

8.1 DLPC200-to-DLP5500 Digital Data and Control Interface

The DLPC200 provides the digital control and DMD pattern data to the DMD over a custom high-speed LVDS interface. The DLPC200 also provides a serial bus used to initialize the DLPA200 and DLP5500.

Table 8-1 describes the signals used for this interface.

Table 8-1. Active Signals – DLPC200 to DLP5500 Digital Data and Control Interface

SIGNAL NAME	DESCRIPTION
DMD (DLP5500) LVDS Bus	
DMD_DAT_AN(1, 3, 5, 7, 11, 13, 15), DMD_DAT_AP(1, 3, 5, 7, 11, 13, 15)	8 differential pairs with the DMD pattern data for the A bus
DMD_DAT_BN(1, 3, 5, 7, 11, 13, 15), DMD_DAT_BP(1, 3, 5, 7, 11, 13, 15)	8 differential pairs with the DMD pattern data for the B bus
DMD_CLK_AN, DMD_CLK_AP	Differential clock for A bus
DMD_CLK_BN, DMD_CLK_BP	Differential clock for B bus
DMD_SCTRL_AN, DMD_SCTRL_AP	Differential serial control for A bus, controls associated with DMD pattern data
DMD_SCTRL_BN, DMD_SCTRL_BP	Differential serial control for B bus, controls associated with DMD pattern data
$\overline{\text{DMD_PWRDN}}$	DMD power-down signal
Serial Control Port	
SCP_DMD_RST_CLK	Serial control port clock
SCP_DMD_RST_DO	Serial control port data output (data out from DLPC200 to either DLP5500 or DLPA200)
SCP_DMD_RST_DI	Serial control port data input (data into DLPC200 from either DLP5500 or DLPA200)
$\overline{\text{SCP_DMD_EN}}$	Serial control port DMD (DLP5500) chip enable
$\overline{\text{SCP_RST_EN}}$	Serial control port DLPA200 chip enable

8.2 DLPC200-to-DLPA200 Micromirror Driver Control Interface

The DLPC200 controls the DLPA200 (micromirror clock-pulse driver). The DLPC200 drives the control signals synchronously with the DMD pattern data to generate the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

Table 8-2 describes the signals used for this interface.

Table 8-2. Active Signals – DLPC200 to DLPA200 Micromirror Driver Control Interface

SIGNAL NAME	DESCRIPTION
RST_STROBE	Strobe, latch mode, address, and select signal
RST_MODE(0:1)	Mode, clock pulse mode
RST_A(0:3)	Address for MBRST
RST_SEL(0:1)	Select
$\overline{\text{RST_IRQ}}$	DLPA200 interrupt signal, indicates system interruption
$\overline{\text{RST_OE}}$	DLPA200 output enable
$\overline{\text{RST_RST}}$	DLPA200 reset

Copyright © 2010–2012, Texas Instruments Incorporated

8.3 DLPA200 to DLP5500 Micromirror Driver Clock Pulses

The DLPA200 provides customized clock pulses that cause the DMD micromirrors to change from the +12-degree state to the –12-degree state or vice versa. These clock pulses are a customized signal with a voltage swing between –26 V and 26 V. The timing of these pulses is controlled and coordinated by the DLPC200. The DLPA200 also generates a specialized voltage used by the DLP5500 (DMD) – (VCC2, also referred to as Voffset). VCC2 is nominally set to 8.5 V.

Table 8-3 describes the signals used for this interface.

Table 8-3. Active Signals – DLPA200 to DLP5500 Micromirror Driver Clock Pulses

SIGNAL NAME	DESCRIPTION
MBRST(0:15)	Micromirror clock (reset) pulses that cause micromirror to change mechanical state.
VCC2, VOFFSET, or VOFFSET_RAIL	Specialized voltage used by the DMD, nominally 8.5 V

Copyright © 2010–2012, Texas Instruments Incorporated

9 Terminal Interconnection

Table 9-1 describes the interconnection of terminals between the 0.55 XGA chipset components (DLP5500, DLPC200, DLPA200), the signal termination (if required), and the interconnection to system components (e.g., USB, SDRAM, etc.). The 0.55 XGA chipset components are designed and verified only with the interconnections specified in Table 9-1, and should be connected as specified below for proper system operation.

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
Data Port 1										
PORT1_HPD	E15	--	--	--	--			100-kΩ pullup to 3.3V	--	HDMI hot-plug detect
PORT1_CLK	J2	--	--	--	TI TFP401A	Pin 44		10-Ω series source termination	--	
PORT1_D0	D2	--	--	--	TI TFP401A	Pin 10		--	--	Blue bit 1
PORT1_D1	D3	--	--	--	TI TFP401A	Pin 11		--	--	Blue bit 2
PORT1_D2	F5	--	--	--	TI TFP401A	Pin 12		--	--	Blue bit 3
PORT1_D3	D1	--	--	--	TI TFP401A	Pin 13		--	--	Blue bit 4
PORT1_D4	F3	--	--	--	TI TFP401A	Pin 14		--	--	Blue bit 5
PORT1_D5	G4	--	--	--	TI TFP401A	Pin 15		--	--	Blue bit 6
PORT1_D6	F1	--	--	--	TI TFP401A	Pin 16		--	--	Blue bit 7
PORT1_D7	G3	--	--	--	TI TFP401A	Pin 17		--	--	Green bit 0
PORT1_D8	H5	--	--	--	TI TFP401A	Pin 20		--	--	Green bit 1
PORT1_D9	H4	--	--	--	TI TFP401A	Pin 21		--	--	Green bit 2
PORT1_D10	G2	--	--	--	TI TFP401A	Pin 22		--	--	Green bit 3
PORT1_D11	J4	--	--	--	TI TFP401A	Pin 23		--	--	Green bit 4
PORT1_D12	H3	--	--	--	TI TFP401A	Pin 24		--	--	Green bit 5
PORT1_D13	J3	--	--	--	TI TFP401A	Pin 25		--	--	Green bit 6
PORT1_D14	K3	--	--	--	TI TFP401A	Pin 26		--	--	Green bit 7
PORT1_D15	L1	--	--	--	TI TFP401A	Pin 27		--	--	Red bit 0
PORT1_D16	L3	--	--	--	TI TFP401A	Pin 30		--	--	Red bit 1
PORT1_D17	L4	--	--	--	TI TFP401A	Pin 31		--	--	Red bit 2
PORT1_D18	M4	--	--	--	TI TFP401A	Pin 32		--	--	Red bit 3
PORT1_D19	K1	--	--	--	TI TFP401A	Pin 33		--	--	Red bit 4
PORT1_D20	M1	--	--	--	TI TFP401A	Pin 34		--	--	Red bit 5
PORT1_D21	K2	--	--	--	TI TFP401A	Pin 35		--	--	Red bit 6
PORT1_D22	M2	--	--	--	TI TFP401A	Pin 36		--	--	Red bit 7
PORT1_D23	M3	--	--	--	TI TFP401A	Pin 37		--	--	
PORT1_HSYNC	P1	--	--	--	TI TFP401A	Pin 48		--	--	
PORT1_IVALID	P2	--	--	--	TI TFP401A	Pin 46		--	--	
PORT1_VSYNC	N3	--	--	--	TI TFP401A	Pin 47		--	--	
PORT1_SYNCDET	J22	--	--	--	TI TFP401A	Pin 8		--	--	
PORT1_TRIG_IN	F2	--	--	--	User discretion			--	--	
PORT1_SYNC_OUT	H6	--	--	--				--	--	Reserved for future use
{ HDMI_ST }	--	--	--	--	TI TFP401A	Pin 3		1-kΩ pulldown to DGND	--	
{ HDMI_STAGz }	--	--	--	--	TI TFP401A	Pin 7		1-kΩ pullup to VCC_3P3V	--	
{ HDMI_DFO }	--	--	--	--	TI TFP401A	Pin 1		1-kΩ pulldown to DGND	--	
{ HDMI_OCK_INV }	--	--	--	--	TI TFP401A	Pin 100		1-kΩ pulldown to DGND	--	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
{ HDMI_PDz }	--	--	--	--	TI TFP401A	Pin 2		1-kΩ pullup to VCC_3P3V	--	
{ HDMI_PDOz }	--	--	--	--	TI TFP401A	Pin 9		1-kΩ pullup to VCC_3P3V	--	
{ HDMI_PIXS }	--	--	--	--	TI TFP401A	Pin 4		1-kΩ pulldown to DGND	--	
{ HDMI_NC }	--	--	--	--	TI TFP401A	Pin 99		Pullup to VCC_3P3V	--	
{ HDMI_THPAD }	--	--	--	--	TI TFP401A	Pin 101		Pulldown to DGND	--	
{ HDMI_PVDD }	--	--	--	--	TI TFP401A	Pin 97		See component data sheet for connection recommendations	--	
{ HDMI_DVDD }	--	--	--	--	TI TFP401A	Pins 67, 38, 6		See component data sheet for connection recommendations	--	
{ HDMI_AVDD }	--	--	--	--	TI TFP401A	Pins 95, 88, 84, 82		See component data sheet for connection recommendations	--	
{ HDMI_OVDD }	--	--	--	--	TI TFP401A	Pins 78, 57, 43, 29, 18		See component data sheet for connection recommendations	--	
EDID PROM										
EDID_I2C_SCL	F8	--	--	--	Microchip 24LC02B-I/MS	Pin 6	HDMI Connector SCL connection	47-kΩ pullup to VCC_3P3V	--	
EDID_I2C_SDA	D6	--	--	--	Microchip 24LC02B-I/MS	Pin 5	HDMI Connector SDA connection	47-kΩ pullup to VCC_3P3V	--	
{ EDID_WP }	--	--	--	--	Microchip 24LC02B-I/MS	Pin 7		Pulldown to DGND	--	
{ EDID_VCC }	--	--	--	--	Microchip 24LC02B-I/MS	Pin 8		VCC_3P3V	--	
{ EDID_A2 }	--	--	--	--	Microchip 24LC02B-I/MS	Pin 3		Pulldown to DGND	--	
{ EDID_A1 }	--	--	--	--	Microchip 24LC02B-I/MS	Pin 2		No connect	--	
{ EDID_A0 }	--	--	--	--	Microchip 24LC02B-I/MS	Pin 1		No connect	--	
Data Port 2										
PORT2_CLK	Y2	--	--	--	Connections are processor dependant			--	--	
PORT2_D0	Y1				Connections are processor dependent			--	--	Blue bit 0
PORT2_D1	AE1				Connections are processor dependent			--	--	Blue bit 1
PORT2_D2	U2				Connections are processor dependent			--	--	Blue bit 2
PORT2_D3	AD12				Connections are processor dependent			--	--	Blue bit 3
PORT2_D4	AB1				Connections are processor dependent			--	--	Blue bit 4
PORT2_D5	V3				Connections are processor dependent			--	--	Blue bit 5
PORT2_D6	U5				Connections are processor dependent			--	--	Blue bit 6

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
PORT2_D7	T3				Connections are processor dependent			--	--	Blue bit 7
PORT2_D8	AD1				Connections are processor dependent			--	--	Green bit 0
PORT2_D9	AA3				Connections are processor dependent			--	--	Green bit 1
PORT2_D10	R6				Connections are processor dependent			--	--	Green bit 2
PORT2_D11	W3				Connections are processor dependent			--	--	Green bit 3
PORT2_D12	AB5				Connections are processor dependent			--	--	Green bit 4
PORT2_D13	AD3				Connections are processor dependent			--	--	Green bit 5
PORT2_D14	AD5				Connections are processor dependent			--	--	Green bit 6
PORT2_D15	AD4				Connections are processor dependent			--	--	Green bit 7
PORT2_D16	AE5				Connections are processor dependent			--	--	Red bit 0
PORT2_D17	AC11				Connections are processor dependent			--	--	Red bit 1
PORT2_D18	AB8				Connections are processor dependent			--	--	Red bit 2
PORT2_D19	AC7				Connections are processor dependent			--	--	Red bit 3
PORT2_D20	AG4				Connections are processor dependent			--	--	Red bit 4
PORT2_D21	AE4				Connections are processor dependent			--	--	Red bit 5
PORT2_D22	AF5				Connections are processor dependent			--	--	Red bit 6
PORT2_D23	AF3				Connections are processor dependent			--	--	Red bit 7
PORT2_HSYNC	AB6				Connections are processor dependent			--	--	
PORT2_IVALID	W1				Connections are processor dependent			--	--	
PORT2_VSYNC	AF2				Connections are processor dependent			--	--	
PORT2_TRIG_IN	AB7				Connections are processor dependent			--	--	
PORT2_SYNC_OUT	Y3				Connections are processor dependent			--	--	Reserved for future use
Expansion Port (2) SPI Interface										

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
SLAVE_SPI_CLK	B14				Connections are processor dependent					
SLAVE_SPI_MISO	D14				Connections are processor dependent					
SLAVE_SPI_MOSI	E14				Connections are processor dependent					
SLAVE_SPI_ACK\	D20				Connections are processor dependent					
SLAVE_SPI_SOP\	F21				Connections are processor dependent					Reserved for future use
SLAVE_SPI_CS\	C14				Connections are processor dependent					
Expansion Port (2) IIC Interface										
I2C_SCL	C25				Connections are processor dependent			2.2-kΩ pullup to 3.3V		Reserved for future use
I2C_SDA	D18				Connections are processor dependent			2.2-kΩ pullup to 3.3V		Reserved for future use
DLPC200 Reset and Power Good signal										
RESET\	A14							10-kΩ pullup to VCC_3P3V		
PWR_GOOD	A23							10-kΩ pullup to VCC_3P3V		
DLPC200 Reference Clock										
REF_CLK	J27	--	--	--	50-MHz clock source			10 ohm series source termination	--	
DLPC200 Configuration PROM interface										
CFG_ASDO	F4	--	--	15	Samtec TSM-105-01-L-DV	Pin 9		--	--	
CFG_ASDI	N7	--	--	8	Samtec TSM-105-01-L-DV	Pin 7		24.9-Ω series termination at DLPR200F Config PROM	--	
CFG_CLK	P3	--	--	16	Samtec TSM-105-01-L-DV	Pin 1		10-Ω series termination at DLPC200	--	
CFG_CSO\	E2	--	--	7	Samtec TSM-105-01-L-DV	Pin 8		--	--	
{ PROM HOLD\ }	--	--	--	1	--			VCC_3P3V	--	
{ PROM WP\ }	--	--	--	9	--			VCC_3P3V	--	
CFG_MSEL0	N22	--	--	--	--			DGND	--	
CFG_MSEL1	P23	--	--	--	--			VCC_2P5V	--	
CFG_MSEL2	M22	--	--	--	--			DGND	--	
CFG_MSEL3	P22	--	--	--	--			DGND	--	
--	--	--	--	--	Samtec TSM-105-01-L-DV	Pin 2		DGND	--	
--	--	--	--	--	Samtec TSM-105-01-L-DV	Pin 4		VCC_3P3V, with 0.1 µF bypass to DGND	--	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
--	--	--	--	--	Samtec TSM-105-01-L-DV	Pin 10		DGND	--	
CFG_CE\	R8	--	--	--	Samtec TSM-105-01-L-DV	Pin 6		1-kΩ pulldown to DGND	--	
CFG_CEO\	P28	--	--	--	No Connect			--	--	Connection not required
CFG_DONE	P24	--	--	--	Samtec TSM-105-01-L-DV	Pin 3		10-kΩ pullup to VCC_3P3V	--	
CFG_EN\	P4	--	--	--	Samtec TSM-105-01-L-DV	Pin 5	Momentary Switch to DGND	10-kΩ pullup to VCC_3P3V, with 0.1 µF bypass to DGND.	--	
CFG_STATUS\	M6	--	--	--	--			10-kΩ pullup to VCC_3P3V	--	
USB Transceiver										
USB_CLK	B15	--	--	--	Cypress CY7C68013	Pin 32		10-Ω series termination, at CY7C68013 and, 10-kΩ pulldown at DLPC200	--	
USB_CTRL0	B17	--	--	--	Cypress CY7C68013	Pin 69		--	--	
USB_CTRL1	A26	--	--	--	Cypress CY7C68013	Pin 70		--	--	
USB_CTRL2	D22	--	--	--	Cypress CY7C68013	Pin 71		--	--	
USB_CTRL3	C19	--	--	--	Cypress CY7C68013	Pin 66		--	--	
USB_CTRL4	D16	--	--	--	Cypress CY7C68013	Pin 67		--	--	
USB_CTRL5	G17	--	--	--	Cypress CY7C68013	Pin 98		--	--	
USB_FD0	G16	--	--	--	Cypress CY7C68013	Pin 44		--	--	
USB_FD1	C26	--	--	--	Cypress CY7C68013	Pin 45		--	--	
USB_FD2	F17	--	--	--	Cypress CY7C68013	Pin 46		--	--	
USB_FD3	C22	--	--	--	Cypress CY7C68013	Pin 47		--	--	
USB_FD4	E18	--	--	--	Cypress CY7C68013	Pin 54		--	--	
USB_FD5	B18	--	--	--	Cypress CY7C68013	Pin 55		--	--	
USB_FD6	F18	--	--	--	Cypress CY7C68013	Pin 56		--	--	
USB_FD7	E19	--	--	--	Cypress CY7C68013	Pin 57		--	--	
USB_FD8	B23	--	--	--	Cypress CY7C68013	Pin 102		--	--	
USB_FD9	D25	--	--	--	Cypress CY7C68013	Pin 103		--	--	
USB_FD10	C21	--	--	--	Cypress CY7C68013	Pin 104		--	--	
USB_FD11	D24	--	--	--	Cypress CY7C68013	Pin 105		--	--	
USB_FD12	B19	--	--	--	Cypress CY7C68013	Pin 121		--	--	
USB_FD13	E25	--	--	--	Cypress CY7C68013	Pin 122		--	--	
USB_FD14	G18	--	--	--	Cypress CY7C68013	Pin 123		--	--	
USB_FD15	C15	--	--	--	Cypress CY7C68013	Pin 124		--	--	
USB_PA02	D23	--	--	--	Cypress CY7C68013	Pin 84		--	--	
{ USB_PA03 }	--	--	--	--	Cypress CY7C68013	Pin 85		USB VBUS (divided down to 3.9 V), 0.1-µF capacitor to DGND, ESD protection	--	
USB_PA04	G15	--	--	--	Cypress CY7C68013	Pin 89		--	--	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
USB_PA05	A22	--	--	--	Cypress CY7C68013	Pin 90		--	--	
USB_PA06	A25	--	--	--	Cypress CY7C68013	Pin 91		--	--	
USB_RDY0	C16	--	--	--	Cypress CY7C68013	Pin 4		--	--	
USB_RDY1	C17	--	--	--	Cypress CY7C68013	Pin 5		--	--	
USB_RDY2	B26	--	--	--	Cypress CY7C68013	Pin 6		--	--	
{ USB_RDY3 }	--	--	--	--	Cypress CY7C68013	Pin 7		10-kΩ pulldown to DGND	--	
{ USB_RDY4 }	--	--	--	--	Cypress CY7C68013	Pin 8		10-kΩ pulldown to DGND	--	
{ USB_RDY5 }	--	--	--	--	Cypress CY7C68013	Pin 9		10-kΩ pulldown to DGND	--	
USB_RSVD_14	A15	--	--	--	Cypress CY7C68013	Pin 1		10-Ω series termination at CY7C68013 and 10-kΩ pulldown to DGND at DLPC200	--	
{ USB_WAKEUP }	--	--	--	--	Cypress CY7C68013	Pin 101		10-kΩ pullup to VCC_3P3V	--	
{ USB_INT4\ }	--	--	--	--	Cypress CY7C68013	Pin 28		10-kΩ pulldown to DGND	--	
{ USB_INT5\ }	--	--	--	--	Cypress CY7C68013	Pin 106		10-kΩ pullup to VCC_3P3V	--	
{ USB_T0 }	--	--	--	--	Cypress CY7C68013	Pin 29		10-kΩ pulldown to DGND	--	
{ USB_T1 }	--	--	--	--	Cypress CY7C68013	Pin 30		10-kΩ pulldown to DGND	--	
{ USB_T2 }	--	--	--	--	Cypress CY7C68013	Pin 31		10-kΩ pulldown to DGND	--	
{ USB_BKPT }	--	--	--	--	Cypress CY7C68013	Pin 34		10-kΩ pulldown to DGND	--	
{ USB_EA }	--	--	--	--	Cypress CY7C68013	Pin 35		10-kΩ pulldown to DGND	--	
{ USB_DMINUS }	--	--	--	--	Cypress CY7C68013	Pin 19		USB DN, ESD protection	USB Diff	
{ USB_DPLUS }	--	--	--	--	Cypress CY7C68013	Pin 18		USB DP, ESD protection	USB Diff	
{ USB_XTALOUT }	--	--	--	--	Cypress CY7C68013	Pin 11		24-MHz crystal, 12-pF capacitor to DGND, 1-MΩ resistor to USB_XTALIN	--	
{ USB_XTALIN }	--	--	--	--	Cypress CY7C68013	Pin 12		24-MHz crystal, 12-pF capacitor to DGND, 1-MΩ resistor to USB_XTALOUT	--	
{ USB_VCC }	--	--	--	--	Cypress CY7C68013	Pins 2, 26, 43, 48, 64, 68, 81, 100, 107		See component data sheet for connection recommendations	--	
{ USB_AVCC }	--	--	--	--	Cypress CY7C68013	Pins 10, 17		See component data sheet for connection recommendations	--	
{ USB_RSVD }	--	--	--	--	Cypress CY7C68013	Pin 33		DGND	--	
{ USB_AGND }	--	--	--	--	Cypress CY7C68013	Pins 13, 20		DGND	--	
{ USB_GND }	--	--	--	--	Cypress CY7C68013	Pins 3, 27, 49, 58, 65, 80, 93, 116, 125		DGND	--	
{ USB_SCL }	--	--	--	--	Cypress CY7C68013	Pin 36		USB EEPROM SCL (see component data sheets for connection recommendations)	--	
{ USB_SDA }	--	--	--	--	Cypress CY7C68013	Pin 37		USB EEPROM SDA (see component data sheets for connection recommendations)	--	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
{ USB_NC }	--	--	--	--	Cypress CY7C68013	Pins 14, 15, 16		No connect	--	
LED Illumination Module Interface										
LED_EN\	L28									
LED_LIT\	J28									
LED_SYNCEN	C24									Reserved for future use
LED_IR_EN	E28							1-kΩ pulldown to DGND		
LED_RED_EN	F28							1-kΩ pulldown to DGND		
LED_GRN_EN	E27							1-kΩ pulldown to DGND		
LED_BLU_EN	F27							1-kΩ pulldown to DGND		
LED_SUBFRAME	E26							1-kΩ pulldown to DGND		Light eng rsvd
LED_SPI_CLK	N26									
LED_SPI_DIR	P25									
LED_SPI_MISO	L27									
LED_SPI_MOSI	L26									
LED_SPI_CS\	M26									
PWM0	C27				TSW-106-23-T-S	Pin 2				Reserved for future use
PWM1	D28				TSW-106-23-T-S	Pin 3				Reserved for future use
PWM2	D27				TSW-106-23-T-S	Pin 4				Reserved for future use
PWM3	D26				TSW-106-23-T-S	Pin 5				Reserved for future use
LED_SENS	K27							1-kΩ pulldown to DGND		
LED_SYNC	M21									Reserved for future use
Illumination SYNC Outputs										
SYNC_0	F26									Lamp header
SYNC_1	F25									Exp
SYNC_2	F24									Exp
Serial configuration for DLP500 & DLPA200										
SCP_DMD_RST_CLK	H25	A8	56	--	--				DAD data sheet	
SCP_DMD_RST_DO	G25	A5	57	--	--				DAD data sheet	Note: "DMD_SCP_RST_DI" is an output from DLPA200 and DLP5500, and an input to DLPC200
SCP_DMD_RST_DI	H26	A9	42	--	--			1 kΩ to VCC_3P3V	DAD data sheet	Note: DMD_SCP_RST_DO is an input to DLPA200 and DLP5500, and an output from DLPC200
SCP_DMD_EN\	L25	B7	--	--	--			1 kΩ to VCC_3P3V	DAD data sheet	
SCP_RST_EN\	H23	--	58	--	--			2.2 kΩ to VCC_3P3V	DAD data sheet	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DLPA200 Control interface & configuration										
RST_STROBE	G28	--	15	--	--				DAD data sheet	
RST_MODE0	L24	--	3	--	--				DAD data sheet	
RST_MODE1	L23	--	2	--	--				DAD data sheet	
RST_A0	K25	--	19	--					DAD data sheet	
RST_A1	J26	--	18	--					DAD data sheet	
RST_A2	J25	--	17	--					DAD data sheet	
RST_A3	K26	--	16	--					DAD data sheet	
RST_SEL0	G27	--	5	--					DAD data sheet	
RST_SEL1	G26	--	4	--					DAD data sheet	
RST_IRQ\	M25	--	43	--				1 kΩ to VCC_3P3V	DAD data sheet	
RST_OE\	M28	--	6	--				1 kΩ to VCC_3P3V	DAD data sheet	
RST_RST\	H24	--	59	--				1 kΩ to VCC_3P3V	DAD data sheet	
DLP5500 DMD Micromirror Reset Pulse Signal										
MBRST0	--	C3	22	--				10-Ω series resistor	MBRST	
MBRST1	--	D2	24	--				10-Ω series resistor	MBRST	
MBRST2	--	D3	27	--				10-Ω series resistor	MBRST	
MBRST3	--	E2	29	--				10-Ω series resistor	MBRST	
MBRST4	--	G3	32	--				10-Ω series resistor	MBRST	
MBRST5	--	E1	34	--				10-Ω series resistor	MBRST	
MBRST6	--	G2	37	--				10-Ω series resistor	MBRST	
MBRST7	--	G1	39	--				10-Ω series resistor	MBRST	
MBRST8	--	N3	62	--				10-Ω series resistor	MBRST	
MBRST9	--	M2	64	--				10-Ω series resistor	MBRST	
MBRST10	--	M3	67	--				10-Ω series resistor	MBRST	
MBRST11	--	L2	69	--				10-Ω series resistor	MBRST	
MBRST12	--	J3	72	--				10-Ω series resistor	MBRST	
MBRST13	--	L1	74	--				10-Ω series resistor	MBRST	
MBRST14	--	J2	77	--				10-Ω series resistor	MBRST	
MBRST15	--	J1	79	--				10-Ω series resistor	MBRST	
DLPA200 Specialized Voltage Rails for Micromirror Reset Pulses										
VCC2, VOFFSET, VOFFSET_RAIL		C1, D1, M1, N1	23, 28, 33, 38, 49, 63, 68, 73, 78					See DLPA200 and DLP5500 data sheets		
VBIAS			9					See DLPA200 data sheet		
VBIAS_LHI			10					See DLPA200 datasheet		
VBIAS_SWL			8					See DLPA200 data sheet		

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
VBIAS_RAIL			21, 30, 31, 40, 61, 70, 71, 80					See DLPA200 data sheet		
VRESET			13					See DLPA200 data sheet		
VRESET_SWL			12					See DLPA200 data sheet		
VRESET_RAIL			25, 26, 35,36, 65, 66, 75, 76					See DLPA200 data sheet		
V5REG			47					See DLPA200 data sheet		
P12V			11, 48, 50					See DLPA200 data sheet		
{ DEV_ID1 }	--	--	45	--				1-kΩ pulldown to DGND	DAD datasheet	
{ DEV_ID0 }	--	--	44	--				1-kΩ pulldown to DGND	DAD datasheet	
DLP5500 LVDS Data and Control interface from DLPC200										
DMD_CLK_AN	U28	D19	--	--					LVDS	
DMD_CLK_AP	T25	E19	--	--					LVDS	
DMD_CLK_BN	U26	N19	--	--					LVDS	
DMD_CLK_BP	U25	M19	--	--					LVDS	
DMD_DAT_AN1	AB28	G20	--	--					LVDS	
DMD_DAT_AN11	V26	B18	--	--					LVDS	
DMD_DAT_AN13	V24	A20	--	--					LVDS	
DMD_DAT_AN15	U27	B19	--	--					LVDS	
DMD_DAT_AN3	Y26	H19	--	--					LVDS	
DMD_DAT_AN5	W26	F18	--	--					LVDS	
DMD_DAT_AN7	W27	E18	--	--					LVDS	
DMD_DAT_AN9	V28	C20	--	--					LVDS	
DMD_DAT_AP1	AB27	H20	--	--					LVDS	
DMD_DAT_AP11	V25	A18	--	--					LVDS	
DMD_DAT_AP13	V23	B20	--	--					LVDS	
DMD_DAT_AP15	T26	A19	--	--					LVDS	
DMD_DAT_AP3	Y25	G19	--	--					LVDS	
DMD_DAT_AP5	W25	G18	--	--					LVDS	
DMD_DAT_AP7	W28	D18	--	--					LVDS	
DMD_DAT_AP9	V27	D20	--	--					LVDS	
DMD_DAT_BN1	AC25	K20	--	--					LVDS	
DMD_DAT_BN11	AC28	R18	--	--					LVDS	
DMD_DAT_BN13	AB26	T20	--	--					LVDS	
DMD_DAT_BN15	AA26	R19	--	--					LVDS	
DMD_DAT_BN3	AD26	J19	--	--					LVDS	
DMD_DAT_BN5	AE28	L18	--	--					LVDS	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DMD_DAT_BN7	AD28	M18	--	--					LVDS	
DMD_DAT_BN9	Y24	P20	--	--					LVDS	
DMD_DAT_BP1	AC24	J20	--	--					LVDS	
DMD_DAT_BP11	AC27	T18	--	--					LVDS	
DMD_DAT_BP13	AB25	R20	--	--					LVDS	
DMD_DAT_BP15	AA25	T19	--	--					LVDS	
DMD_DAT_BP3	AC26	K19	--	--					LVDS	
DMD_DAT_BP5	AE27	K18	--	--					LVDS	
DMD_DAT_BP7	AD27	N18	--	--					LVDS	
DMD_DAT_BP9	Y23	N20	--	--					LVDS	
DMD_SCTRL_AN	R26	F20	--	--					LVDS	
DMD_SCTRL_AP	R25	E20	--	--					LVDS	
DMD_SCTRL_BN	T22	L20	--	--					LVDS	
DMD_SCTRL_BP	T21	M20	--	--					LVDS	
MODE_A	--	A4	--	--				Connect to GND	--	Set to low/GND
DMD_PWRDN\	P26	B9	--	--					LVDS	
SDRAM (DDR2) Interface										
MEM_A0	AD24	--	--	--				56-Ω pullup to 0.9 V		
MEM_A1	AF21	--	--	--				56-Ω pullup to 0.9 V		
MEM_A2	AG23	--	--	--				56-Ω pullup to 0.9 V		
MEM_A3	AE8	--	--	--				56-Ω pullup to 0.9 V		
MEM_A4	AG12	--	--	--				56-Ω pullup to 0.9 V		
MEM_A5	AF23	--	--	--				56-Ω pullup to 0.9 V		
MEM_A6	AC17	--	--	--				56-Ω pullup to 0.9 V		
MEM_A7	AA16	--	--	--				56-Ω pullup to 0.9 V		
MEM_A8	AE23	--	--	--				56-Ω pullup to 0.9 V		
MEM_A9	AE22	--	--	--				56-Ω pullup to 0.9 V		
MEM_A10	AE16	--	--	--				56-Ω pullup to 0.9 V		
MEM_A11	AD25	--	--	--				56-Ω pullup to 0.9 V		
MEM_A12	AF19	--	--	--				56-Ω pullup to 0.9 V		
MEM_A13	AH10	--	--	--				56-Ω pullup to 0.9 V		
MEM_A14	AA8	--	--	--				56-Ω pullup to 0.9 V		
MEM_A15	AD11	--	--	--				56-Ω pullup to 0.9 V		
MEM_BA0	Y19	--	--	--				56-Ω pullup to 0.9 V		
MEM_BA1	AD21	--	--	--				56-Ω pullup to 0.9 V		
MEM_BA2	AE7	--	--	--				56-Ω pullup to 0.9 V		
MEM_CKE0	AF12	--	--	--				56-Ω pullup to 0.9 V		
MEM_CAS\	AG19	--	--	--				56-Ω pullup to 0.9 V		

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
MEM_CS0\	AF13	--	--	--				56-Ω pullup to 0.9 V		
MEM_RAS\	AE20	--	--	--				56-Ω pullup to 0.9 V		
MEM_WE\	AG25	--	--	--				56-Ω pullup to 0.9 V		
MEM_ODT	AH12	--	--	--				56-Ω pullup to 0.9 V		
MEM_CLK_N0	R1	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_P0	R2	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_N1	U4	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_P1	U3	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_N2	AC4	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_P2	AC5	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_N3	AF14	--	--	--				100-Ω resistor between N and P differential signal		
MEM_CLK_P3	AE14	--	--	--				100-Ω resistor between N and P differential signal		
MEM_D0	R3	--	--	--				51-Ω pullup to 0.9 V		
MEM_D1	R4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D2	T4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D3	R5	--	--	--				51-Ω pullup to 0.9 V		
MEM_D4	U1	--	--	--				51-Ω pullup to 0.9 V		
MEM_D5	V4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D6	V2	--	--	--				51-Ω pullup to 0.9 V		
MEM_D7	V1	--	--	--				51-Ω pullup to 0.9 V		
MEM_D8	U6	--	--	--				51-Ω pullup to 0.9 V		
MEM_D9	Y4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D10	AC2	--	--	--				51-Ω pullup to 0.9 V		
MEM_D11	AC1	--	--	--				51-Ω pullup to 0.9 V		
MEM_D12	AC3	--	--	--				51-Ω pullup to 0.9 V		
MEM_D13	AD2	--	--	--				51-Ω pullup to 0.9 V		
MEM_D14	AB3	--	--	--				51-Ω pullup to 0.9 V		
MEM_D15	AA4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D16	AE6	--	--	--				51-Ω pullup to 0.9 V		
MEM_D17	AF4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D18	AG3	--	--	--				51-Ω pullup to 0.9 V		
MEM_D19	AH3	--	--	--				51-Ω pullup to 0.9 V		
MEM_D20	AF6	--	--	--				51-Ω pullup to 0.9 V		

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
MEM_D21	AH4	--	--	--				51-Ω pullup to 0.9 V		
MEM_D22	AD8	--	--	--				51-Ω pullup to 0.9 V		
MEM_D23	AG6	--	--	--				51-Ω pullup to 0.9 V		
MEM_D24	AB9	--	--	--				51-Ω pullup to 0.9 V		
MEM_D25	AD10	--	--	--				51-Ω pullup to 0.9 V		
MEM_D26	AG7	--	--	--				51-Ω pullup to 0.9 V		
MEM_D27	AH7	--	--	--				51-Ω pullup to 0.9 V		
MEM_D28	AC8	--	--	--				51-Ω pullup to 0.9 V		
MEM_D29	AA10	--	--	--				51-Ω pullup to 0.9 V		
MEM_D30	AG8	--	--	--				51-Ω pullup to 0.9 V		
MEM_D31	AH8	--	--	--				51-Ω pullup to 0.9 V		
MEM_D32	AF8	--	--	--				51-Ω pullup to 0.9 V		
MEM_D33	AE9	--	--	--				51-Ω pullup to 0.9 V		
MEM_D34	AF10	--	--	--				51-Ω pullup to 0.9 V		
MEM_D35	AG10	--	--	--				51-Ω pullup to 0.9 V		
MEM_D36	AE12	--	--	--				51-Ω pullup to 0.9 V		
MEM_D37	AE11	--	--	--				51-Ω pullup to 0.9 V		
MEM_D38	AG11	--	--	--				51-Ω pullup to 0.9 V		
MEM_D39	AH11	--	--	--				51-Ω pullup to 0.9 V		
MEM_D40	AC15	--	--	--				51-Ω pullup to 0.9 V		
MEM_D41	AF15	--	--	--				51-Ω pullup to 0.9 V		
MEM_D42	AG17	--	--	--				51-Ω pullup to 0.9 V		
MEM_D43	AH17	--	--	--				51-Ω pullup to 0.9 V		
MEM_D44	AF16	--	--	--				51-Ω pullup to 0.9 V		
MEM_D45	AB16	--	--	--				51-Ω pullup to 0.9 V		
MEM_D46	AE17	--	--	--				51-Ω pullup to 0.9 V		
MEM_D47	AG18	--	--	--				51-Ω pullup to 0.9 V		
MEM_D48	AH19	--	--	--				51-Ω pullup to 0.9 V		
MEM_D49	AD17	--	--	--				51-Ω pullup to 0.9 V		
MEM_D50	AG21	--	--	--				51-Ω pullup to 0.9 V		
MEM_D51	AH21	--	--	--				51-Ω pullup to 0.9 V		
MEM_D52	AG22	--	--	--				51-Ω pullup to 0.9 V		
MEM_D53	AH22	--	--	--				51-Ω pullup to 0.9 V		
MEM_D54	AH23	--	--	--				51-Ω pullup to 0.9 V		
MEM_D55	AE19	--	--	--				51-Ω pullup to 0.9 V		
MEM_D56	AF25	--	--	--				51-Ω pullup to 0.9 V		
MEM_D57	AF20	--	--	--				51-Ω pullup to 0.9 V		
MEM_D58	AD18	--	--	--				51-Ω pullup to 0.9 V		

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
MEM_D59	AE21	--	--	--				51-Ω pullup to 0.9 V		
MEM_D60	AE25	--	--	--				51-Ω pullup to 0.9 V		
MEM_D61	AH25	--	--	--				51-Ω pullup to 0.9 V		
MEM_D62	AF22	--	--	--				51-Ω pullup to 0.9 V		
MEM_D63	AE24	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM0	W2	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM1	AE2	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM2	AH6	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM3	AF7	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM4	AE13	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM5	AH18	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM6	AF24	--	--	--				51-Ω pullup to 0.9 V		
MEM_DM7	AG26	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS0	AB2	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS1	AE3	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS2	AD7	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS3	AE10	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS4	AF11	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS5	AF17	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS6	AE18	--	--	--				51-Ω pullup to 0.9 V		
MEM_DS7	AF26	--	--	--				51-Ω pullup to 0.9 V		
FLASH_SRAM_A0	D13	--	--	--	Unused					
FLASH_SRAM_A1	A11	--	--	--	NOR_FLASH pin 29		SRAM pin 5			
FLASH_SRAM_A2	C11	--	--	--	NOR_FLASH pin 25		SRAM pin 4			
FLASH_SRAM_A3	D11	--	--	--	NOR_FLASH pin 24		SRAM pin 3			
FLASH_SRAM_A4	A12	--	--	--	NOR_FLASH pin 23		SRAM pin 2			
FLASH_SRAM_A5	B12	--	--	--	NOR_FLASH pin 22		SRAM pin 1			
FLASH_SRAM_A6	D10	--	--	--	NOR_FLASH pin 21		SRAM pin 44			
FLASH_SRAM_A7	A10	--	--	--	NOR_FLASH pin 20		SRAM pin 43			
FLASH_SRAM_A8	B10	--	--	--	NOR_FLASH pin 19		SRAM pin 42			
FLASH_SRAM_A9	B8	--	--	--	NOR_FLASH pin 8		SRAM pin 27			
FLASH_SRAM_A10	C8	--	--	--	NOR_FLASH pin 7		SRAM pin 26			
FLASH_SRAM_A11	A7	--	--	--	NOR_FLASH pin 6		SRAM pin 25			
FLASH_SRAM_A12	B7	--	--	--	NOR_FLASH pin 5		SRAM pin 24			
FLASH_SRAM_A13	A4	--	--	--	NOR_FLASH pin 4		SRAM pin 22			
FLASH_SRAM_A14	D7	--	--	--	NOR_FLASH pin 3		SRAM pin 21			
FLASH_SRAM_A15	C6	--	--	--	NOR_FLASH pin 2		SRAM pin 20			
FLASH_SRAM_A16	D8	--	--	--	NOR_FLASH pin 1		SRAM pin 19			

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
FLASH_SRAM_A17	B6	--	--	--	NOR_FLASH pin 55		SRAM pin 18			
FLASH_SRAM_A18	C7	--	--	--	NOR_FLASH pin 18		No connect			
FLASH_SRAM_A19	A8	--	--	--	NOR_FLASH pin 17		No connect			
FLASH_SRAM_A20	C4	--	--	--	NOR_FLASH pin 16		No connect			
FLASH_SRAM_A21	B3	--	--	--	NOR_FLASH pin 11		No connect			
FLASH_SRAM_A22	A3	--	--	--	NOR_FLASH pin 10		No connect			
FLASH_SRAM_A23	C5	--	--	--	NOR_FLASH pin 9		No connect			
FLASH_SRAM_A24	D5	--	--	--	NOR_FLASH pin 26		No connect			
FLASH_SRAM_A25	B4	--	--	--	NOR_FLASH pin 27		No connect			
FLASH_SRAM_A26	D4	--	--	--	NOR_FLASH pin 28		No connect			
FLASH_SRAM_D0	E11	--	--	--	NOR_FLASH pin 34		SRAM pin 7			
FLASH_SRAM_D1	F10	--	--	--	NOR_FLASH pin 36		SRAM pin 8			
FLASH_SRAM_D2	E10	--	--	--	NOR_FLASH pin 39		SRAM pin 9			
FLASH_SRAM_D3	G9	--	--	--	NOR_FLASH pin 41		SRAM pin 10			
FLASH_SRAM_D4	E8	--	--	--	NOR_FLASH pin 47		SRAM pin 13			
FLASH_SRAM_D5	E7	--	--	--	NOR_FLASH pin 49		SRAM pin 14			
FLASH_SRAM_D6	E5	--	--	--	NOR_FLASH pin 51		SRAM pin 15			
FLASH_SRAM_D7	E4	--	--	--	NOR_FLASH pin 53		SRAM pin 16			
FLASH_SRAM_D8	F11	--	--	--	NOR_FLASH pin 35		SRAM pin 29			
FLASH_SRAM_D9	E12	--	--	--	NOR_FLASH pin 37		SRAM pin 30			
FLASH_SRAM_D10	F12	--	--	--	NOR_FLASH pin 40		SRAM pin 31			
FLASH_SRAM_D11	G12	--	--	--	NOR_FLASH pin 42		SRAM pin 32			
FLASH_SRAM_D12	G13	--	--	--	NOR_FLASH pin 48		SRAM pin 35			
FLASH_SRAM_D13	H13	--	--	--	NOR_FLASH pin 50		SRAM pin 36			
FLASH_SRAM_D14	F14	--	--	--	NOR_FLASH pin 52		SRAM pin 37			
FLASH_SRAM_D15	G14	--	--	--	NOR_FLASH pin 54		SRAM pin 38			
FLASH_CE\	D12	--	--	--	NOR_FLASH pin 30		No connect			
FLASH_SRAM_OE\	C10	--	--	--	NOR_FLASH pin 32		SRAM pin 41			
FLASH_SRAM_RST\	C12	--	--	--	NOR_FLASH pin 44		No connect			Connect to system global $\overline{\text{RESET}}$
FLASH_SRAM_WE\	A6	--	--	--	NOR_FLASH pin 14		SRAM pin 17			
FLASH_SRAM_RDY	C13	--	--	--	NOR_FLASH pin 56		No connect			
SRAM_CE\	B11	--	--	--	No connect		SRAM pin 6			
SRAM_LB\	D9	--	--	--	No connect		SRAM pin 39			
SRAM_UB\	C9	--	--	--	No connect		SRAM pin 40			
DGND/VSS	AA2	A6	1	10						
DGND/VSS	AA27	A11	7	--						
DGND/VSS	AC13	A13	14	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DGND/VSS	AC16	A15	20	--						
DGND/VSS	AC20	A17	41	--						
DGND/VSS	AC23	B4	46	--						
DGND/VSS	AC6	B5	53	--						
DGND/VSS	AC9	B8	55	--						
DGND/VSS	AF1	B14	60	--						
DGND/VSS	AF28	B15	--	--						
DGND/VSS	AG13	B17	--	--						
DGND/VSS	AG16	C2	--	--						
DGND/VSS	AG2	C18	--	--						
DGND/VSS	AG20	C19	--	--						
DGND/VSS	AG24	F1	--	--						
DGND/VSS	AG27	F2	--	--						
DGND/VSS	AG5	F19	--	--						
DGND/VSS	AG9	H1	--	--						
DGND/VSS	B13	H2	--	--						
DGND/VSS	B16	H3	--	--						
DGND/VSS	B2	H18	--	--						
DGND/VSS	B20	J18	--	--						
DGND/VSS	B24	K1	--	--						
DGND/VSS	B27	K2	--	--						
DGND/VSS	B5	L19	--	--						
DGND/VSS	B9	N2	--	--						
DGND/VSS	C1	P18	--	--						
DGND/VSS	C28	P19	--	--						
DGND/VSS	F13	R4	--	--						
DGND/VSS	F16	R9	--	--						
DGND/VSS	F20	R14	--	--						
DGND/VSS	F23	R15	--	--						
DGND/VSS	F6	T7	--	--						
DGND/VSS	F9	T13	--	--						
DGND/VSS	H2	T15	--	--						
DGND/VSS	H27	T17	--	--						
DGND	J11	--	--	--						
DGND	J18	--	--	--						
DGND	K10	--	--	--						
DGND	K12	--	--	--						
DGND	K14	--	--	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DGND	K16	--	--	--						
DGND	K18	--	--	--						
DGND	K20	--	--	--						
DGND	K23	--	--	--						
DGND	K6	--	--	--						
DGND	L11	--	--	--						
DGND	L13	--	--	--						
DGND	L15	--	--	--						
DGND	L17	--	--	--						
DGND	L19	--	--	--						
DGND	L9	--	--	--						
DGND	M10	--	--	--						
DGND	M12	--	--	--						
DGND	M14	--	--	--						
DGND	M16	--	--	--						
DGND	M18	--	--	--						
DGND	M20	--	--	--						
DGND	N11	--	--	--						
DGND	N13	--	--	--						
DGND	N15	--	--	--						
DGND	N17	--	--	--						
DGND	N19	--	--	--						
DGND	N2	--	--	--						
DGND	N23	--	--	--						
DGND	N27	--	--	--						
DGND	N6	--	--	--						
DGND	N9	--	--	--						
DGND	P10	--	--	--						
DGND	P12	--	--	--						
DGND	P14	--	--	--						
DGND	P16	--	--	--						
DGND	P18	--	--	--						
DGND	P20	--	--	--						
DGND	R11	--	--	--						
DGND	R13	--	--	--						
DGND	R15	--	--	--						
DGND	R17	--	--	--						
DGND	R19	--	--	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DGND	R9	--	--	--						
DGND	T10	--	--	--						
DGND	T12	--	--	--						
DGND	T14	--	--	--						
DGND	T16	--	--	--						
DGND	T18	--	--	--						
DGND	T2	--	--	--						
DGND	T20	--	--	--						
DGND	T23	--	--	--						
DGND	T27	--	--	--						
DGND	T6	--	--	--						
DGND	U11	--	--	--						
DGND	U13	--	--	--						
DGND	U15	--	--	--						
DGND	U17	--	--	--						
DGND	U19	--	--	--						
DGND	U9	--	--	--						
DGND	V10	--	--	--						
DGND	V12	--	--	--						
DGND	V14	--	--	--						
DGND	V16	--	--	--						
DGND	V18	--	--	--						
DGND	V20	--	--	--						
DGND	W11	--	--	--						
DGND	W13	--	--	--						
DGND	W15	--	--	--						
DGND	W17	--	--	--						
DGND	W19	--	--	--						
DGND	W23	--	--	--						
DGND	W6	--	--	--						
DGND	W9	--	--	--						
DGND	Y11	--	--	--						
DGND	Y18	--	--	--				See DLPC200 datasheet		Should be connected to an isolated ground
DGND2	H9	--	--	--				See DLPC200 datasheet		Should be connected to an isolated ground
DGND2	H20	--	--	--				See DLPC200 datasheet		Should be connected to an isolated ground

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
DGND2	AA9	--	--	--				See DLPC200 datasheet		Should be connected to an isolated ground
DGND2	AA20	--	--	--						
VCC_1P2V	K11	--	--	--						
VCC_1P2V	K13	--	--	--						
VCC_1P2V	K15	--	--	--						
VCC_1P2V	K17	--	--	--						
VCC_1P2V	K19	--	--	--						
VCC_1P2V	K9	--	--	--						
VCC_1P2V	L10	--	--	--						
VCC_1P2V	L12	--	--	--						
VCC_1P2V	L14	--	--	--						
VCC_1P2V	L16	--	--	--						
VCC_1P2V	L18	--	--	--						
VCC_1P2V	L20	--	--	--						
VCC_1P2V	M11	--	--	--						
VCC_1P2V	M13	--	--	--						
VCC_1P2V	M15	--	--	--						
VCC_1P2V	M17	--	--	--						
VCC_1P2V	M19	--	--	--						
VCC_1P2V	M9	--	--	--						
VCC_1P2V	N10	--	--	--						
VCC_1P2V	N12	--	--	--						
VCC_1P2V	N14	--	--	--						
VCC_1P2V	N16	--	--	--						
VCC_1P2V	N18	--	--	--						
VCC_1P2V	N20	--	--	--						
VCC_1P2V	P11	--	--	--						
VCC_1P2V	P13	--	--	--						
VCC_1P2V	P15	--	--	--						
VCC_1P2V	P17	--	--	--						
VCC_1P2V	P19	--	--	--						
VCC_1P2V	P9	--	--	--						
VCC_1P2V	R10	--	--	--						
VCC_1P2V	R12	--	--	--						
VCC_1P2V	R14	--	--	--						
VCC_1P2V	R16	--	--	--						
VCC_1P2V	R18	--	--	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
VCC_1P2V	R20	--	--	--						
VCC_1P2V	T11	--	--	--						
VCC_1P2V	T13	--	--	--						
VCC_1P2V	T15	--	--	--						
VCC_1P2V	T17	--	--	--						
VCC_1P2V	T19	--	--	--						
VCC_1P2V	T9	--	--	--						
VCC_1P2V	U10	--	--	--						
VCC_1P2V	U12	--	--	--						
VCC_1P2V	U14	--	--	--						
VCC_1P2V	U16	--	--	--						
VCC_1P2V	U18	--	--	--						
VCC_1P2V	U20	--	--	--						
VCC_1P2V	V11	--	--	--						
VCC_1P2V	V13	--	--	--						
VCC_1P2V	V15	--	--	--						
VCC_1P2V	V17	--	--	--						
VCC_1P2V	V19	--	--	--						
VCC_1P2V	V9	--	--	--						
VCC_1P2V	W10	--	--	--						
VCC_1P2V	W12	--	--	--						
VCC_1P2V	W14	--	--	--						
VCC_1P2V	W16	--	--	--						
VCC_1P2V	W18	--	--	--						
VCC_1P2V	W20	--	--	--						
VCC_1P8V	AA1	--	--	--						
VCC_1P8V	AA11	--	--	--						
VCC_1P8V	AA18	--	--	--						
VCC_1P8V	AD13	--	--	--						
VCC_1P8V	AD16	--	--	--						
VCC_1P8V	AD20	--	--	--						
VCC_1P8V	AD23	--	--	--						
VCC_1P8V	AD6	--	--	--						
VCC_1P8V	AD9	--	--	--						
VCC_1P8V	AG1	--	--	--						
VCC_1P8V	AH13	--	--	--						
VCC_1P8V	AH16	--	--	--						
VCC_1P8V	AH2	--	--	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
VCC_1P8V	AH20	--	--	--						
VCC_1P8V	AH24	--	--	--						
VCC_1P8V	AH27	--	--	--						
VCC_1P8V	AH5	--	--	--						
VCC_1P8V	AH9	--	--	--						
VCC_1P8V	T1	--	--	--						
VCC_1P8V	T5	--	--	--						
VCC_1P8V	W5	--	--	--						
VCC_2P5V	AA28	--	--	--						
VCC_2P5V	AG28	--	--	--						
VCC_2P5V	T24	--	--	--						
VCC_2P5V	T28	--	--	--						
VCC_2P5V	W24	--	--	--						
VCC_3P3V	A13	A12	--	--						
VCC_3P3V	A16	A14	--	--						
VCC_3P3V	A2	A16	--	--						
VCC_3P3V	A20	B11	--	--						
VCC_3P3V	A24	B12	--	--						
VCC_3P3V	A27	B13	--	--						
VCC_3P3V	A5	B16	--	--						
VCC_3P3V	A9	R12	--	--						
VCC_3P3V	B1	R13	--	--						
VCC_3P3V	B28	R16	--	--						
VCC_3P3V	E13	R17	--	--						
VCC_3P3V	E16	T12	--	--						
VCC_3P3V	E20	T14	--	--						
VCC_3P3V	E23	T16	--	--						
VCC_3P3V	E6	--	--	--						
VCC_3P3V	E9	--	--	--						
VCC_3P3V	H1	--	--	--						
VCC_3P3V	H11	--	--	--						
VCC_3P3V	H18	--	--	--						
VCC_3P3V	H28	--	--	--						
VCC_3P3V	K24	--	--	--						
VCC_3P3V	K5	--	--	--						
VCC_3P3V	N1	--	--	--						
VCC_3P3V	N24	--	--	--						
VCC_3P3V	N28	--	--	--						

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
VCC_3P3V	N5	--	--	--						
VCCA	J21	--	--	--						
VCCA	J8	--	--	--						
VCCA	Y21	--	--	--						
VCCA	Y8	--	--	--						
VCCD_PLL	J20	--	--	--						
VCCD_PLL	J9	--	--	--						
VCCD_PLL	Y20	--	--	--						
VCCD_PLL	Y9	--	--	--						
VREF_B2	AB4	--	--	--						
VREF_B2	T7	--	--	--						
VREF_B2	T8	--	--	--						
VREF_B4	AA15	--	--	--						
VREF_B3	AB11	--	--	--						
VREF_B3	AB13	--	--	--						
VREF_B4	AB20	--	--	--						
VREF_B4	AC18	--	--	--						
VREF_B3	Y10	--	--	--						
RESERVED_R7		R7						Connected to VSS, see DLP5500 data sheet		
RESERVED_R8		R8						Connected to VSS, see DLP5500 data sheet		
RESERVED_T8		T8						Connected to VSS, see DLP5500 data sheet		
RESERVED_B6		B6						Connected to VSS, see DLP5500 data sheet		
RSVD_D0	A17	--	--	--	No connection			--	--	Reserved for future use
RSVD_D1	D15	--	--	--	No connection			--	--	Reserved for future use
RSVD_D2	E17	--	--	--	No connection			--	--	Reserved for future use
RSVD_D3	F15	--	--	--	No connection			--	--	Reserved for future use
RSVD_G0	C23	--	--	--	No connection			--	--	Reserved for future use
RSVD_G1	F19	--	--	--	No connection			--	--	Reserved for future use
RSVD_G2	M27	--	--	--	No connection			--	--	Reserved for future use
RSVD_G3	N21	--	--	--	No connection			--	--	Reserved for future use
RSVD_G4	P27	--	--	--	No connection			--	--	Reserved for future use
RSVD_G5	A18	--	--	--	No connection			--	--	Reserved for future use
RSVD_G6	A19	--	--	--	No connection			--	--	Reserved for future use
RSVD_H1	C2	--	--	--	No connection			--	--	Reserved for future use
RSVD_H10	N4	--	--	--	No connection			--	--	Reserved for future use

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
RSVD_H11	L2	--	--	--	No connection			--	--	Reserved for future use
RSVD_H12	K4	--	--	--	No connection			--	--	Reserved for future use
RSVD_H13	J1	--	--	--	No connection			--	--	Reserved for future use
RSVD_H2	E1	--	--	--	No connection			--	--	Reserved for future use
RSVD_H3	E3	--	--	--	No connection			--	--	Reserved for future use
RSVD_H4	G6	--	--	--	No connection			--	--	Reserved for future use
RSVD_H5	G5	--	--	--	No connection			--	--	Reserved for future use
RSVD_H6	G1	--	--	--	No connection			--	--	Reserved for future use
RSVD_H7	H7	--	--	--	No connection			--	--	Reserved for future use
RSVD_H8	L5	--	--	--	No connection			--	--	Reserved for future use
RSVD_H9	M5	--	--	--	No connection			--	--	Reserved for future use
RSVD_P0	P7	--	--	--	No connection			--	--	Reserved for future use
RSVD_P1	P6	--	--	--	No connection			--	--	Reserved for future use
RSVD_P2	P8	--	--	--	No connection			--	--	Reserved for future use
RSVD_P3	P5	--	--	--	No connection			--	--	Reserved for future use
RSVD_S0	AA24	--	--	--	No connection			--	--	Reserved for future use
RSVD_S1	AG14	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_S2	AG15	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_S3	AH14	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_S4	AH26	--	--	--	No connection			--	--	Reserved for future use
RSVD_S5	B25	--	--	--	No connection			--	--	Reserved for future use
RSVD_S6	C20	--	--	--	No connection			--	--	Reserved for future use
RSVD_S8	D19	--	--	--	No connection			--	--	Reserved for future use
RSVD_S10	F22	--	--	--	No connection			--	--	Reserved for future use
RSVD_S11	K28	--	--	--	No connection			--	--	Reserved for future use
RSVD_S14	N25	--	--	--	No connection			--	--	Reserved for future use
RSVD_S16	R27	--	--	--	No connection			--	--	Reserved for future use
RSVD_S17	R28	--	--	--	No connection			--	--	Reserved for future use
RSVD_S18	U23	--	--	--	No connection			--	--	Reserved for future use
RSVD_S19	U24	--	--	--	No connection			--	--	Reserved for future use
RSVD_S20	Y27	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_S21	Y28	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_T0	E22	--	--	--	No connection			--	--	Reserved for future use
RSVD_T1	D21	--	--	--	No connection			--	--	Reserved for future use
RSVD_T2	A21	--	--	--	No connection			--	--	Reserved for future use
RSVD_T3	C18	--	--	--	No connection			--	--	Reserved for future use
RSVD_T4	B22	--	--	--	No connection			--	--	Reserved for future use
RSVD_T5	B21	--	--	--	No connection			--	--	Reserved for future use

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
RSVD_T6	D17	--	--	--	No connection			--	--	Reserved for future use
RSVD_T7	E21	--	--	--	No connection			--	--	Reserved for future use
RSVD_TC	M24	--	--	--	No connection			--	--	Reserved for future use
RSVD_X0	AF18	--	--	--	No connection			--	--	Reserved for future use
RSVD_X1	AD15	--	--	--	No connection			--	--	Reserved for future use
RSVD_X10	AB23	--	--	--	No connection			--	--	Reserved for future use
RSVD_X11	AH15	--	--	--	Connect to DGND		Unused input	--	--	Reserved for future use
RSVD_X12	U8	--	--	--	No connection			--	--	Reserved for future use
RSVD_X13	U7	--	--	--	No connection			--	--	Reserved for future use
RSVD_X14	AB17	--	--	--	No connection			--	--	Reserved for future use
RSVD_X15	AA17	--	--	--	No connection			--	--	Reserved for future use
RSVD_X2	AE15	--	--	--	No connection			--	--	Reserved for Future use
RSVD_X3	AC21	--	--	--	No connection			--	--	Reserved for future use
RSVD_X4	AF9	--	--	--	No connection			--	--	Reserved for future use
RSVD_X5	E24	--	--	--	No connection			--	--	Reserved for future use
RSVD_X6	AB24	--	--	--	No connection			--	--	Reserved for future use
RSVD_X7	R24	--	--	--	No connection			--	--	Reserved for future use
RSVD_X8	AF27	--	--	--	No connection			--	--	Reserved for future use
RSVD_X9	AA22	--	--	--	No connection			--	--	Reserved for future use

Copyright © 2010–2012, Texas Instruments Incorporated

Table 9-1. Terminal Interconnection (continued)

SIGNAL NAME	PIN NUMBER				SYSTEM COMPONENT CONNECTION			SYSTEM TERMINATION	LAYOUT CONSIDERATIONS	NOTES
	DLPC200	DLP5500	DLPA200	"DLPR200F (DLP CONFIG PROM)"						
No_connect	C3, F7, G7, G8, G10, G11, G19, G20,G21, G22, G23, G24, H8, H10, H12,H14, H15, H16, H17, H19, H21, H22, J5,J6, J7, J10, J12, J13, J14, J15, J16, J17,J19, J23, J24, K7, K8, K21, K22, L6, L7,L8, L21, L22, M7, M8, M23, N8, P21, R7, R21, R22, R23, U21, U22, V5, V6, V7, V8, V21, V22, W4, W7, W8, W21, W22, Y5, Y6, Y7, Y12, Y13, Y14, Y15,Y16, Y17, Y22, AA5, AA6, AA7, AA12, AA13, AA14, AA19, AA21, AA23, AB10, AB12, AB14, AB15, AB18, AB19, AB2, AB22, AC10, AC12, AC14, AC19, AC22, AD14, AD19, AD22, AE26	A3, A7, A10, B2, B3, B10, E3, F3, K3, L3, P1, P2, P3, R1, R2, R3, R5, R6, R10, R11, T1, T2, T3, T4, T5, T6, T9, T10, T11	51, 52, 54	2, 3, 4, 5, 6, 10, 11, 12, 13, 14				No system termination should be made.		

Copyright © 2010–2012, Texas Instruments Incorporated

Copyright © 2010–2012, Texas Instruments Incorporated

10 Printed Circuit Board (PCB) System Design

The 0.55 XGA Chipset is a high-performance (high-frequency and high-bandwidth) set of components. This section provides guidelines and PCB design rules that are required in order to ensure proper operation of the 0.55 XGA chipset. The guidelines and design rules described in this section have been implemented and verified in a PCB reference design (*Ref Design*) used in the DLP LightCommander Kit. (www.ti.com/dlplightcommander).

10.1 Printed Circuit Layer Stack-Up

The 0.55 XGA chipset Ref Design is implemented with 10 layers, with layer stack-up and copper weight for each layer as shown in Table 10-1. All of the components in the system block diagram and 0.55 XGA chipset are lead-free, and therefore the PCB should also be designed for lead-free assembly.

The PCB Layer stack may vary depending on system design. However, careful attention must be kept in order to meet design considerations listed in the following sections.

Table 10-1. Layer Stack-Up(1)

LAYER NO.	LAYER NAME	COPPER WT.	COMMENTS
1	Side A – primary components	½ oz (0.018-mm thick) (before plating)	Top-side components Low-frequency signal routing, GND, 1.8 V, and 1.2 V Copper fill (GND) plated up to 1 oz. (0.035-mm thick)
2	Ground	1 oz. (0.035-mm thick)	Reference for signal layer
3	Signal (high-frequency)	½ oz. (0.018-mm thick)	Signal layer - Priority DDR2 (SDRAM) and LVDS, then others
4	Signal	½ oz. (0.018-mm thick)	Signal layer
5	Power	1 oz. (0.035-mm thick)	Split 3.3-V, 1.5-V, 5-V, and VCC2 power planes. May include any necessary mini planes for 1.8 V, 12 V, and 1.2 V.
6	Ground	1 oz. (0.035-mm thick)	Reference for signal layer
7	Signal (high-frequency)	½ oz. (0.018-mm thick)	Signal layer - Priority DDR2 (SDRAM) and LVDS, then other signal layer
8	Signal (high-frequency)	½ oz. (0.018-mm thick)	Signal layer - Priority DDR2 (SDRAM) and LVDS, then other signal layer
9	Ground	1 oz. (0.035-mm thick)	Reference for signal layer
10	Side B – secondary components	½ oz (0.018-mm thick) (before plating)	Discrete components, low-frequency signals routing, 2.5 V, and GND Copper fill (GND) plated up to 1 oz. (0.035-mm thick)

(1) Routing on external layers should be less than 0.25” for priority signals.

10.2 Trace Impedance, Width and Spacing, Device Placement

10.2.1 Impedance Requirements

Unless otherwise noted, the signals on the 0.55 XGA chipset PCB should be routed to have matched impedance of 50 Ω ±10% for all signals. The exceptions are listed in Table 10-2.

Table 10-2. Special Impedance Requirements

SIGNAL TYPE	SIGNALS	IMPEDANCE (Ω)
Digital receiver differential pairs	HDMI_Dn0 and HDMI_Dp0	100 ±10% differential across each pair
	HDMI_Dn1 and HDMI_Dp1	
	HDMI_Dn2 and HDMI_Dp2	
	HDMI_CKn and HDMI_CKp	

Copyright © 2010–2012, Texas Instruments Incorporated

Table 10-2. Special Impedance Requirements (continued)

SIGNAL TYPE	SIGNALS	IMPEDANCE (Ω)
A channel LVDS differential pairs	(DMD_DAT_ANn, DMD_DAT_APn) n= 1, 3, 5...15	100 ±10% differential across each pair
	DMD_CLK_AN, DMD_CLK_AB	
	DMD_SCTRL_AN, DMD_SCTRL_AP	
B channel LVDS differential pairs	(DMD_DAT_BNn, DMD_DAT_BPn) n= 1, 3, 5...15	100 ±10% differential across each pair
	DMD_SCTRL_BN, DMD_SCTRL_BP	
	DMD_CLK_BN, DMD_CLK_BP	
DDR2 interface differential clocks (SDRAM)	DDR_CLKn0, DDR_CLKp0	100 ±10% differential across each pair
	DDR_CLKn1, DDR_CLKp1	
	DDR_CLKn2, DDR_CLKp2	
	DDR_CLKn3, DDR_CLKp3	

10.2.2 Trace Width and Trace Spacing

10.2.2.1 General Design Rules for Trace Width and Spacing

- For reference, 1 mil = 0.001 inch (0.0254 mm)
- Unless otherwise specified, all signals should follow the 0.005-inch/0.005-inch (0.127-mm/0.127-mm) design rule. Minimum trace clearance from the ground ring around the PCB should be 0.1 inch (2.54 mm) minimum. Actual trace widths and clearances should be determined based on an analysis of impedance and stack-up requirements as listed in the preceding sections.
- Routing for the DDR2 (SDRAM) termination signals may use the top and bottom layers in addition to the inner layers to accomplish a maximum trace length of 0.5 inch (12.2 mm).
- Clock trace should be separated from other signals by a minimum of 20 mils (0.508 mm).
- Escape routing (two traces between vias) for the DDR2 and DLPC200 components should be routed with a minimum 4-mil (0.102-mm) trace width and 4-mil (0.102-mm) space, and then expand to a minimum of 5-mil (0.127-mm) width and 5-mil (0.127-mm) space at nearest opportunity.
- Vias for the DLPC200 and DDR2 (SDRAM) should be sized to 9 mils (0.229 mm) with a pad size of 19 mils (0.483 mm). After the signals escape the package vias, the trace width should be widened to achieve the desired impedance and spacing.

10.2.2.2 Special Design Rules for Trace Width and Spacing

The width of all voltage signals should be maximized as space permits. In particular, width and spacing requirements should be observed for the specific signals listed in Table 10-3.

Table 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH [Mils (mm)]	MINIMUM TRACE SPACING [Mils (mm)]	LAYOUT REQUIREMENT
GND	Maximize	5 (0.127)	Maximize trace width to connecting pin as a minimum.
P3P3V	400 (10.2)	10 (0.254)	Create mini plane on layer 5. Connect to devices on layers 1 and 10 as necessary with multiple vias.
P12V	70 (1.78)	15 (0.381)	Create mini plane on layer 5. Connect to devices on layers 1 and 10 as necessary with multiple vias.
P5V	50 (1.27)	10 (0.254)	Create mini plane on layer 5. Connect to devices on layers 1 and 10 as necessary with multiple vias.
P1P8V	50 (1.27)	10 (0.254)	Create mini plane on layer 5. Connect both with multiple vias.
P1P5V	50 (1.27)	10 (0.254)	Create mini plane on layer 5. Connect to devices on layers 1 and 10 as necessary with multiple vias.
P1P2V	50 (1.27)	10 (0.254)	Create mini plane on layer 5. Connect both with multiple vias.

Copyright © 2010–2012, Texas Instruments Incorporated

Table 10-3. Special Trace Widths, Spacing Requirements (continued)

SIGNAL NAME	MINIMUM TRACE WIDTH [Mils (mm)]	MINIMUM TRACE SPACING [Mils (mm)]	LAYOUT REQUIREMENT
P2P5V	50 (1.27)	10 (0.254)	Create mini plane on layer 10.
P3P3V, P5V, P2P5V, P12V, P1P8V, P1P5V, P1P2V	30 (0.762)	10 (0.254)	Stub width to connecting IC pins. Maximize width when possible.
DDR2_VREF	200 (5.08)	30 (0.762)	
VRST, VBIAS, VCC2	20 (0.508)	10 (0.254)	
VRESET_SWL, VBIAS_SWL , VBIAS_LHI	20 (0.508)	10 (0.254)	
MBRST[15:0]	10 (0.254)	10 (0.254)	
DDR_CLKn(0:3), DDR_CLKp(0:3)		30 (0.762)	Note: Clock for DDR2 (SDRAM)
External clocks		30 (0.762)	
LVDS pairs			See Section 11.5.2

10.2.3 Device Placement

Component locations can be optimized to improve routability. The majority of large surface-mount components should be placed with thermal (cooling) considerations.

- Component distance from board edge should be a minimum of 0.100 inch (2.54 mm).
- Component distance from mounting holes should be a minimum of 0.100 inch (2.54 mm).
- Decoupling capacitors placed to minimize the distance from the decoupling capacitor to the supply and ground pins of the component. In the case where an IC has multiple decoupling capacitors with different values, alternate the values of those that are side-by-side as much as possible and place the smaller value capacitor closer to the device pin.

Copyright © 2010–2012, Texas Instruments Incorporated

11 PCB Electrical Specifications

This section outlines the electrical specifications for the PCB.

11.1 Power Planes

Signal routing should not be allowed on power planes. The power planes (layers 4 and 5) should clear the edge of the PCB by 0.1inch (2.54 mm).

11.1.1 Ground Rings

Place ground-ring traces around the perimeter of the PCB on all layers. The width of each trace should be 0.025 inch (0.635 mm) wide, minimum. Prior to routing, vias connecting all digital ground layers (GND) and the ground rings should be placed around the edge of the rigid PCB regions 0.025 inch (0.635 mm) from the board edges with a 0.100-inch (2.54-mm) spacing.

It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5 inch (12.7 mm). Extra vias are not required if there are sufficient ground vias, due to normal ground connections of devices.

All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and ground pins of each component should be connected to the power and ground planes with one via for each pin.

Trace lengths for component power and ground pins should be minimized [ideally, less than 0.100 inch (2.54 mm)]. Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground.

11.2 Mini-Planes

Some components require special mini-planes to be created under them. These are listed in Table 11-1.

Table 11-1. Mini-Planes Requirement

COMPONENT	MINI-PLANE REQUIREMENT
TFP401A	Create a mini-plane under component on layer 1 and connect to all ground planes. See the TI TFP401A data sheet for additional guidelines and information.
DDR2 (SDRAM)	See the Micron MT47H32M16 PCB layout guidelines and this layout document for MT47H32M16 guidelines.
SRAM	Form mini-planes under component on layer 1 and connect to all ground planes. See CY7C1011DV33 data sheet for information.
USB Controller	See the Cypress CY7C68013 layout guidelines.
DLPA200	Form mini-planes under component on layer 1. See DLPA200 data sheet for specific PCB layout guidelines.
DLP5500	Form mini-planes for power under component on layer 2. This is meant to separate the DLP5500 power from the rest of the board.

11.3 Placement and Routing for Decoupling Capacitors

Placement of and routing for the decoupling capacitors should meet the following guidelines. These guidelines apply for decoupling capacitors used for large high-speed components such as DDR memory, DLPC200, TFP401A, etc.

- The supply voltage pin of the capacitor should be located very close to the device supply voltage pin(s).

Copyright © 2010–2012, Texas Instruments Incorporated

- The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.05 inch (1.27 mm). Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- Decoupling capacitors for the DLPC200 and DDR2 (SDRAM) should have two vias connecting the capacitor to ground and two connecting the capacitor to the voltage. These vias should be located on opposite sides of the long side of the capacitor.
- The trace lengths of the voltage and ground connections for the capacitors should be less than 0.05 inch (1.27 mm).
- The DLPC200 and DDR2 (SDRAM) decoupling capacitors should be given placement priority.

11.4 Signal Layers

- All signal routing should be done on the layers indicated in Table 11-2.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Signal trace corners should be no sharper than 45 degrees.
- Adjacent signal layers should have the predominant traces routed orthogonal to each other.

11.5 Critical Signals and Routing Priority

In order to meet the following listed specifications, typcially the PCB designer must route these signals manually (not using automated PCB routing software). In case of length-matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long traces all around the PCB.

11.5.1 DDR2 (SDRAM) Memory Signals – Highest Priority

The DDR2 memory signals should be routed first in accordance with the specific DDR2 design guidelines provided in this document and the Micron MT47H32M16 PCB Layout Guidelines.

Table 11-2. Routing Priority

SIGNAL	ROUTING LAYERS
MEM_CLK_N(0:3), MEM_CLK_P(0:3)(1)(2)	3
MEM_A(16:0), MEM_BA(2:0), MEM_RAS, DDR2_CAS, DDR2_CS0, DDR2_WE(2)(3)	3, 7, 8
MEM_D(0:7), MEM_DM0, MEM_DS0(2)(4)	3, 4, 7, 8
MEM_D(8:15), MEM_DM1, MEM_DS1(2)(4)	3, 4, 7, 8
MEM_D(16:23), MEM_DM2, MEM_DS2(2)(4)	3, 4, 7, 8
MEM_D(24:31), MEM_DM3, MEM_DS3(2)(4)	3, 4, 7, 8
MEM_D(32:39), MEM_DM4, MEM_DS4(2)(4)	3, 4, 7, 8
MEM_D(40:47), MEM_DM5, MEM_DS5(2)(4)	3, 4, 7, 8
MEM_D(48:55), MEM_DM6, MEM_DS6(2)(4)	3, 4, 7, 8
MEM_D(56:63), MEM_DM7, MEM_DS7(2)(4)	3, 4, 7, 8

(1) The P and N signals of the DDR2 differential clock pair should be routed with 100-Ω differential impedance. The trace lengths of the P and N signals should be matched to 12 mils (0.305 mm). Routing should be from the DLPC200 to the DDR2 memory and then to the termination resistor.
(2) Switching routing layers is not permitted accept at the beginning and end of the trace.
(3) Trace lengths between the DLPC200 and the DDR2 memory should be matched relative to the MEM_CLK differential pair associated with each SDRAM device within ±75 mils (±1.91 mm).
(4) Trace lengths between the DLPC200 and the DDR2 memory should be matched relative to the MEM_DS(0:7) for each device within ±75 mils (±1.91 mm).

Copyright © 2010–2012, Texas Instruments Incorporated

11.5.2 Routing Constraints for Differential/LVDS/TMDS Signals – Next Highest Priority

The differential pairs/LVDS/TMDS signals should be routed next and are listed in Table 11-3.

Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as specified in “Special Impedance Requirements table”) is maintained throughout the routed trace.

Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another should be at least 2 times the distance between traces within a given pair.

Table 11-3. Differential Signals Routing Constraints

SIGNAL	CONSTRAINTS	ROUTING LAYERS
HDMI_Dn0 and HDMI_Dp0 HDMI_Dn1 and HDMI_Dp1 HDMI_Dn2 and HDMI_Dp2 HDMI_CKn and HDMI_CKp	Match length of all four pairs to within 0.02 inch (20 mils) (0.508 mm) and within a pair the trace length tolerance is 0.005 inch (5 mils) (0.127 mm).	7 and 8
(DMD_DAT_ANn, DMD_DAT_Apn) n = 1, 3, 5..15 DMD_CLK_AN, DMD_CLK_AB, DMD_SCTRL_AN, DMD_SCTRL_AP (DMD_DAT_BNn, DMD_DAT_BPn) n = 1, 3, 5..15 DMD_CLK_BN, DMD_CLK_BP DMD_SCTRL_AN, DMD_SCTRL_AP	Differential pair spacing: In ball field: 4-mil (0.102 mm) line, 4-mil (0.102 mm) space PCB etch: 4-mil (0.102 mm) line, 14-mil (0.102 mm) space Pair-to-pair spacing: Data: 20-mil (0.508-mm) min. space to other signals. Clock: 20-mil (0.508-mm) min. space to other signals Length mismatch: P-to-N data: <10 mils (<0.254 mm) P-to-N clock: <10 mils (<0.254 mm) Pair-to-pair (within a bundle): <10 mils (<0.254 mm) Bundle-to-bundle: <2000 mils (<5.08 mm) DMD_SCRTL_* to DMD_CLK_*(1) <150 mils (<3.81 mm) Trace length matching should include the package trace length of the DMD package. See DLPS013 for specific package trace lengths. Differential pair maximum trace length should not exceed 6 inches (15.2 cm) (total etch length between the DLPC200 and DLP5500).	7 and 8

(1) Asterisks represent various DMD_SCTRL and DMD_CLK signals.

11.5.3 Timing Critical Signals

The following signals should be routed next in priority, and should follow the specifications outlined in Table 11-4.

Table 11-4. Timing Critical Signals(1)

GROUP	SIGNAL	CONSTRAINTS	ROUTING LAYERS(2)
1	Port1_D[23:0] PORT1_HSYNC PORT1_VSYNC PORT1_CLK PORT1_IVALID PORT1_SYNC_OUT PORT1_TRIG_IN Port2_D[23:0] PORT2_HSYNC PORT2_VSYNC PORT2_CLK PORT2_IVALID PORT2_SYNC_OUT PORT2_TRIG_IN	Matched to 0.05 inch (50 mils) (1.27 mm)	2, 5
3	RST_STROBE RST_MODE(0:1) RST_A(0:3) RST_SEL(0:1) $\overline{\text{RST_IRQ}}$ $\overline{\text{RST_OE}}$ $\overline{\text{RST_RST}}$	Matched to 0.05 inch (50 mils) (1.27 mm) between DLPC200 and DLPA200	
4	MBRST(0:15]	Matched to 0.05 inch (50 mils) (1.27 mm) between DLPA200 and DLP5500	Avoid layer switching when routing these signals.
7	FLASH_SRAM_D(0:15) FLASH_SRAM_A(0:26)	Matched to 0.05 inch (50 mils) (1.27 mm)	Avoid layer switching when routing these signals.
	$\overline{\text{FLASH_CE}}$ $\overline{\text{FLASH_SRAM_OE}}$ $\overline{\text{FLASH_SRAM_RST}}$ $\overline{\text{FLASH_SRAM_WE}}$ FLASH_SRAM_RDY $\overline{\text{SRAM_CE}}$ $\overline{\text{SRAM_LB}}$ $\overline{\text{SRAM_UB}}$	Matched to 0.1 inch (100 mils) (2.54 mm)	Avoid layer switching when routing these signals.

(1) Signals should have minimum spacing of 0.02 inch (20 mils) (0.51 mm)
(2) Trace length on Layers 1 and 10 must be less than 0.5 inch (12.7 mm).

Copyright © 2010–2012, Texas Instruments Incorporated

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2010) to Revision A	Page
• Changed PCB layer stack-up text	2
• Changed PCB layer stack-up text	48
• Changed language for escape routing	49
• Changed to reflect new PCB layer stack-up	49
• Deleted comment for thermal reliefs	51
• Changed reference from Silicon Image to TI	51
• Added that guidelines apply to large high-speed components	51
• Changed table to reflect new PCB layer stack-up	52
• Changed table to reflect new PCB layer stack-up	53

Changes from Revision A (December 2010) to Revision B	Page
• Changed Warning to Caution	15
• Changed RESET signal in Power-Up Procedure figure	15
• Changed Warning to Caution	16
• Added a note to PORT1_HPD signal	23
• Added metric equivalents to inch dimensions	49
• Changed referenced table name to "Special Impedance Requirements Table"	53
• Added note to Differential Signals Routing Constraints	53

Copyright © 2010–2012, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated