Application Report
DLPA089–May 2018

DLPC34xx General System Design Guide Application Note

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ABSTRACT

This application note serves as an additional resource to introduce general design guidelines for DLP Pico™ products in addition to the detailed design information found in each DLP® chip's datasheet. A system designer should reference this application note when designing a DLP Pico display system using the DLPC34xx display controller.

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1 System Overview

1.1 System Block Diagram

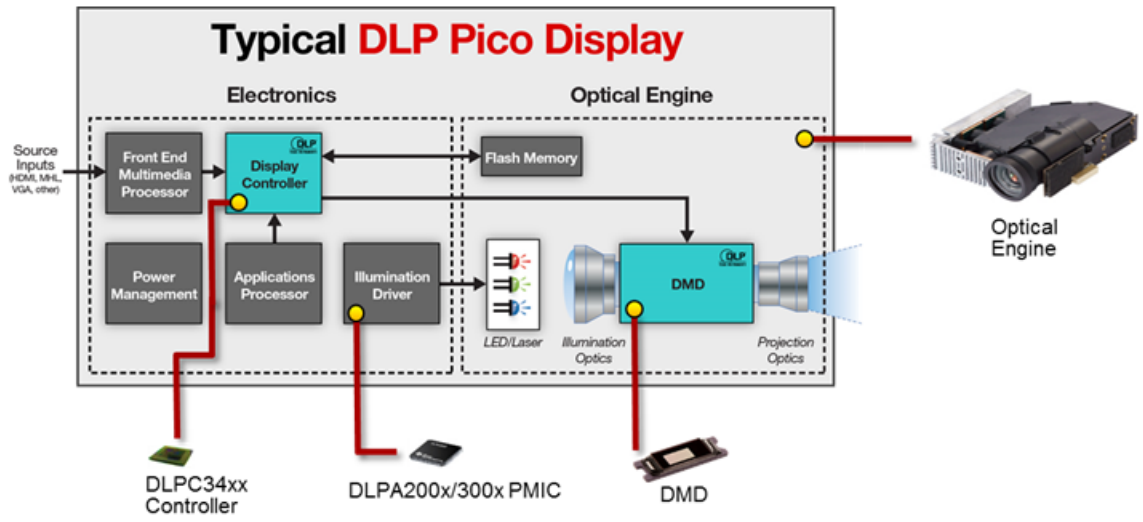

Figure 1. Typical DLP Pico System Block Diagram

Figure 1 shows a typical system block diagram of a DLP Pico display system, which has an optical engine and an electronic board. Various optical engine manufacturers in the DLP Pico supply chain provide a choice of optical engines with different DMD resolutions. The optical engine typically includes a DMD, illumination LEDs, a projection lens, and flash memory. The flash memory stores the color calibration data and the operating software for the Arm CPU inside the DLPC34xx controller. The DLPC34xx controller and the DLPA200x or DLPA300x PMIC are placed on the electronic board along with other system chips. These additional chips are added based on the product's intended application. The electronic board connects to the optical engine through a board-to-board connector, or a flex board for the bi-directional SPI flash memory and DMD interface.

NOTE: It is extremely important to consider the cooling design of the complete projection system, especially the heat dissipation of the LED illuminator. Contact the optical engine provider for thermal design guidelines and suggestions.

For proper system operation, the DLP Pico chipset has three chips: The DLPC34xx, the PMIC, and the DMD. All chips must be integrated into one system. The DLPC34xx and the PMIC are typically purchased directly from TI or one of TI's authorized distributors. The DMD typically is supplied with the optical engine. The product configuration is shown in Table 1 below.

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Table 1. Product Configuration of DLPC34xx Chipset

DLP Pico	DMD Resolution	Controller	PMIC/LED Driver
DLP2010 (0.2" WVGA)	854 × 480	DLPC3430, DLPC3435	DLPA2000, DLPA2005, DLPA3000
DLP3010 (0.3" 720p)	1280 × 720	DLPC3433, DLPC3438	DLPA2000, DLPA2005, DLPA3000, DLPA3005
DLP3310 (0.33" 1080p)	1920 × 1080	Two DLPC3437	DLPA3000, DLPA3005
DLP4710 (0.47" 1080p)	1920 × 1080	Two DLPC3439	DLPA3000, DLPA3005

1.2 Schematic and PCB Design

All reference designs for DLPDLCR2010EVM, DLPDLCR3010EVM, and DLPDLCR4710EVM are available on the TI website. These related documents include schematics, PCB layout files, bill of materials (BOMs), and test reports. Guidelines for PCB layout are provided in PCB Design Requirements for TI DLP Pico DMDs and the DLPC34xx datasheets.

2 System Power

2.1 System Power Block Diagram

The DLPC34xx chipset has four PMIC options. The DLPA2000 and DLPA2005 can drive maximum LED current values of 0.75 A and 2.4 A, respectively. The PMIC chips require additional external LDOs to support the power demands of the whole system, as shown in Figure 2. A red dot represents the source of the voltage supply. V_{INTF} can be 1.8 V, 2.5 V, or 3.3 V for a 24-bit parallel RGB interface. I^2C bus 0 can be driven by the DLPA200x load switch if it is 1.8 V. V_{FLSH} can be 1.8 V, 2.5 V, or 3.3 V for SPI flash. SPI flash can be driven by the DLPA200x load switch if it is 1.8 V. To avoid current overload, the DLPA200x load switch should not be used to drive any other device other than the DLPC34xx, DMD, and flash memory.

The DLPA3000 and DLPA3005 chips can drive maximum LED current values of 6 A and 16 A, respectively. Both chips integrate more power supply capabilities, as shown in Figure 3. A red dot represents the source of the voltage supply. V_{FLSH} can be 1.8 V, 2.5 V, or 3.3 V for SPI flash (SPI bus 0). V^{INTF} can be 1.8 V, 2.5 V, or 3.3 V for a parallel 24 bit data bus. I^2C bus 0 voltage also can be supplied by the DLPA3000/5.

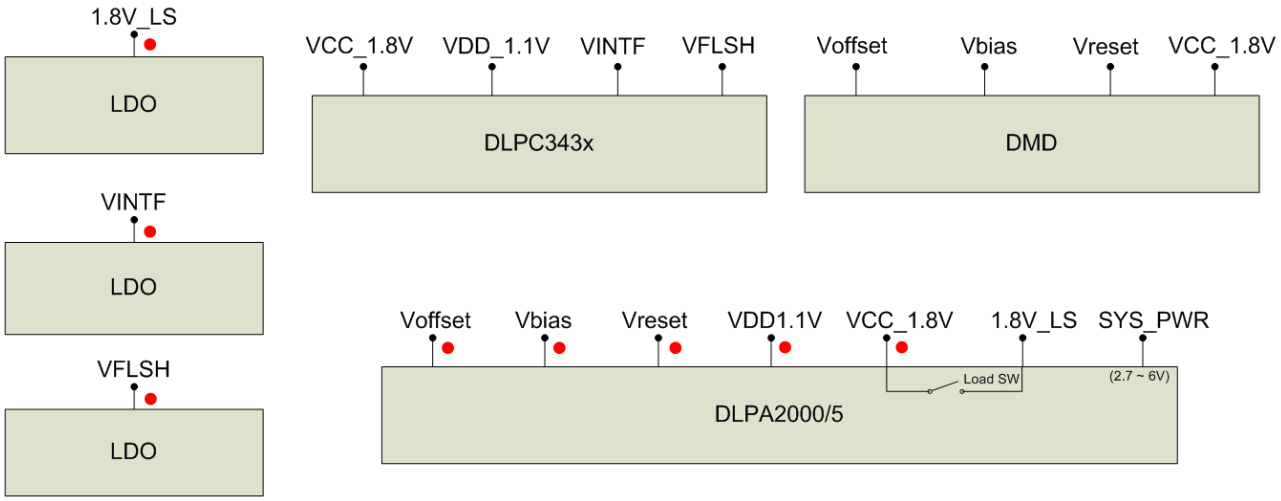

Figure 2. System Power Block With DLPA2000/5

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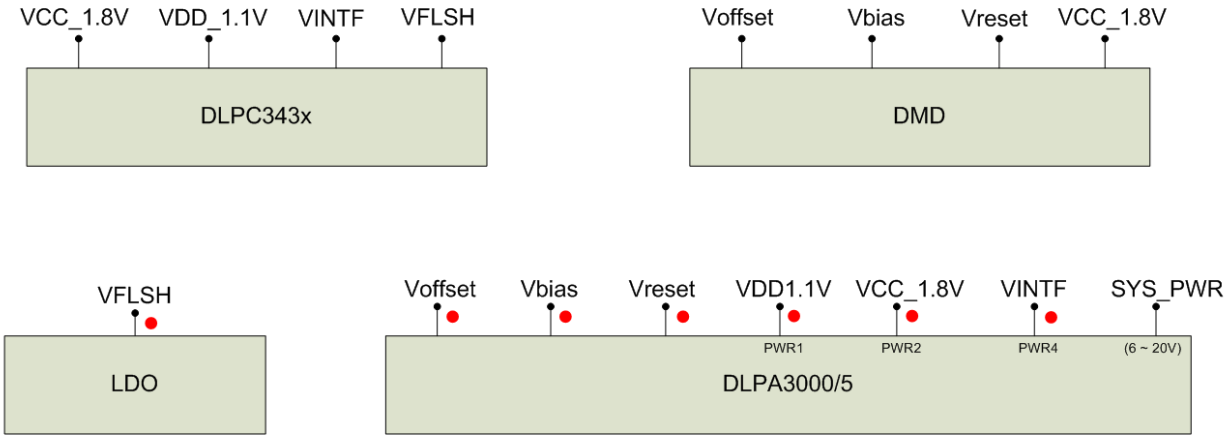

Figure 3. System Power Block With DLPA3000/5

2.2 System Power On/Off Sequence

A typical system requires a digital micromirror device (DMD), a DLPC34xx, and a PMIC. Each chip has its own power on and power off sequence specified separately in its datasheet. Figure 4 shows the critical signals that need to be monitored during system power on/off events. Figure 5 and Figure 6 give an integrated view of the critical signals shown in Figure 4 during the power on/off sequence of the DLPC34xx, PMIC, and DMD. The order of each signal is critical to ensure correct system operation. Failure to follow the guidelines provided can cause latent as well as permanent damage to the DMD.

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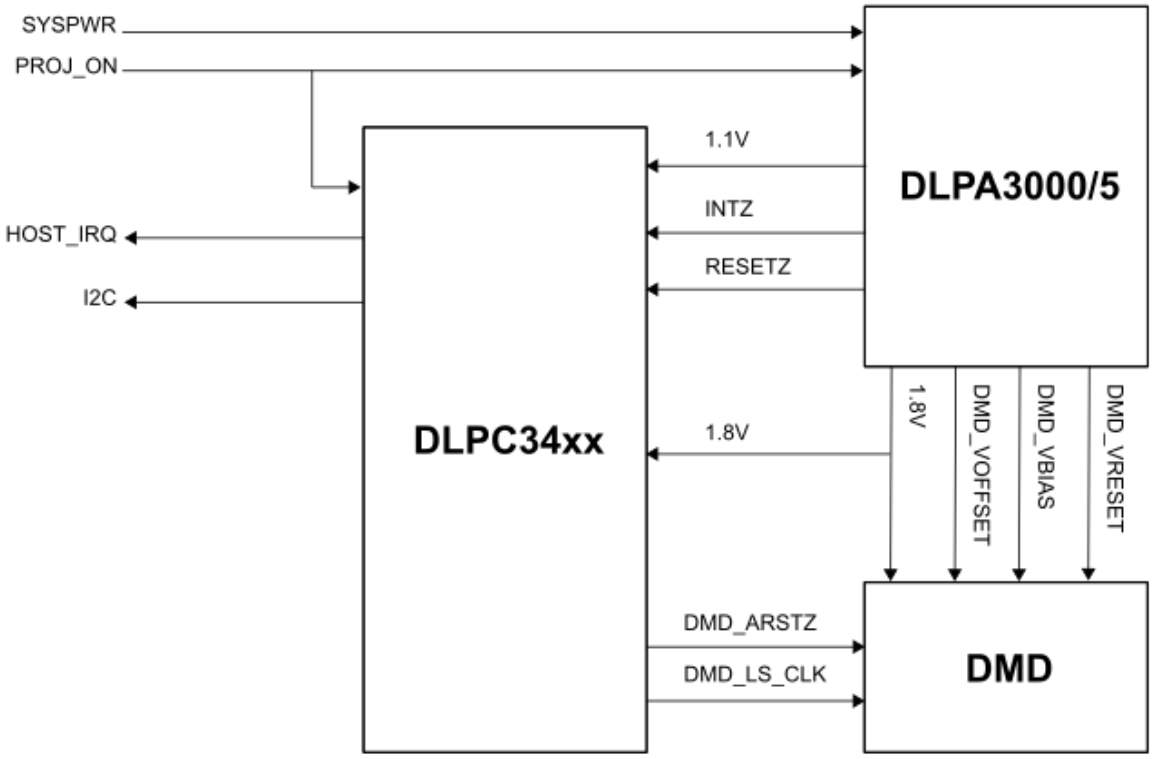

Figure 4. Critical Signals in DLPC34xx System

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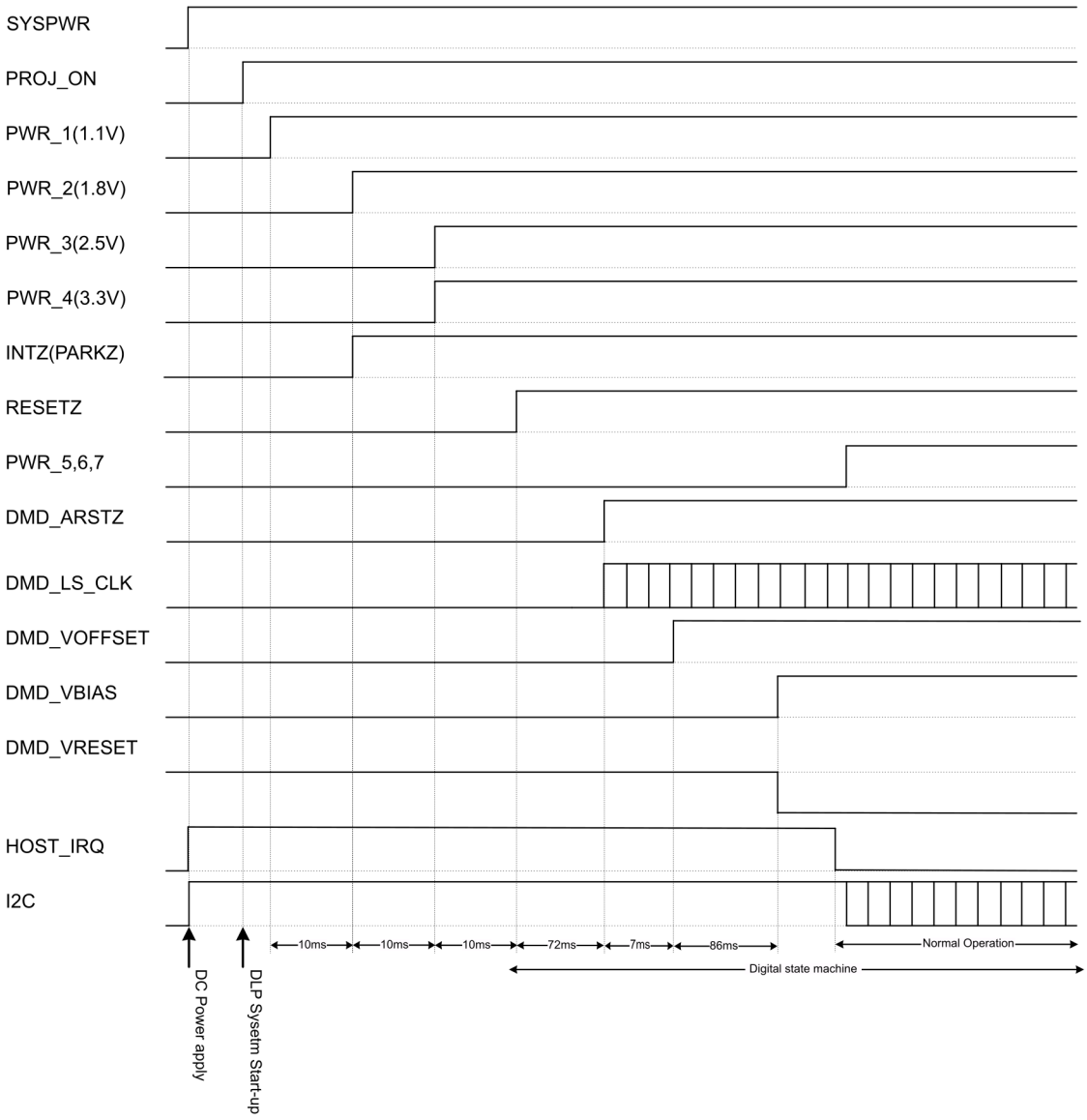

Figure 5. Normal System Power On Sequence With DLPA3000/5

NOTE: The exact times indicated in Figure 5 may vary depending on the DLPC34xx software chosen.

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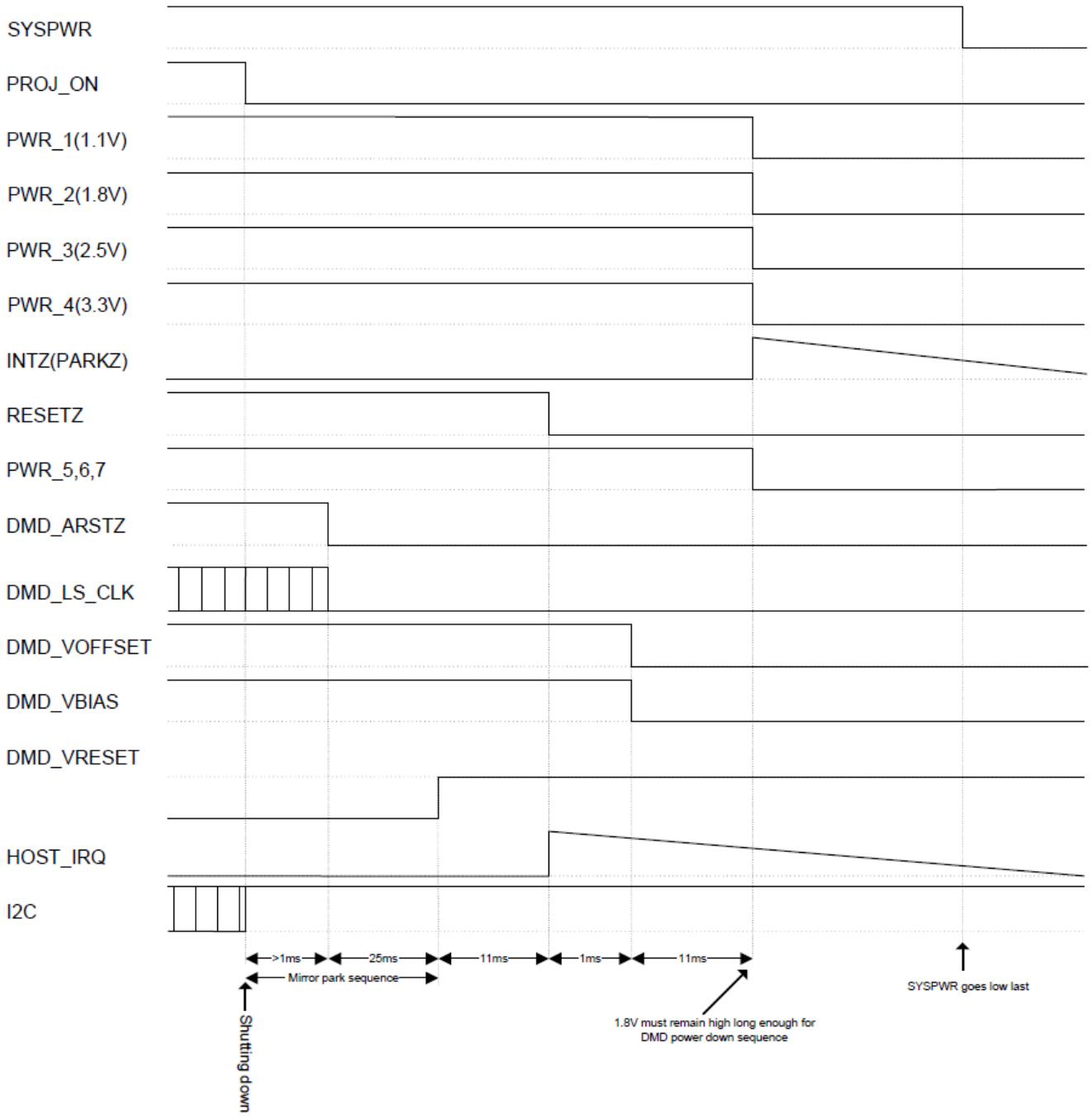

Figure 6. Normal System Power Off Sequence With DLPA3000/5

NOTE: The exact times indicated in Figure 6 may vary depending on the specific DLPC34xx software

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3 System Control

The DLPC34xx display controller is generally accessed via the I^2C bus interface. The smaller 7-mm × 7–mm package controllers (DLPC3430 and DLPC3433) offer additional system control via the DSI interface. The I^2C bus speed is fixed at 100 kHz. The I^2C bus pull-high voltage is determined by V_{INTF} which can be 1.8 V, 2.5 V, or 3.3 V. The default DLPC34xx I^2C device address is 0x36 (can be optionally set to 0x3A). All I^2C read and write commands for the DLPC34xx can be found in DLPC34xx Software Programming Guide. The reference code for a TI MSP430™ MCU to control a DLPC34xx is available from the EVM tools for the DLPC2010, the DLPC3010, and the DLPC4710.

For debugging and system test uses, the DLP composer tool can be installed in a Windows-based computer. The DLP composer tool features a graphical user interface that contains all I^2C commands needed to access and control a DLPC34xx system. A DeVaSys USB-I2C board is required to interface between a computer and a DLPC34xx. The other I^2C master device needs to be removed when a DeVaSys USB-I2C board is connected. Please contact your TI representative to acquire the DLP composer. An example of the DLP composer control GUI is shown in Figure 7.

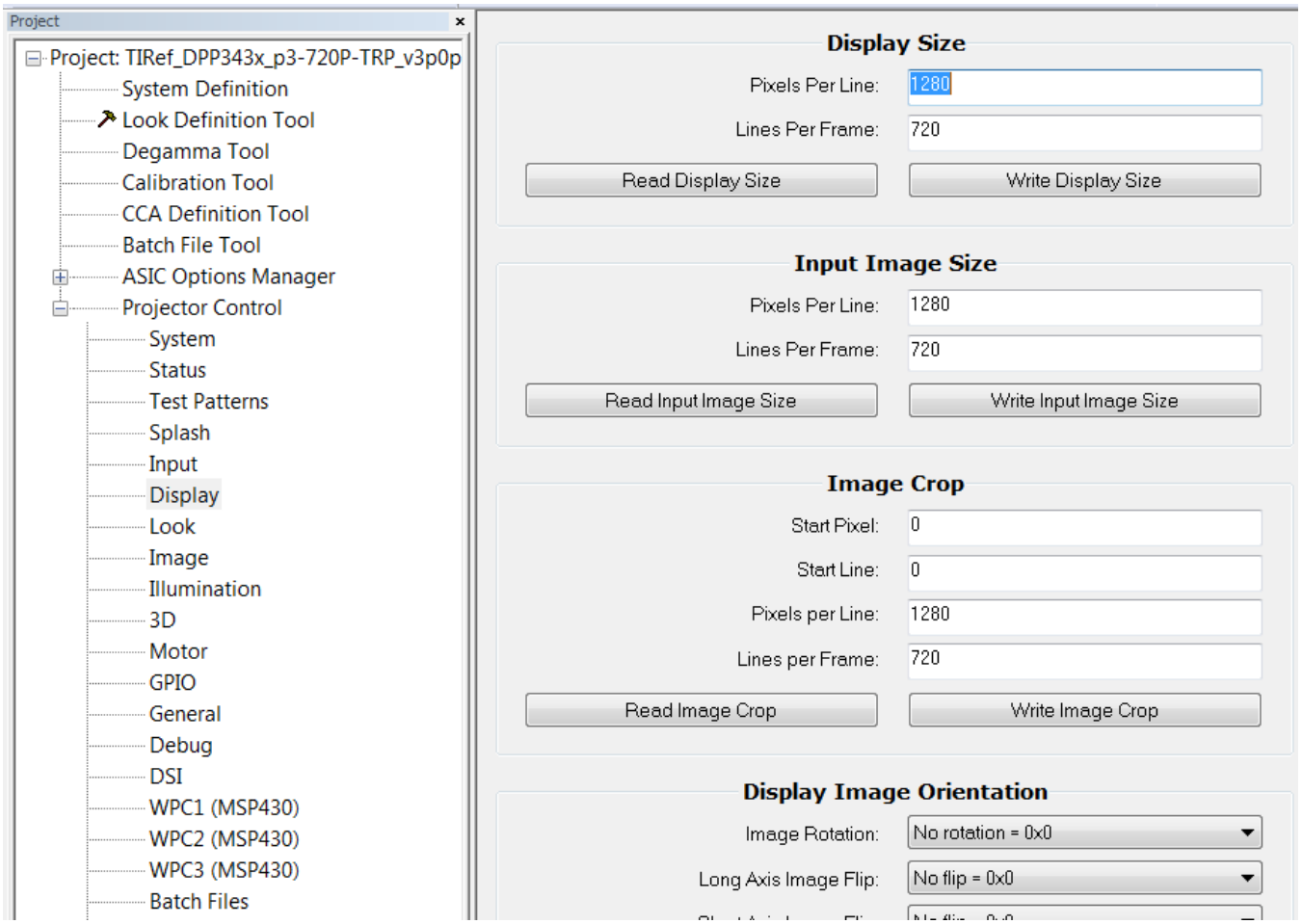

Figure 7. DLP Composer Control GUI

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4 DMD Operation Tips

4.1 Block Boundary Reset

1. DMDs have 8, 12, or 16 RESET blocks for WVGA, 720p, or 1080p resolutions, respectively.
2. RESETs (mirror state changes) occur one block at a time.
3. It is important to follow all design guidelines in order for RESETs to occur properly.
4. Failure to adhere to PCB design guidelines and published device specifications can result in RESET issues and permanent damage to the DMD.

4.2 What Can Cause Block Boundary Issues?

- Improper control of signals: ARSTZ, LS_CLK, LS_WDATA.
- Supplies ($V_{DD,}$ V_{DDI}, V_{offset}, V_{bias}, or V_{reset}) out of specification.
- Hot plugging or unplugging the DMD.
- An improper power down sequence.

4.3 How To Ensure Proper Block Boundary Resets

1. Software power-on protection:
   - The software mechanism helps protect the DMD mirrors during system power up.
   - During the power-up sequence, an attempt is made to read the DMD device ID. This command uses V_{DD} and ARSTZ.
   - A successful read indicates that a DMD is connected, and the system proceeds to turn on the remaining power supplies.
   - An unsuccessful read will not proceed to power up. This indicates that either no DMD is connected, or that a connection is bad, or that something is wrong with V_{DD}, ARSTZ, or the clock signals.
   - Power-on protection will protect DMDs from hot-plugging.
   - Power-on protection will **NOT** protect the DMD from hot-unplugging, noisy signals or grounds, open V_{DD}, ARSTZ, LS_CLK, or LS_WDATA after power up.
2. DMD signal quality:
   - All signals must be measured as close as possible to the DMD (< 5 mm). See Figure 8.
   - V_{DD} should be 1.8 V ± 0.15 V.
   - V_{DDI} should be 1.8 V ± 0.15 V.
   - V_{offset} should be 10 V ± 0.5 V.
   - V_{bias} should be 18 V ± 0.5 V.
   - V_{reset} should be –14 V ± 0.5 V
   - ARSTZ, LS_CLK, and LS_WDATA have a minimum input logic high level of 0.7 × V_{DD}. The maximum input logic high level is V_{DD} + 0.3 V, with V_{DD} = 1.8 V (typical).
   - ARSTZ, LS_CLK, and LS_WDATA have minimum input logic low level of –0.3 V. The maximum input logic low level is 0.3 × V_{DD}, with V_{DD} = 1.8 V (typical).
   - Some capacitance is needed in order to control the ripple or noise on the DMD signal and supply voltage lines.
   - The larger the DMD, the more capacitance is needed.
   - The capacitance needed for the voltage lines should be determined by experiment.
   - Avoid an improper power down sequence. V_{in} and the 1.8-V supply need to be held at least 36 ms, or longer, after PROJ_ON goes low.
   - The length of etched traces from the controller to the DMD must be ≤ 165 mm, including both PCB and FPC traces. Ground layer planes are required between the top and bottom layers of the FPC. See detailed layout and PCB considerations in PCB Design Requirements for TI DLP Pico TRP Digital Micromirror Devices.

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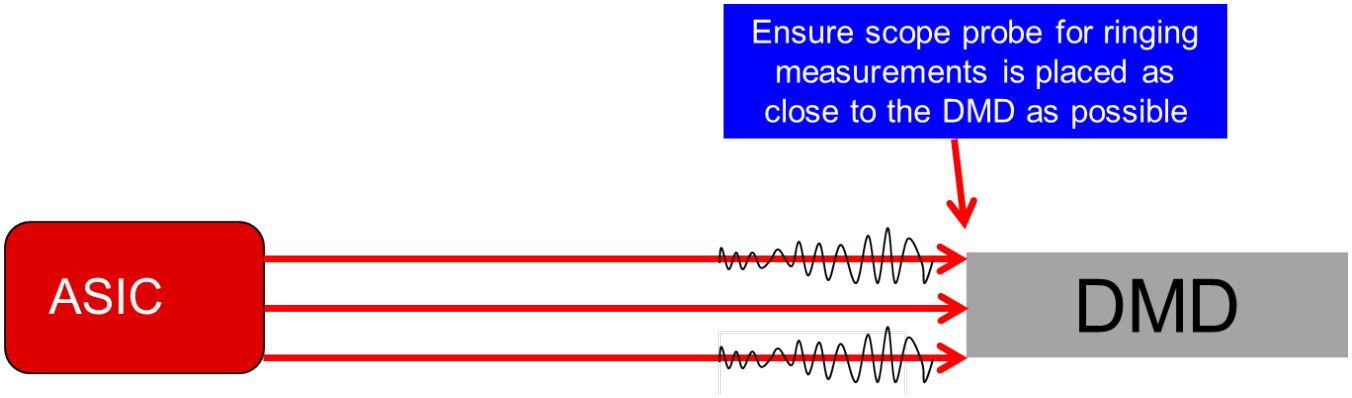

Figure 8. Measurement of DMD Signal Quality

5 System Debug Tips

Once the whole system is assembled it may require additional debugging in order to achieve proper operation. This section describes a debugging flow and presents some common design errors. Figure 9 shows the debug process from initial check out to having the external video display working properly.

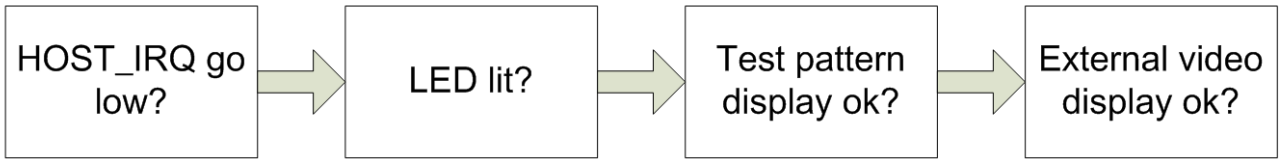

Figure 9. Debugging Flow

5.1 HOST_IRQ Goes Low

The HOST_IRQ signal is a useful indication that the embedded Arm CPU inside the DLPC34xx is booting successfully. HOST_IRQ should go low once system power is applied and PROJ_ON goes high. If not, check that the:

- DLPC3000/5 V_{IN} range is 6 to 20 V.
- Clock to DLPC34xx is 24 MHz and is at the proper signal level.
- PROJ_ON goes high (1.8 V to 3.3 V).
- The correct chips (DLPC34xx, DMD, and PMIC) are all present and properly connected. The software will check the chip IDs and the boot operation is cancelled if the chip IDs do not match.
- The LEDs are connected properly. If not, the LED open load protection will activate.
- PARKZ (INT_Z) and RESETZ are high after PROJ_ON is asserted.
- All power supply voltages are within specifications (1.1 V, 1.8 V, 2.5 V or 3.3 V).
- DLPC34xx JTAG reset has a pull-down resistor
- Ensure SPI bus 1 connection between the DLPC34xx and the PMIC is correct, and proper pull-ups are used.

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5.2 LEDs Lit

- The DLPA2000/5 and the DLPA3000/5 are designed for a common anode LED configuration.
- Check the R_{LIM} (current sense) resistor value and power dissipation rating.
- Check PARKZ (INTZ) of the DLPA2000/5 or the DLPA3000/5. A 'low' indicates a system error.
- Check that the LED enable command is set.
- Check that the LED_SEL0 and LED_SEL1 signals are being sent properly from the DLPC34xx.

5.3 Display Internal Test Pattern

- Check that the DMD routing option matches the software setting. Check the controller-to-DMD mapping options in the DLPC34xx datasheet.
- Check the I^2C bus activity.

5.4 Display External Video

- Check that the selected resolution does not exceed the maximum resolution value.

6 DLPC34xx Video Input Interface

The DLPC34xx supports an 8-bit parallel RGB interface with a pixel clock up to 150 MHz, with 120 Hz frame rates for a standard display as well as a frame sequential 3D display at the DMD's native resolution. The DLP4710 supports 120 Hz only at resolutions of 1280 × 720, 960 × 1080, or 1920 × 540. When using the parallel RGB interface at 150 MHz pixel clock, signal integrity and EMI will require attention, especially if the parallel RGB bus goes through a flex cable between PCB boards. PCB or flex cable length, impedance control, signal trace routing, and proper shielding need to be considered fully in the project design phase. An example of poor signal integrity of the pixel clock and data bus is shown in Figure 10. This could cause image quality problems. When a long flex cable has to be used, an LVDS converter is recommended to mitigate EMI and signal integrity problems.

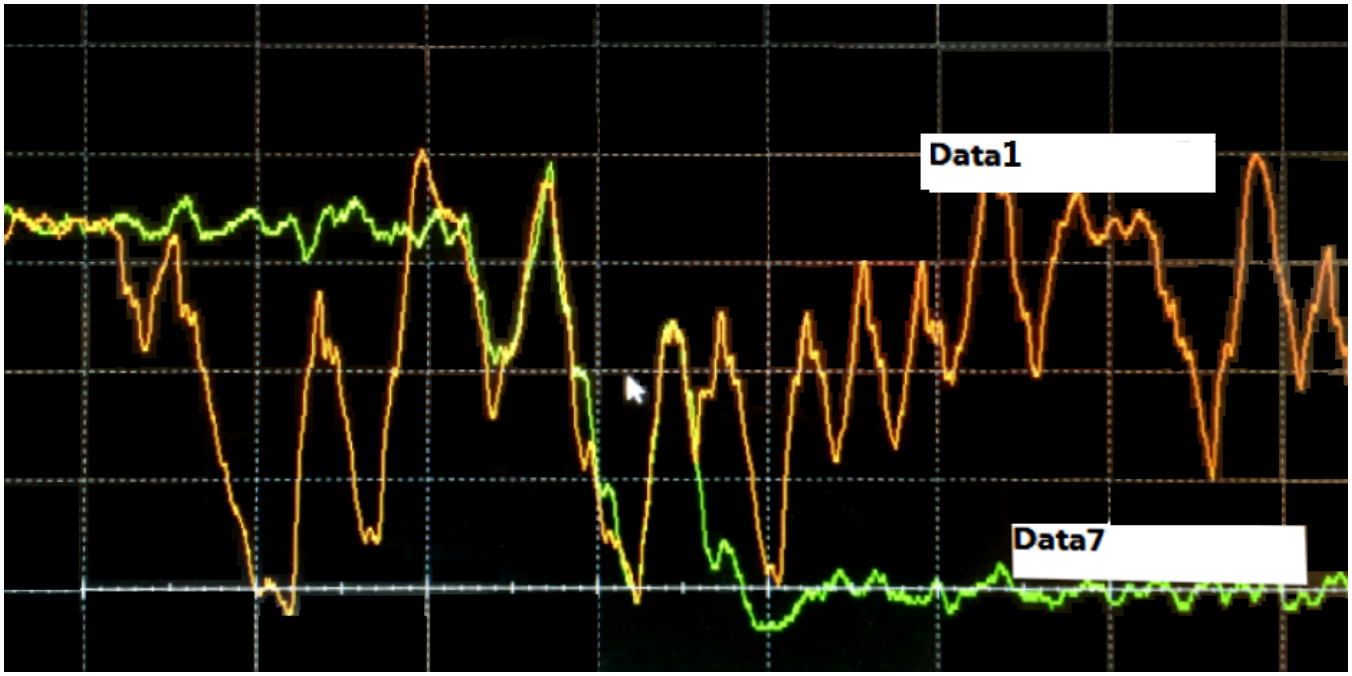

Figure 10. Data Signal Integrity Issues – Reflections, Discontinuities, and Noise

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The DPP3430/3 input interface supports the industry standard DSI type-3 video interface of up to four lanes. Please note that the DLPC3435/8/9 only support the parallel RGB interface, not the DSI interface. DSI is a source-synchronous, high speed, low power, low cost physical layer. The DSI-PHY unit is responsible for the reception of data in high speed (HS) mode, or the reception and transmission of data in low power (LP) mode for unidirectional data lanes. The high speed receiver is a differential line receiver, while the low-power receiver is unterminated and single-ended. The DLPC3430/3 supports a MIPI DSI interface type-3 up to four lanes, with 470 Mbps lane speed, and resolutions from 320 × 200 to 1280 × 800. The DLPC3430/3 GPIO_1 and GPIO_2 can be used to configure the number of DSI lanes. Pull-up and pull-down resistor can be populated on GPIO_1 and GPIO_2 to enable different lane configurations at startup, as shown in Table 2.

Table 2. DSI Lane Configurations via GPIO_01 and GPIO_02 on DLPC3430/3

GPIO_02	GPIO_01	Number of DSI Data Lanes
DSI-Lane-Config_1	DSI-Lane-Config_0	
0	0	1
0	1	2
1	0	3
1	1	4

For a DLPC3430 or DLPC3433 with MIPI DSI bus, it is recommended to closely follow the PCB layout guide:

- The differential lines of all the data and clocks must be routed to match a 50-Ω single-ended (and 100-Ω differential) impedance.
- The differential lines should be shielded on both sides by ground traces.
- The differential pair (dp/dn lines within each lane) must be tightly coupled.
- The differential pair should see identical environment (ground traces on either side and in between them).
- The lines should be far away from any other signal to minimize cross-talk.
- It is recommended to match the lengths of dp and dn.
- If an absolute match is not possible, it is recommended to have dp slightly longer than dn (delta delay not to exceed 8 to 10 ps). This is especially important for the clock lane. This is to prevent glitch propagation on the clock lane during the HS to LP transition.
- Route the differential signals on the same plane and avoid VIAs.

For the timing requirements of the DLPC3430/3, see Table 3. Match this is to the configuration done by the DSI host processor.

- For a specific product, either the DSI or the parallel RGB can be supported by the DLPC3430/3, but not both at the same time.
- The DLPC3430/3 does not support the DSI or RGB switch in real time because there is a handshaking process between the DSI host processor and the DLPC3430/3. To successfully complete this handshaking process, the DLPC3430/3 controller has to be up and running and set up for the DSI before the DSI host processor is running. In case the DSI host processor is already running and the controller is still booting the controller will miss the handshaking and the DSI will not work.
- The DLPC3430/3 supports the MIPI DSI video transfer only, but does not support DSI commands. The DLPC3430/3 display configurations, such as input source, input resolution, input crop, and display resolution, need to be set by the I^2C bus from the DSI host processor.
- For a given frame rate, the DSI high-speed (HS) clock frequency must be fixed. If a different DSI clock rate is ever needed to support another frame rate or resolution, an I^2C command "Write DSI Parameters (BDh)" will be required.
- Bus turn around is not supported, so BTA must be disabled from the DSI host processor.
- Timing requirements of the DLPC3430/3 are shown in Table 3. This must be matched to the configuration done by the DSI host processor.

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Table 3. MIPI-DSI Timing Requirement on DLPC3430/3

			MIN	MAX	UNIT
Supported Frequency Lane	Clock lane		80	235	MHz
	Data lane	Effective data rate	160	470	Mbps
	Number of data lanes	Selectable	1	4	lanes
$T_{HS-PREPARE} + T_{HS-ZERO}$	During a low power (LP) to high speed (HS) transition, the time that the transmitter drives the HS-0 state prior to transmitting the sync sequence	80-MHz to 94-MHz HS clock	565		ns
		95-MHz to 235-MHz HS clock	465		ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any data lane HS transitions, starting from the beginning of the $T_{HS-PREPARE}$. The HS receiver shall ignore any data lane transitions before the minimum value, and shall respond to any data lane transitions after the maximum value.	80-MHz to 94-MHz HS clock		565	ns
		95-MHz to 235-MHz HS clock		465	ns

7 DMD Interface Design Considerations

There are four power supplies connected to the DMD. DMD_VCC serves as the CMOS power supply and DMD_Vbias, DMD_Vreset, and DMD_Voffset are used to tilt the mirrors on the DMD. Make sure that these four power supplies are stable at the DMD. Overshoot, undershoot, ripple, and voltage ranges must meet the DMD specifications. The trace width and length for these four power supplies also need to be considered in order to ensure stability. On the TI reference design, 15 mil traces are used for routing these four power supplies. Adequate bypass capacitors should be put close to the DMD power pins. The bigger the DMD, the higher the capacitance needed. On the TI reference design, there are two 0.1-µF capacitors on DMD_VCC, and one 0.1-µF capacitor for V_{bias}, V_{reset}, and V_{offset}. As stated, the power up and power down sequence of these four power supplies must be ensured and verified on the PCB board. Violating these requirements could cause image problems, or even permanent damage to the DMD. The power up and power down sequence of the DMD power supply is shown in Figure 11.

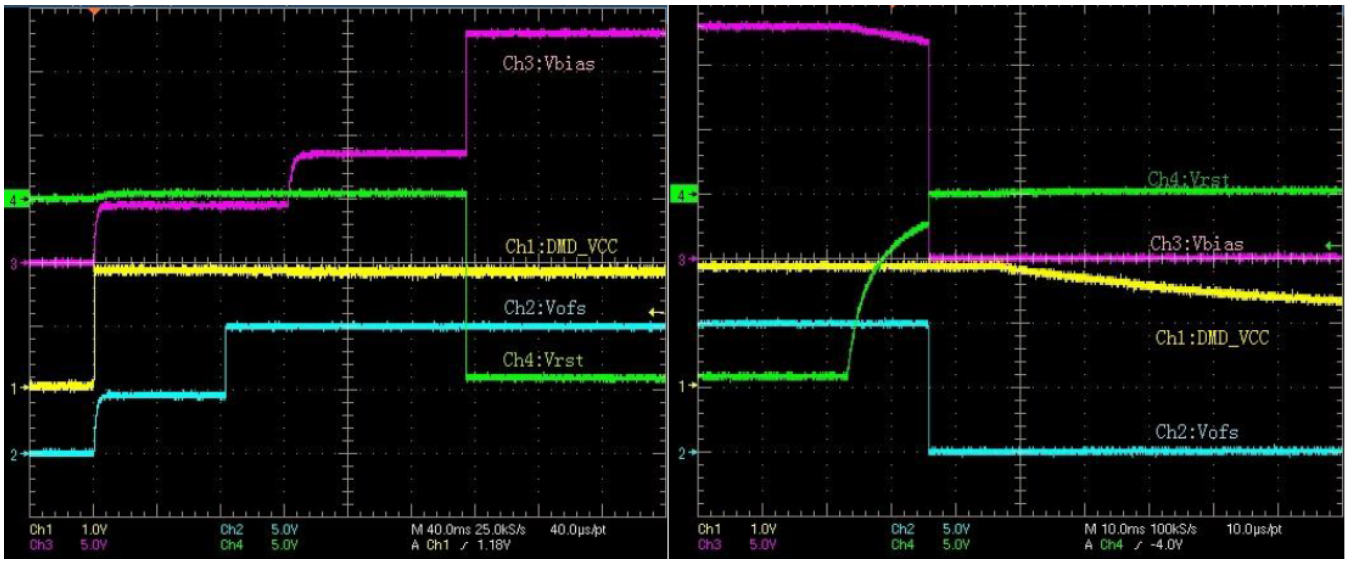

Figure 11. DMD Power On and Power Off Sequence

There are two sets of signals between the DLPC34xx and the DMD which ensure proper operation. An LVDS interface transfers video data from the DLPC34xx to the DMD at up to 600 MHz. For the DLPC2010, four pairs of data bus are used, and there are four different pin mapping options available to ease the PCB layout. For the DLP3010, DLP4710, and DLP3310, all eight pairs of data bus are used, and there are two pin mapping options to ease the PCB layout. Signal integrity must be assured by design. If a

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flex cable is used, a ground plane should be added to ensure a 100-Ω ± 10% impedance for the differential pairs of the high speed data bus. Voltage (±200 mV), rising or falling edge, and the CLK and data timing margin should be considered at the design and verification stage to prevent image quality or flickering problems at the production stage due to the tolerance of the flex cable or the PCB traces. For these high speed signals the DLPC34xx implements a bus training scheme every time at start up to optimize clock or data timing. There is an I²C register that the host processor can read. The value resulting from the training indicates how much margin exists on each specific PCB or flex cable for each clock and data pair. An example of a good training result of bus H is a high-pass DLL value of 47, and low-pass DLL value of 5. The DLPC34xx would choose a value midway between the low and high. This is a value of 26, with a margin of 21. There needs to be enough margin to ensure that the system works properly with aging of the PCB or FPC, and over the rated temperature range. This is shown in Figure 12.

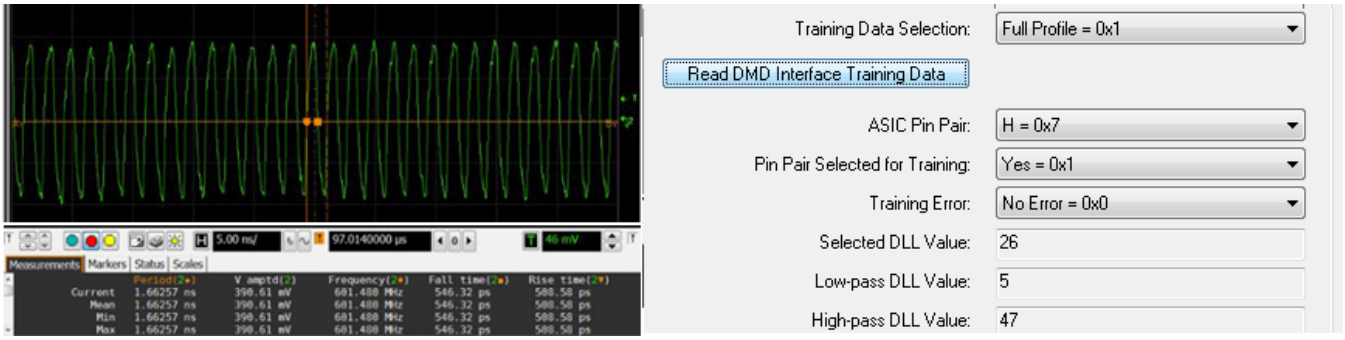

Figure 12. Good Bus Training Result Read From DLP Composer via I²C of DLPC3438

The DLPC34xx will fail the training if the high DLL-low DLL at less than 20, and the DLL is set to 25 as shown in Figure 13. This result indicates that the DMD could not sample the correct data, which results in a defective image, or a flickering problem.



Figure 13. Training Bus Fail Result Read From DLP Composer via I²C Bus of DLPC3438

The other set of signals between the DLPC34x and the DMD is the low speed bus which usually runs at 120 MHz. These signals are very critical for DMD control. PCB or flex design must be done carefully to ensure signal integrity. Voltage levels, rising and falling edges, and timing are critical. The signal trace routing length or width, the series resistor (43 Ω on the TI reference design), and trace impedances must be considered. The DMD low speed bus requires a 68-Ω ± 10% impedance. The low speed bus series resistor can be adjusted to achieve the required signal quality. Violating specifications on a low speed signal could cause image problems and flickering, or even permanent damage to the DMD, as stated in Section 4.

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8 PMIC Design Considerations

The DLPA3000 is a single channel LED driver supplying up to 6A with an internal FET and switch. It switches among three LED loads sequentially, according to the setting of LED_SEL0/1 from DLPC3438 during normal operation. The switching frequency can be 120 Hz, 240 Hz, or 480 Hz depending on the duty cycle of each LED. This high current and load switching mechanism requires attention to peripheral component selection and layout considerations to ensure stable operation.

Illumination driver chips such as Figure 14 feature LED driver circuits including peripheral components (inductors and so forth) separate from other digital power supplies for V_{core}, V_{CC}, or general purpose buck regulators in order to avoid any interference. Inductor and capacitor value should be calculated and verified to accommodate different input voltages, the output forward voltage, and the output current.

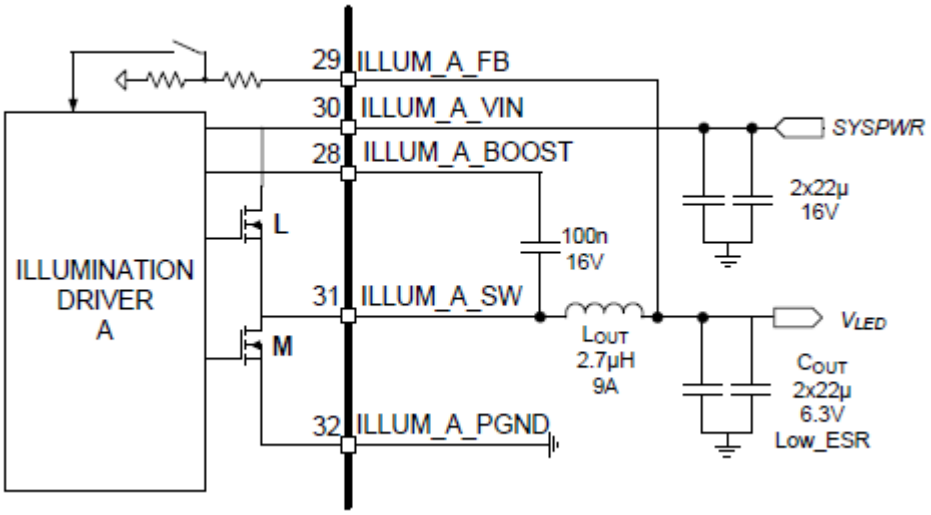

Figure 14. DLPA3000 Illumination Driver Circuits

Formulas can be used as a starting point for selecting proper inductor and capacitor values. An inductor value that is too small could cause a high reverse current, or a high overshoot on the LED_SW signal, which reduces reliability, as shown in Figure 15. The same principle applies to output capacitors which are required to achieve the desired ripple level and overshoot or undershoot level, as well as minimize the reverse current. In a normal case, 44 µF is recommended (Figure 16). This can be adjusted based on specific system requirements. For example, 22 µF should be used when selecting a 4.7-µH inductor.

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$$L_{OUT} = \frac{\frac{V_{OUT}}{V_{IN}} \cdot (V_{IN} - V_{OUT})}{k_{I_RIPPLE} \cdot I_{OUT} \cdot f_{SWITCH}}$$

Example: $V_{IN} = 12V, V_{OUT} = 4.3V, I_{OUT} = 6A$ results in an inductor value of $L_{OUT} = 4.6\mu H$

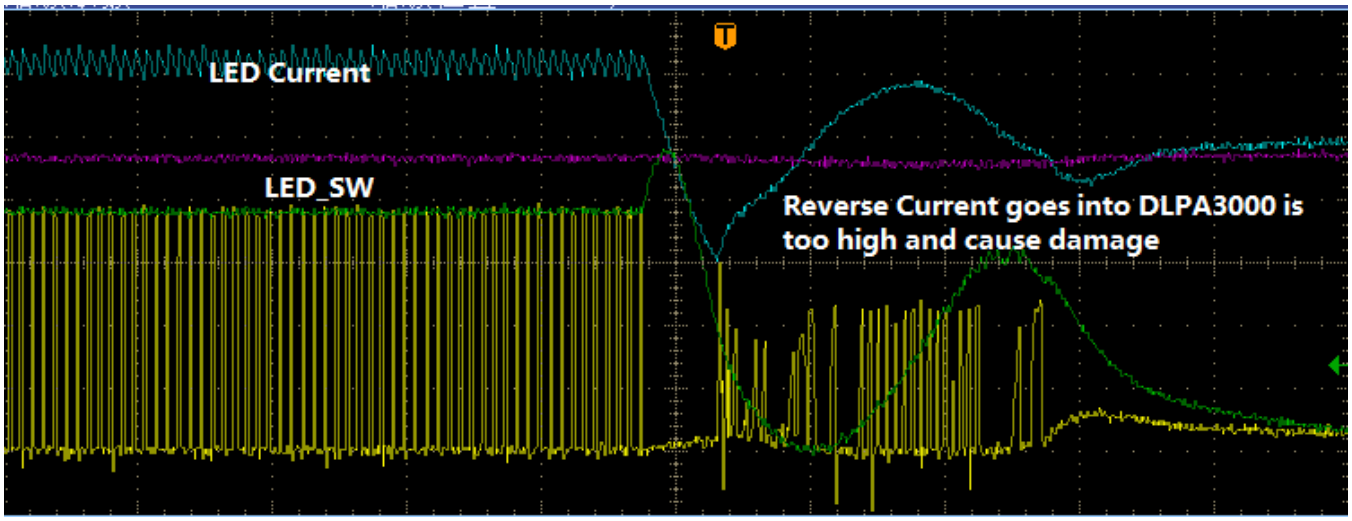

Figure 15. High Reverse Current Could Damage the Part

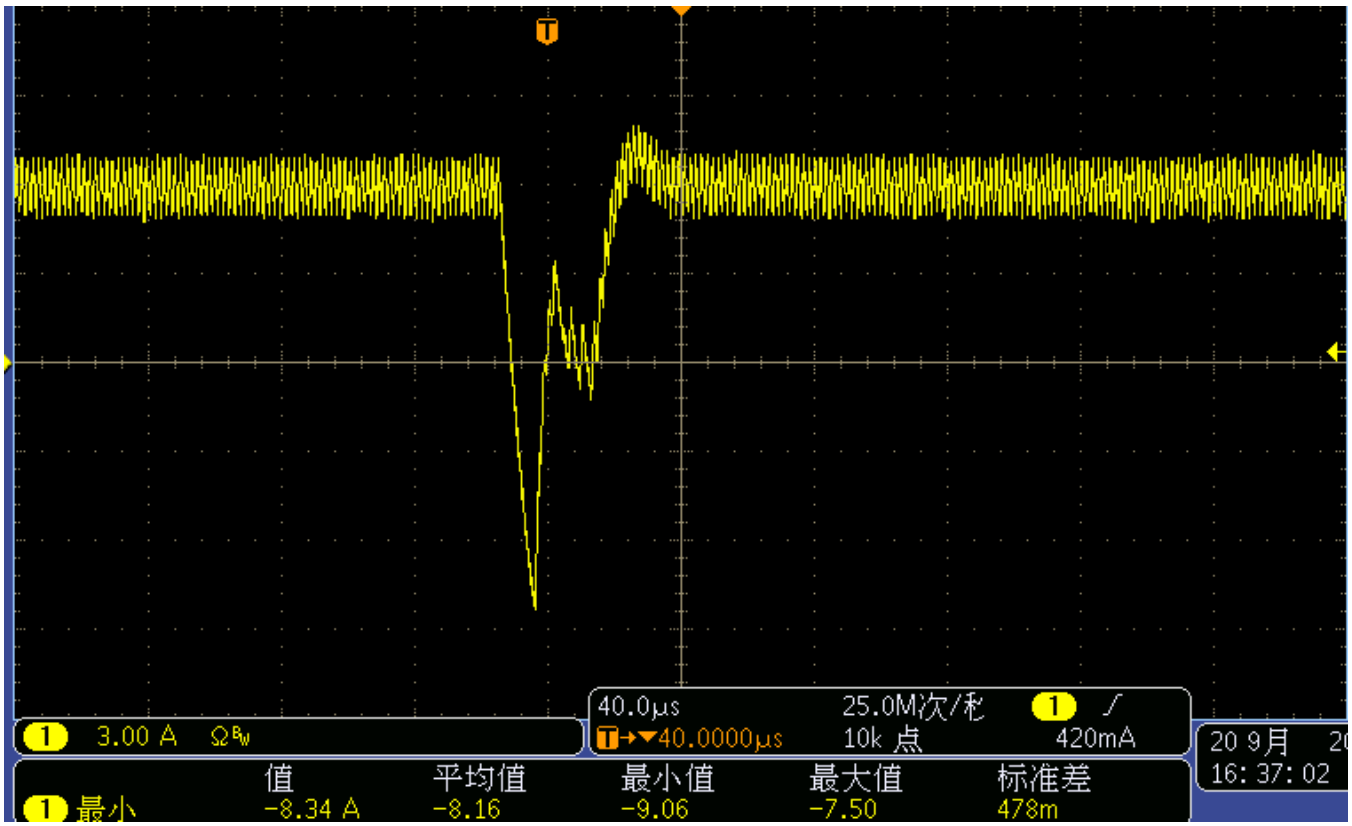

Figure 16. Reverse Current at VIN = 19 V, Inductor at 2.7 µH, and Output Capacitor at 44 µF

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The waveform in Figure 17 shows the result of changing the inductor from 2.7 µH to 4.7 µH. The reverse current is reduced from 9 A to 7 A.

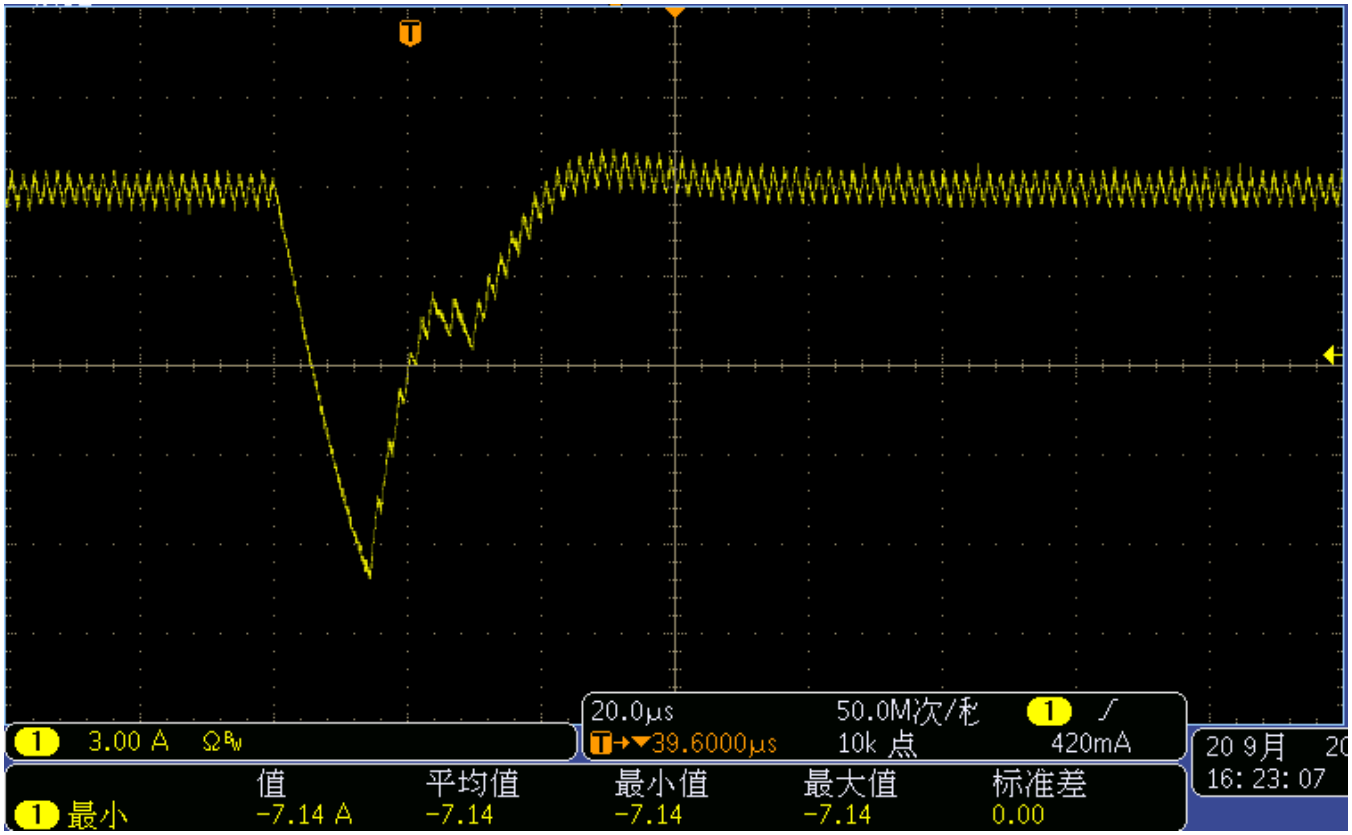

Figure 17. Reverse Current at VIN = 19 V, Inductor at 4.7 µF, and Output Capacitor at 44 µF

Due to the LED driver switching among three LED loads, during the switching transition period the control loop for the buck converter via the LED is not present. In order to prevent the output voltage of the buck converter from running away, the loop is closed by means of an internal resistive load. During this period the open-loop voltage control is active. The transition from one LED to another implies that during the BBM time all LEDs are off. The current setting for all three LEDs is 0. It is advisable to set the open-loop voltage to around the lowest LED forward voltage. The open-loop voltage can be set between 3 V and 18 V in steps of 1 V through register 0x18. This open loop voltage also affects the reverse current and should be set properly for the specific design requirements. Figure 18 shows that the reverse current is reduced to 10.2 A, 7.5 A, and 4.7 A when the open loop voltage is set to 3 V, 4 V, and 5 V, respectively.

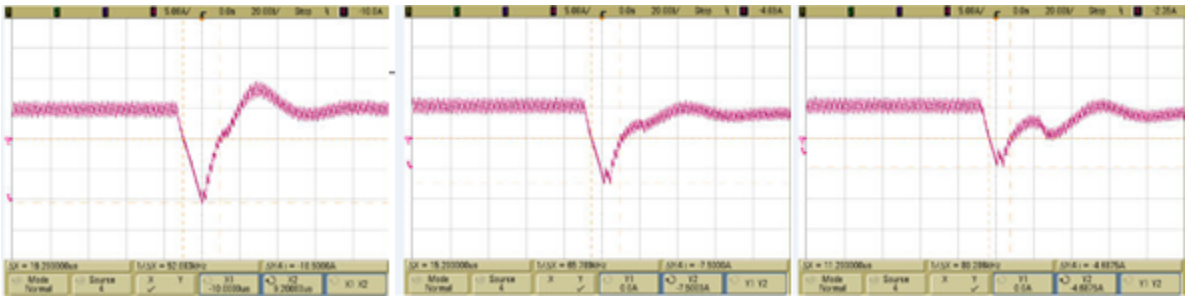

Figure 18. Reverse Current vs. Open Loop Voltage

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