DLP3310 0.33 1080p DMD

1 Features

- 0.33-Inch (8.47-mm) Diagonal Micromirror Array
  - Displays Full-HD 1920 × 1080 Pixels on the Screen
  - 5.4-µm Micromirror Pitch
  - 17° Micromirror Tilt (Relative to Flat Surface)
  - Side Illumination for Optimal Efficiency and Optical Engine Size
  - Polarization Independent Aluminum Micromirror Surface
- 32-Bit SubLVDS Input Data Bus
- Dedicated DLPC3437 Display Controller and DLPA3000 PMIC/LED Driver for Reliable Operation

2 Applications

- Mobile Smart TVs
- Screenless TVs
- Gaming Displays
- Digital Signage
- Wearable Displays
- Pico Projectors
- Interactive Displays
- Ultra Mobile Displays
- Smart Home Displays
- Virtual Assistant

3 Description

The DLP3310 digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP3310 DMD displays a very crisp and high quality image or video. DLP3310 is part of the chipset comprising of the DLP3310 DMD, DLPC3437 display controller, and DLPA3000 PMIC/LED driver. The compact physical size of the DLP3310 coupled with the controller and the PMIC/LED driver provides a complete system solution that enables small form factor, low power, and high resolution full-HD displays.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP3310	FQM (92)	19.25 mm × 7.2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

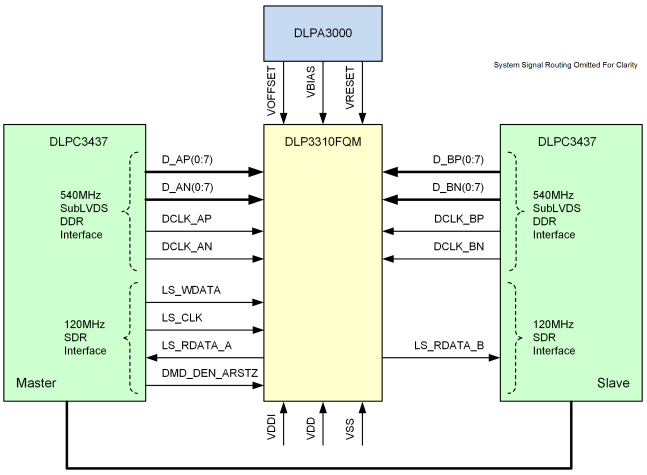


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 7
6.1 Absolute Maximum Ratings ... 7
6.2 Storage Conditions ... 7
6.3 ESD Ratings ... 8
6.4 Recommended Operating Conditions ... 8
6.5 Thermal Information ... 10
6.6 Electrical Characteristics ... 10
6.7 Timing Requirements ... 11
6.8 Switching Characteristics ... 16
6.9 System Mounting Interface Loads ... 16
6.10 Micromirror Array Physical Characteristics ... 17
6.11 Micromirror Array Optical Characteristics ... 18
6.12 Window Characteristics ... 19
6.13 Chipset Component Usage Specification ... 19
7 Detailed Description ... 20
7.1 Overview ... 20
7.2 Functional Block Diagram ... 20
7.3 Feature Description ... 21
7.4 Device Functional Modes ... 21
7.5 Optical Interface and System Image Quality Considerations ... 21
7.6 Micromirror Array Temperature Calculation ... 22
7.7 Micromirror Landed-On/Landed-Off Duty Cycle ... 23
8 Application and Implementation ... 28
8.1 Application Information ... 28
8.2 Typical Application ... 29
9 Power Supply Recommendations ... 31
9.1 Power Supply Power-Up Procedure ... 31
9.2 Power Supply Power-Down Procedure ... 31
9.3 Power Supply Sequencing Requirements ... 32
10 Layout ... 34
10.1 Layout Guidelines ... 34
10.2 Layout Example ... 34
11 Device and Documentation Support ... 35
11.1 Device Support ... 35
11.2 Related Links ... 35
11.3 Community Resources ... 35
11.4 Trademarks ... 36
11.5 Electrostatic Discharge Caution ... 36
11.6 Glossary ... 36
12 Mechanical, Packaging, and Orderable Information ... 36

4 Revision History

Changes from Revision A (January 2017) to Revision B — **Page**

- Removed the ± sign before 17° in Features ... 1
- Removed trace lengths of power supplies V_{BIAS}, V_{OFFSET}, and V_{RESET} from Pin Functions - Connector Pins ... 4
- Updated MIN values for V_{DD} and V_{DDI} from 1.7 to 1.65 in *Recommended Operating Conditions* ... 8
- ILL_{VIS} changed from TBD to Thermally Limited in *Recommended Operating Conditions* ... 9

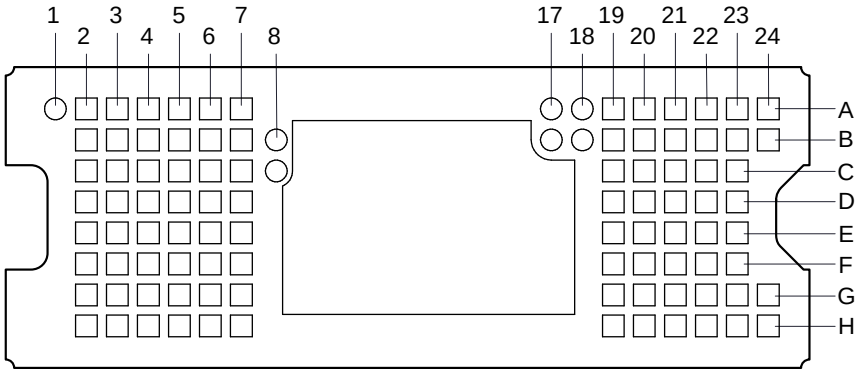
Changes from Original (June 2016) to Revision A — **Page**

- Updated list in Applications section ... 1
- ILL_{VIS} changed to TBD in *Recommended Operating Conditions* ... 9
- Changed electrical characteristics values from TBD in *Electrical Characteristics* ... 10
- Changed measured values for Capacitance under *Electrical Characteristics* ... 11
- Included mechanical load values in *System Mounting Interface Loads* ... 16

Copyright © 2016–2018, Texas Instruments Incorporated

5 Pin Configuration and Functions

FQM Package
92-Pin CLGA
Bottom View



Pin Functions – Connector Pins(1)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH(2) (mm)
NAME	NO.					
DATA INPUTS						
D_AN(0)	C6	I	SubLVDS	Double	Data, Negative	2.83
D_AN(1)	D7	I	SubLVDS	Double	Data, Negative	4.00
D_AN(2)	D5	I	SubLVDS	Double	Data, Negative	1.97
D_AN(3)	F7	I	SubLVDS	Double	Data, Negative	4.03
D_AN(4)	F5	I	SubLVDS	Double	Data, Negative	1.90
D_AN(5)	G6	I	SubLVDS	Double	Data, Negative	3.08
D_AN(6)	H5	I	SubLVDS	Double	Data, Negative	2.23
D_AN(7)	H7	I	SubLVDS	Double	Data, Negative	3.88
D_AP(0)	C5	I	SubLVDS	Double	Data, Positive	2.72
D_AP(1)	D6	I	SubLVDS	Double	Data, Positive	3.89
D_AP(2)	D4	I	SubLVDS	Double	Data, Positive	1.87
D_AP(3)	F6	I	SubLVDS	Double	Data, Positive	3.93
D_AP(4)	F4	I	SubLVDS	Double	Data, Positive	1.79
D_AP(5)	G5	I	SubLVDS	Double	Data, Positive	2.97
D_AP(6)	H4	I	SubLVDS	Double	Data, Positive	2.12
D_AP(7)	H6	I	SubLVDS	Double	Data, Positive	3.78
D_BN(0)	C20	I	SubLVDS	Double	Data, Negative	2.23
D_BN(1)	D19	I	SubLVDS	Double	Data, Negative	3.27
D_BN(2)	D21	I	SubLVDS	Double	Data, Negative	1.27
D_BN(3)	F19	I	SubLVDS	Double	Data, Negative	3.52
D_BN(4)	F21	I	SubLVDS	Double	Data, Negative	1.34
D_BN(5)	G20	I	SubLVDS	Double	Data, Negative	2.55
D_BN(6)	H21	I	SubLVDS	Double	Data, Negative	1.71
D_BN(7)	H19	I	SubLVDS	Double	Data, Negative	3.37
D_BP(0)	C21	I	SubLVDS	Double	Data, Positive	2.13

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)*. See JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQM ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 in/ns.
Propagation delay = 0.265 ns/inch = 265 ps/in = 10.43 ps/mm.

Copyright © 2016–2018, Texas Instruments Incorporated

Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
D_BP(1)	D20	I	SubLVDS	Double	Data, Positive	3.16
D_BP(2)	D22	I	SubLVDS	Double	Data, Positive	1.17
D_BP(3)	F20	I	SubLVDS	Double	Data, Positive	3.42
D_BP(4)	F22	I	SubLVDS	Double	Data, Positive	1.23
D_BP(5)	G21	I	SubLVDS	Double	Data, Positive	2.44
D_BP(6)	H22	I	SubLVDS	Double	Data, Positive	1.61
D_BP(7)	H20	I	SubLVDS	Double	Data, Positive	3.27
DCLK_AN	E6	I	SubLVDS	Double	Clock, Negative	2.56
DCLK_AP	E5	I	SubLVDS	Double	Clock, Positive	2.46
DCLK_BN	E20	I	SubLVDS	Double	Clock, Negative	2.05
DCLK_BP	E21	I	SubLVDS	Double	Clock, Positive	1.95
CONTROL INPUTS						
LS_WDATA	B3	I	LPSDR[1]	Single	Write data for low speed interface.	1.78
LS_CLK	B5	I	LPSDR	Single	Clock for low-speed interface.	1.78
DMD_DEN_ARSTZ	B2	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	0.85
LS_RDATA_A	B7	O	LPSDR	Single	Read data for low-speed interface.	4.19
LS_RDATA_B	B4	O	LPSDR	Single	Read data for low-speed interface.	2.18
POWER						
V_{BIAS}[3]	A6	Power			Supply voltage for positive bias level at micromirrors.	
V_{BIAS}[3]	A22	Power				
V_{OFFSET}[3]	B21	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.	
V_{OFFSET}[3]	G2	Power				
V_{RESET}	A5	Power			Supply voltage for negative reset level at micromirrors.	
V_{RESET}	A23	Power				
V_{DD}[3]	C2	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.	
V_{DD}	A19	Power				
V_{DD}	A20	Power				
V_{DD}	A21	Power				
V_{DD}	B20	Power				
V_{DD}	C2	Power				
V_{DD}	D2	Power				
V_{DD}	D3	Power				
V_{DD}	D23	Power				
V_{DD}	E2	Power				
V_{DD}	F2	Power				
V_{DD}	F3	Power				
V_{DD}	F23	Power				

(3) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.

Copyright © 2016–2018, Texas Instruments Incorporated

Pin Functions – Connector Pins[1] (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
NAME	NO.					
V_{DDI}	B6	Power			Supply voltage for SubLVDS receivers.	
V_{DDI}	B19	Power				
V_{DDI}	C3	Power				
V_{DDI}	C23	Power				
V_{DDI}	E3	Power				
V_{DDI}	E23	Power				
V_{DDI}	G3	Power				
V_{DDI}	G23	Power				
V_{SS}	A2	Ground			Common return. Ground for all power.	
V_{SS}	A3	Ground				
V_{SS}	A4	Ground				
V_{SS}	A7	Ground				
V_{SS}	A24	Ground				
V_{SS}	B22	Ground				
V_{SS}	B23	Ground				
V_{SS}	B24	Ground				
V_{SS}	C4	Ground				
V_{SS}	C7	Ground				
V_{SS}	C19	Ground				
V_{SS}	C22	Ground				
V_{SS}	E4	Ground				
V_{SS}	E7	Ground				
V_{SS}	E19	Ground				
V_{SS}	E22	Ground				
V_{SS}	G4	Ground				
V_{SS}	G7	Ground				
V_{SS}	G19	Ground				
V_{SS}	G22	Ground				
V_{SS}	G24	Ground				
V_{SS}	H2	Ground				
V_{SS}	H3	Ground				
V_{SS}	H23	Ground				
V_{SS}	H24	Ground				

Copyright © 2016–2018, Texas Instruments Incorporated

Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
A1	Do not connect
A17	Do not connect
A18	Do not connect
B8	Do not connect
B17	Do not connect
B18	Do not connect
C8	Do not connect

Copyright © 2016–2018, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
Supply voltage	V_{DD}	Supply voltage for LVCMOS core logic (2) Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	V_{DDI}	Supply voltage for SubLVDS receivers (2)	–0.5	2.3	V
	V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	11	V
	V_{BIAS}	Supply voltage for micromirror electrode (2)	–0.5	19	V
	V_{RESET}	Supply voltage for micromirror electrode (2)	–15	0.5	V
	$\lvert V_{DDI}–V_{DD}\rvert$	Supply voltage delta (absolute value) (4)		0.3	V
	$\lvert V_{BIAS}–V_{OFFSET}\rvert$	Supply voltage delta (absolute value) (5)		11	V
	$\lvert V_{BIAS}–V_{RESET}\rvert$	Supply voltage delta (absolute value) (6)		34	V
Input voltage	Input voltage for other inputs LPSDR (2)		–0.5	V_{DD} + 0.5	V
	Input voltage for other inputs SubLVDS (2) (7)		–0.5	V_{DDI} + 0.5	V
Input pins	$\lvert V_{ID}\rvert$	SubLVDS input differential voltage (absolute value) (7)		810	mV
	I_{ID}	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational (8)	–20	90	°C
		Temperature – non-operational (8)	–40	90	°C
	$\lvert T_{DELTA}\rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminals (V_{SS}). The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated by the *Micromirror Array Temperature Calculation*) or of any point along the window edge as defined in Figure 18. The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 18 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 18. The window test points TP2, TP3, TP4, and TP5 shown in Figure 18 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP}	Average dew point temperature (non-condensing) (1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

Copyright © 2016–2018, Texas Instruments Incorporated

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE (3)					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode (4)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\lvert V_{DDI}–V_{DD}\rvert$	Supply voltage delta (absolute value) (5)			0.3	V
$\lvert V_{BIAS}–V_{OFFSET}\rvert$	Supply voltage delta (absolute value) (6)			10.5	V
$\lvert V_{BIAS}–V_{RESET}\rvert$	Supply voltage delta (absolute value) (7)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK (8)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK (9)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE (9)					
$\lvert V_{ID}\rvert$	SubLVDS input differential voltage (absolute value). See Figure 8. Figure 9	150	250	350	mV
V_{CM}	Common mode voltage. See Figure 8. Figure 9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage. See Figure 8. Figure 9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance. See Figure 10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

(1) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(2) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(3) All voltage values are with respect to the ground pins (V_{SS}).
(4) V_{OFFSET} supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(7) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(8) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(9) Refer to the SubLVDS timing requirements in *Timing Requirements*.

Copyright © 2016–2018, Texas Instruments Incorporated

Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array temperature – long-term operational(10) (11) (12) (13)	0		40 to 70(12)	°C
	Array temperature – short-term operational, 25 hr max(11) (14)	–20		–10	°C
	Array temperature – short-term operational, 500 hr max(11) (14)	–10		0	°C
	Array temperature – short-term operational, 500 hr max(11) (14)	70		75	°C
T_{WINDOW}	Window temperature – operational (15) (16)			90	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(17)			30	°C
T_{DP-AVG}	Average dew point temperature, non-condensing(18)			24	°C
T_{DP-ELR}	Elevated dew point temperature range, non-condensing(19)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range.			6	Months
ILL_{UV}	Illumination wavelengths < 420 nm (10)			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 420 nm and 700 nm			Thermally Limited	
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle (16)			55	degrees

(10) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 18 and the package thermal resistance using *Micromirror Array Temperature Calculation*.
(12) Per Figure 1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-On/Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the useful life of the device.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The locations of thermal test points TP2, TP3, TP4, and TP5 shown in Figure 18 are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
(16) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 18. The window test points TP2, TP3, TP4, and TP5 shown in Figure 18 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

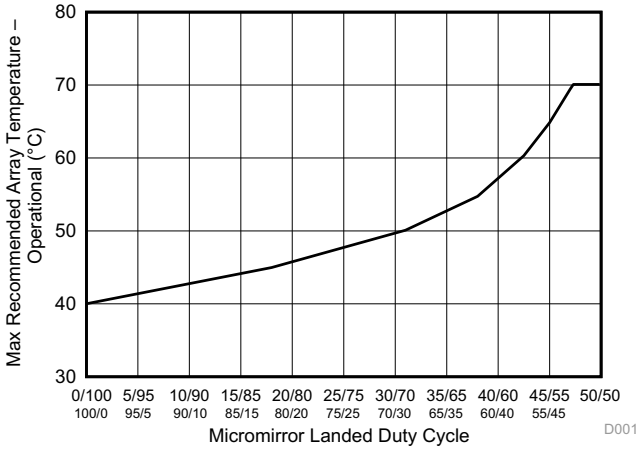


Figure 1. Maximum Recommended Array Temperature – Derating Curve

Copyright © 2016–2018, Texas Instruments Incorporated

6.5 Thermal Information

THERMAL METRIC[1]		DLP3310 FQM (LGA) 92 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)[1]	6.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS[2]	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD}[3] [4]	V_{DD} = 1.95 V			135	mA
		V_{DD} = 1.8 V		123.6		
I_{DDI}	Supply current: V_{DDI}[3] [4]	V_{DDI} = 1.95 V			35.34	mA
		V_{DD} = 1.8 V		32		
I_{OFFSET}	Supply current: V_{OFFSET}[5] [6]	V_{OFFSET} = 10.5 V			2.55	mA
		V_{OFFSET} = 10 V		2.5		
I_{BIAS}	Supply current: V_{BIAS}[5] [6]	V_{BIAS} = 18.5 V			1.25	mA
		V_{BIAS} = 18 V		1.2		
I_{RESET}	Supply current: V_{RESET}[6]	V_{RESET} = –14.5 V			–2.55	mA
		V_{RESET} = –14 V		–2.5		
POWER[7]						
P_{DD}	Supply power dissipation: V_{DD}[3] [4]	V_{DD} = 1.95 V			263.25	mW
		V_{DD} = 1.8 V		222.48		
P_{DDI}	Supply power dissipation: V_{DDI}[3] [4]	V_{DDI} = 1.95 V			68.91	mW
		V_{DD} = 1.8 V		57.6		
P_{OFFSET}	Supply power dissipation: V_{OFFSET}[5] [6]	V_{OFFSET} = 10.5 V			26.78	mW
		V_{OFFSET} = 10 V		25		
P_{BIAS}	Supply power dissipation: V_{BIAS}[5] [6]	V_{BIAS} = 18.5 V			23.13	mW
		V_{BIAS} = 18 V		21.6		
P_{RESET}	Supply power dissipation: V_{RESET}[6]	V_{RESET} = –14.5 V			36.98	mW
		V_{RESET} = –14 V		35		
P_{TOTAL}	Supply power dissipation: Total			361.68	419.05	mW
LPSDR INPUT[8]						
$V_{IH(DC)}$	DC input high voltage[9]		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(DC)}$	DC input low voltage[9]		–0.3		0.3 × V_{DD}	V
$V_{IH(AC)}$	AC input high voltage[9]		0.8 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(AC)}$	AC input low voltage[9]		–0.3		0.2 × V_{DD}	V
ΔV_T	Hysteresis ($V_{T+} – V_{T–}$)	Figure 10	0.1 × V_{DD}		0.4 × V_{DD}	V

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.

Copyright © 2016–2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
I_{IL}	Low–level input current	V_{DD} = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	V_{DD} = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × V_{DD}			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × V_{DD}	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (768 × 344) micromirrors	400		500	pF

(10) LPSDR specification is for pin LS_RDATA.

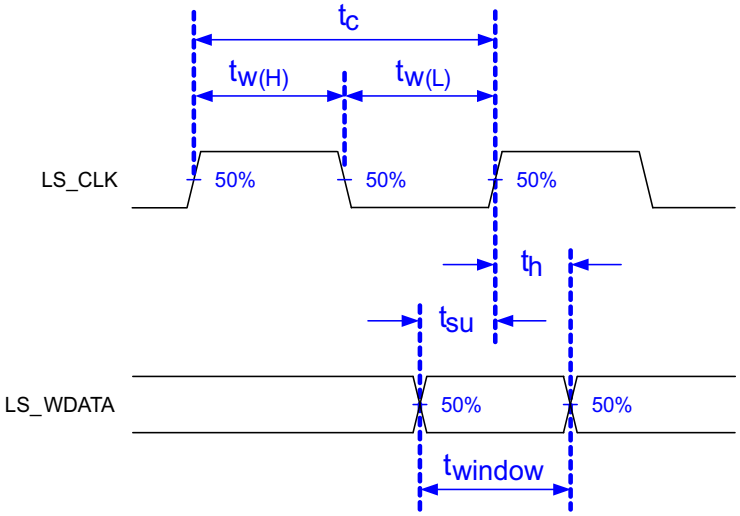
6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × V_{DD}, See Figure 3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × V_{DD}, See Figure 3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × V_{DD}, See Figure 3	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × V_{DD}, See Figure 3	0.25			V/ns
t_c	Cycle time LS_CLK,	See Figure 2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, See Figure 2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, See Figure 2	3.1			ns
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, See Figure 2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, See Figure 2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + Hold time, Figure 2	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, See Figure 5		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, See Figure 4	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, See Figure 4	0.7	1		V/ns
t_c	Cycle time DCLK	See Figure 6	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, See Figure 6	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, See Figure 6	0.79			ns
t_{su}	Setup time	D(0:7) valid before DCLK ↑ or DCLK ↓, See Figure 6				
t_h	Hold time	D(0:7) valid after DCLK ↑ or DCLK ↓, See Figure 6				
t_{WINDOW}	Window time	Setup time + Hold time, See Figure 6, Figure 7			0.3	ns
$t_{LVDS-ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in Figure 3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in Figure 3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.

Copyright © 2016–2018, Texas Instruments Incorporated



Low-speed interface is LPSDR and adheres to the *Electrical Characteristics* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

Figure 2. LPSDR Switching Parameters

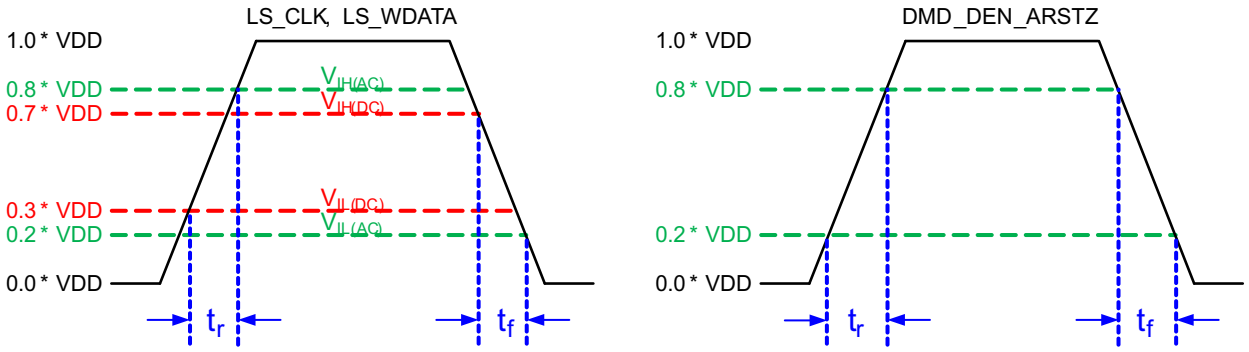


Figure 3. LPSDR Input Rise and Fall Slew Rate

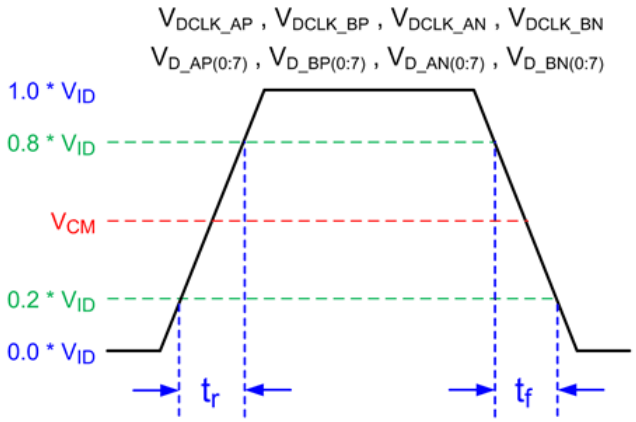


Figure 4. SubLVDS Input Rise and Fall Slew Rate

Copyright © 2016–2018, Texas Instruments Incorporated

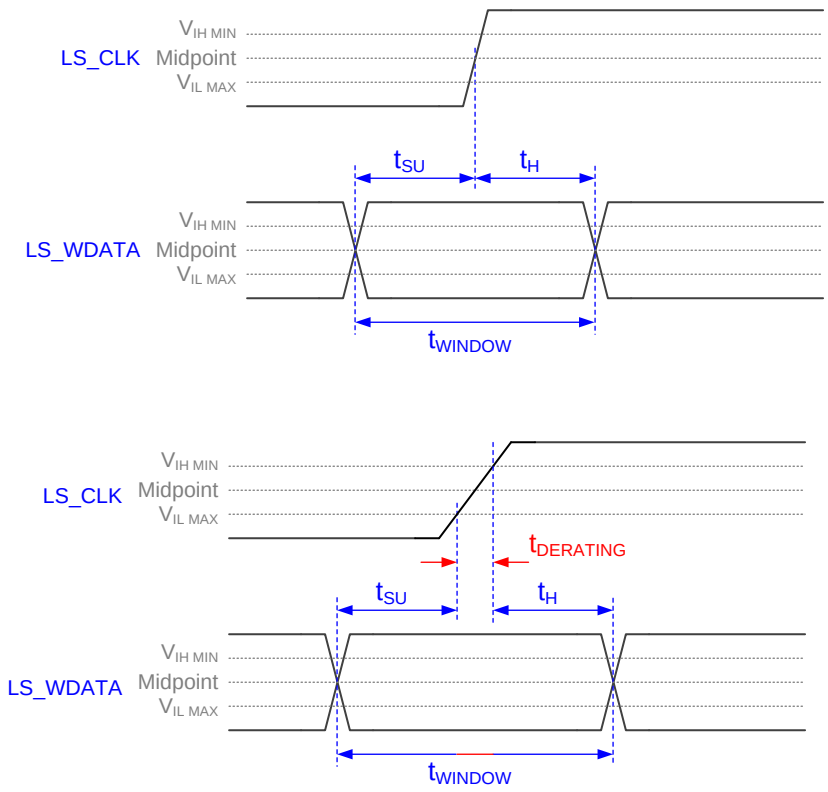


Figure 5. Window Time Derating Concept

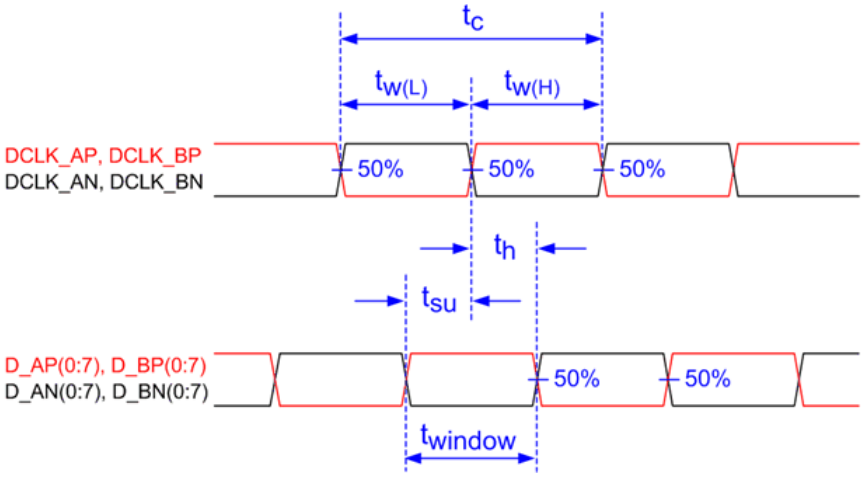
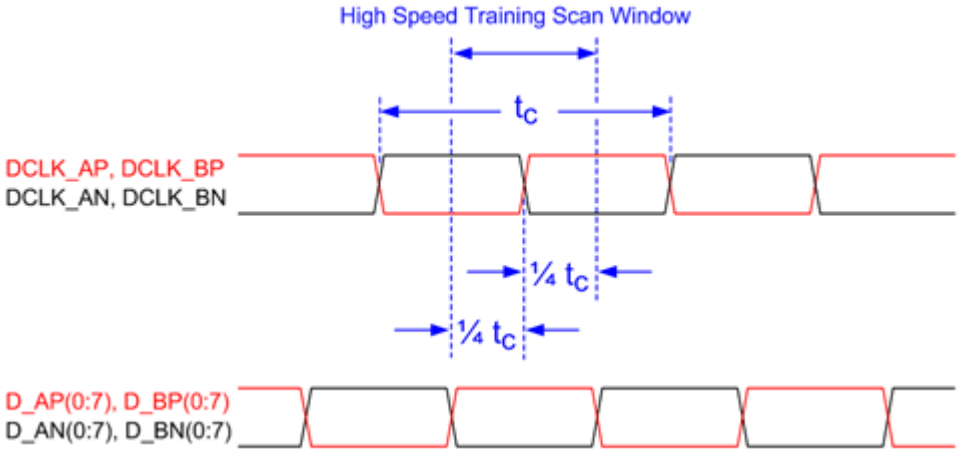


Figure 6. SubLVDS Switching Parameters



Note: Refer to *High-Speed Interface* for details.

Figure 7. High-Speed Training Scan Window

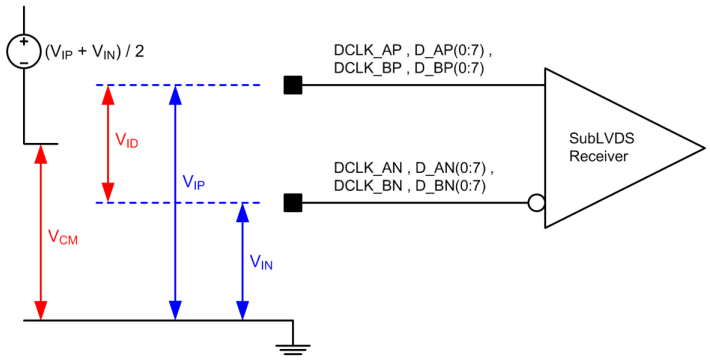


Figure 8. SubLVDS Voltage Parameters

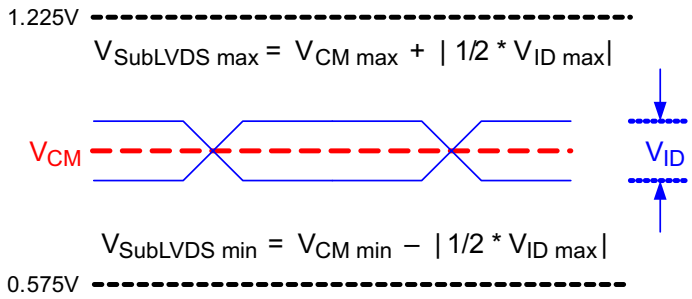


Figure 9. SubLVDS Waveform Parameters

Copyright © 2016–2018, Texas Instruments Incorporated

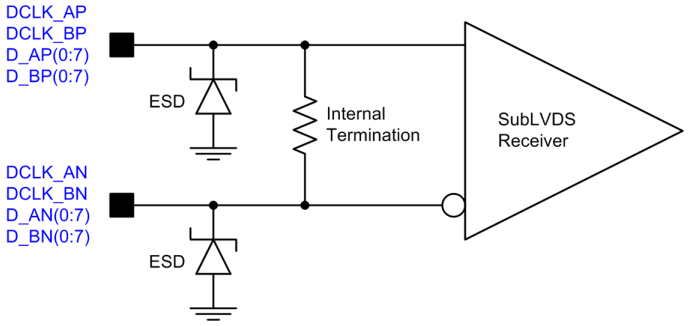


Figure 10. SubLVDS Equivalent Input Circuit

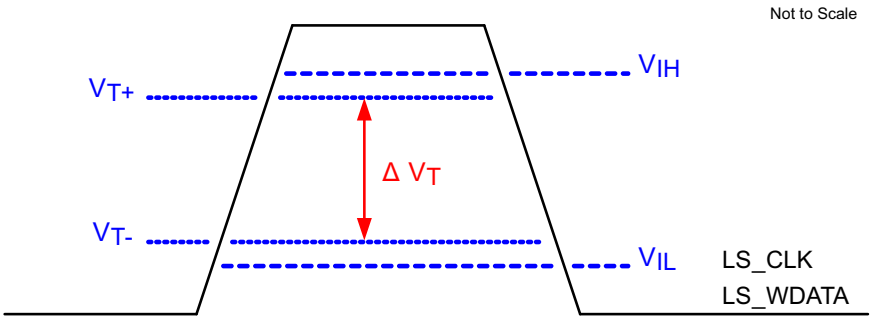


Figure 11. LPSDR Input Hysteresis

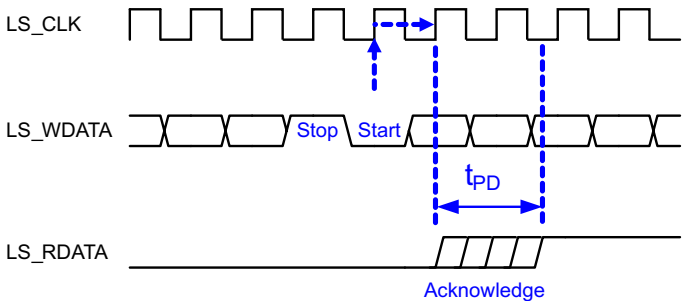
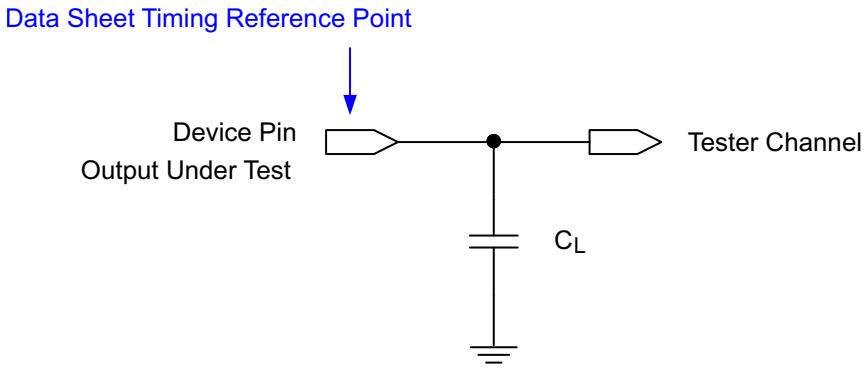


Figure 12. LPSDR Read Out



See *Timing* for more information.

Figure 13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, Clock to Q, rising edge of LS_CLK input to LS_RDATA output (See Figure 12).	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal Interface Area (1)			60	N
• Clamping and Electrical Interface Area (1)			110	N

(1) Uniformly distributed within area shown in Figure 14.

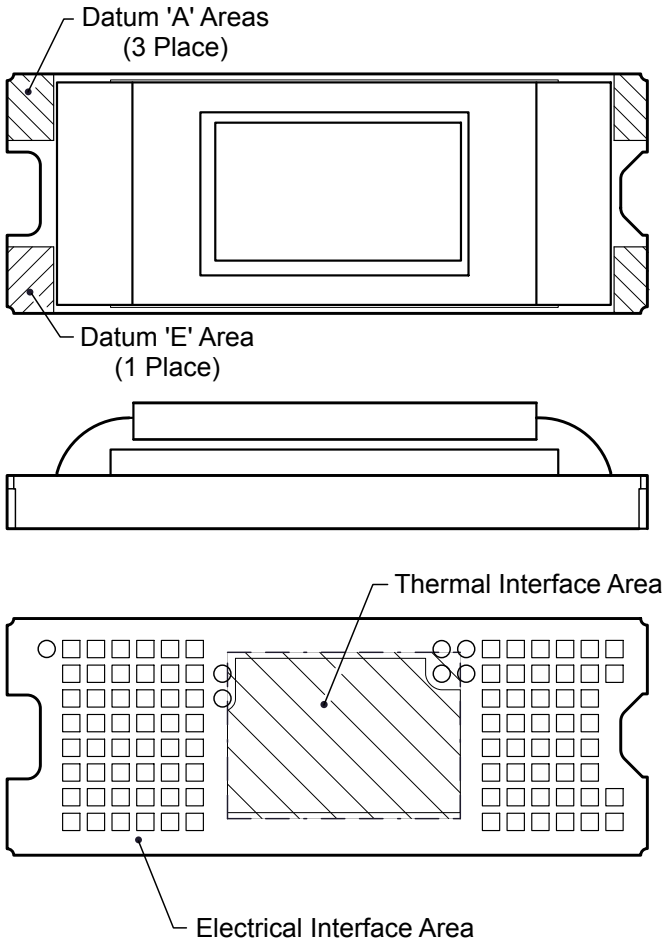


Figure 14. System Interface Loads

Copyright © 2016–2018, Texas Instruments Incorporated

6.10 Micromirror Array Physical Characteristics

	PARAMETER		VALUE	UNIT
	Number of active columns	See Figure 15	1368	micromirrors
	Number of active rows	See Figure 15	768	micromirrors
ε	Micromirror (pixel) pitch	See Figure 16	5.4	µm
	Micromirror active array width	Micromirror pitch × number of active columns; see Figure 15	7.387	mm
	Micromirror active array height	Micromirror pitch × number of active rows; see Figure 15	4.147	mm
	Micromirror active border	Pond of micromirror (POM)(1)	20	micromirrors/side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

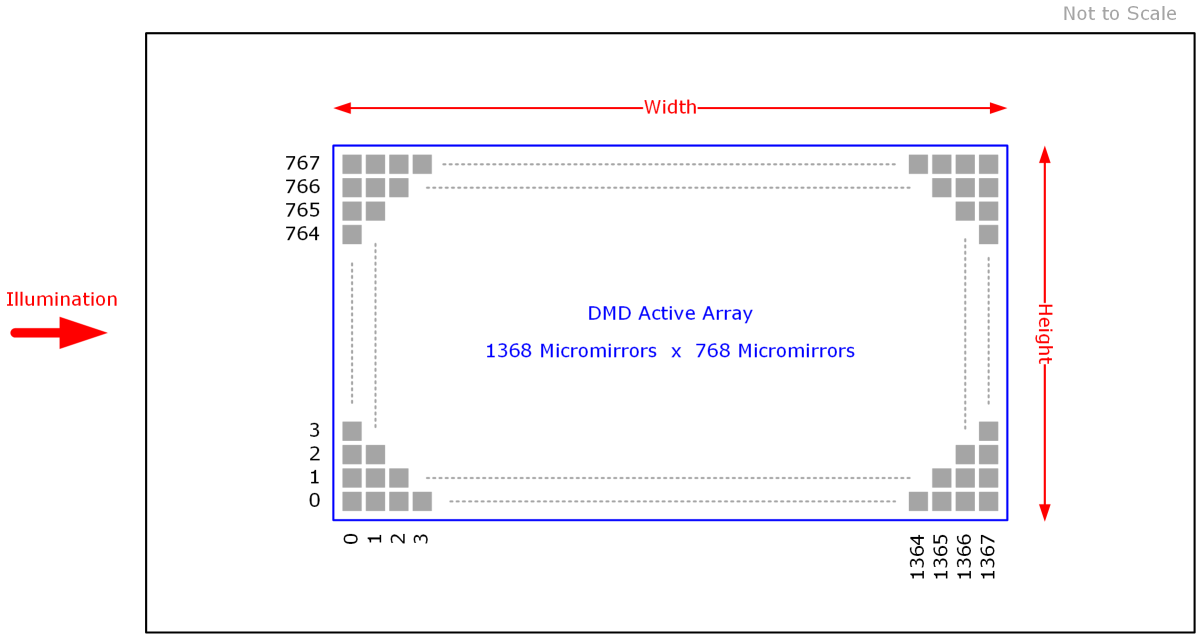


Figure 15. Micromirror Array Physical Characteristics

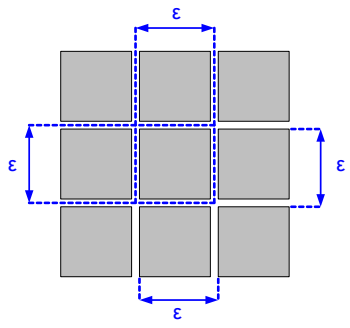


Figure 16. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle	DMD landed state(1)		17		degree
Micromirror tilt angle tolerance(2) (3) (4) (5)		–1.4		1.4	degree
Micromirror tilt direction(6) (7)	Landed ON state		180		degree
	Landed OFF state		270		
Micromirror crossover time(8)	Typical Performance		1	3	µs
Micromirror switching time(9)	Typical Performance	10			
Number of out-of-specification micromirrors(10)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror.
(10) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.

Not to Scale

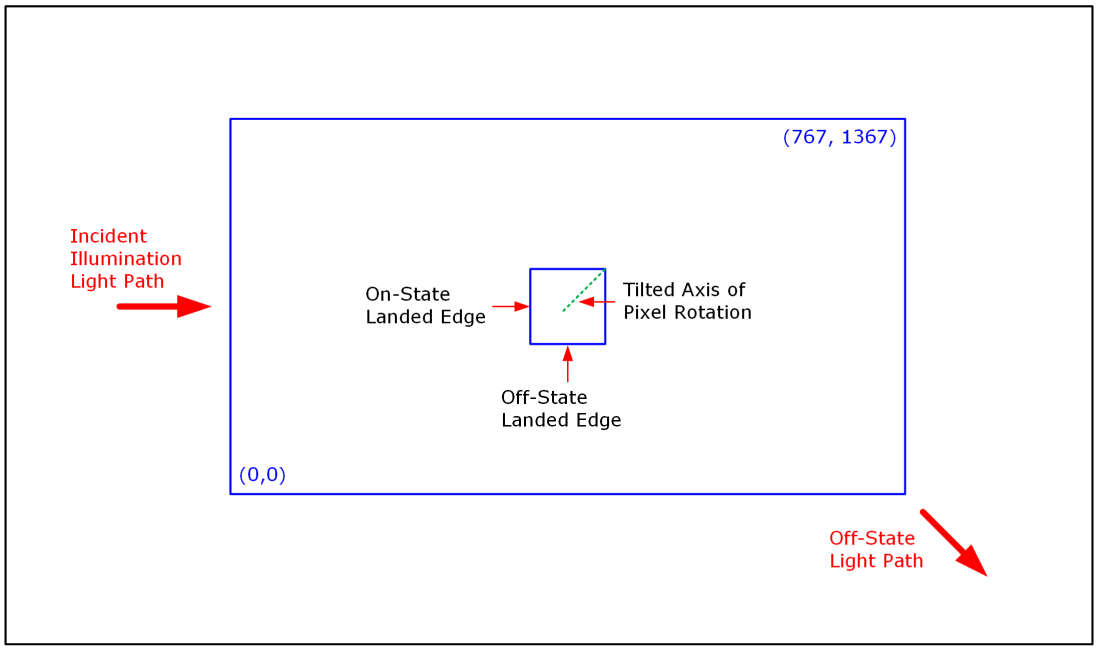


Figure 17. Landed Pixel Orientation and Tilt

Copyright © 2016–2018, Texas Instruments Incorporated

6.12 Window Characteristics

PARAMETER(1)		MIN	NOM	MAX	UNIT
Window material			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture(2)				See (2)	
Illumination overfill(3)				See (3)	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Optical Interface and System Image Quality Considerations* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP3310 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

6.13 Chipset Component Usage Specification

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP3310 is a component of one or more DLP® chipsets. Reliable function and operation of the DLP3310 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices for operating or controlling a DLP DMD.

Copyright © 2016–2018, Texas Instruments Incorporated

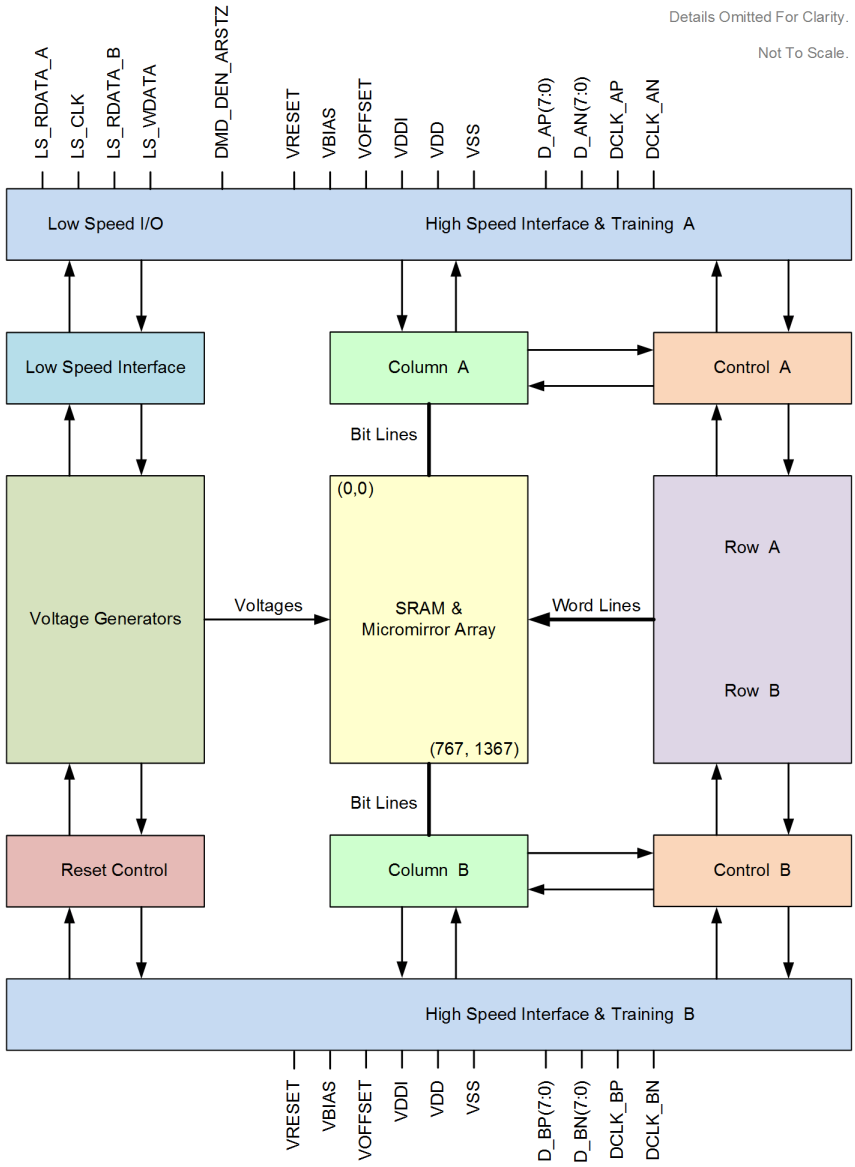
7 Detailed Description

7.1 Overview

The DLP3310 is a 0.33 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1368 columns by 768 rows in a square grid pixel arrangement. The electrical interface is Sub Low Voltage Differential Signaling (SubLVDS) data.

The DLP3310 is part of the chipset comprising of the DLP3310 DMD, DLPC3437 display controller, and DLPA3000 PMIC/LED driver. To ensure reliable operation, the DLP3310 DMD must always be used with the DLPC3437 display controller and the DLPA3000 PMIC/LED drivers.

7.2 Functional Block Diagram



(1) Details omitted for clarity.

Copyright © 2016–2018, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Power Interface

The power management IC DLPA3000 contains 3 regulated DC supplies for the DMD reset circuitry: V_{BIAS}, V_{RESET} and V_{OFFSET}, as well as the 2 regulated DC supplies for the DLPC3437 controller.

7.3.2 Low-Speed Interface

The Low Speed Interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3437 controller. See the DLPC3437 controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

Copyright © 2016–2018, Texas Instruments Incorporated

Optical Interface and System Image Quality Considerations (continued)

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

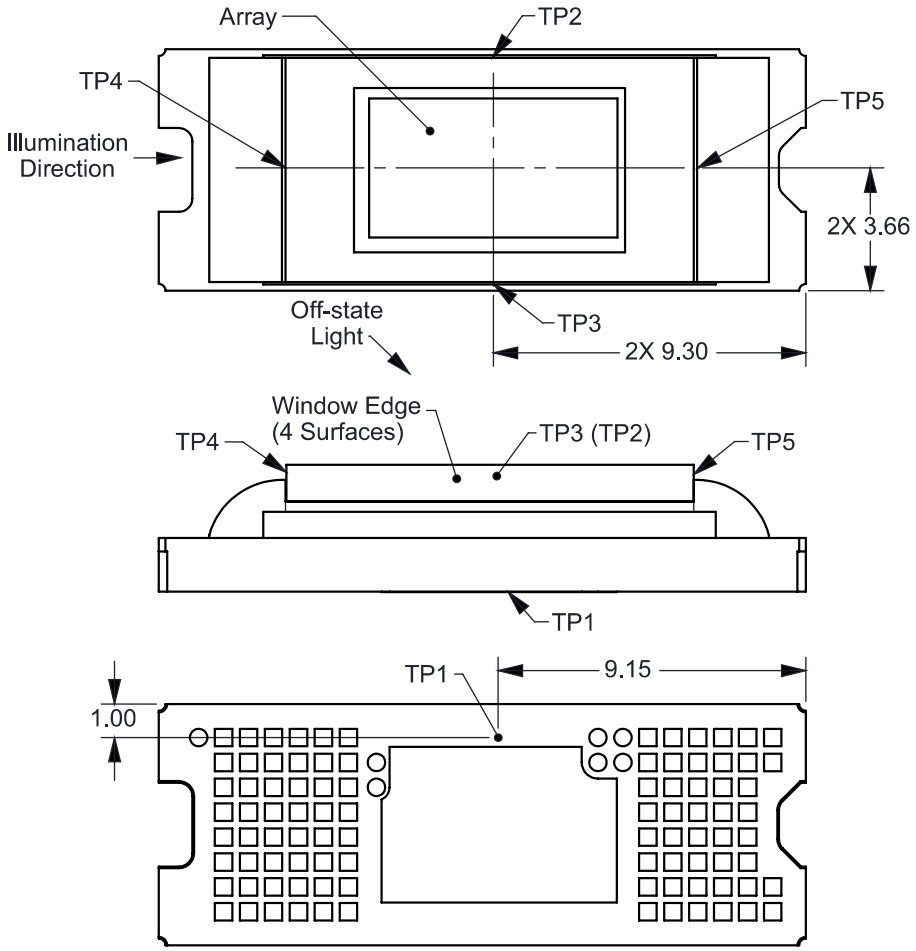


Figure 18. DMD Thermal Test Points

Copyright © 2016–2018, Texas Instruments Incorporated

Micromirror Array Temperature Calculation (continued)

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 18) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = thermal resistance of package specified in *Thermal Information* from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total (electrical + absorbed) DMD power on the array (Watts)
- $Q_{ELECTRICAL}$ = nominal electrical power
- $Q_{ILLUMINATION} = (C_{L2W} \times SL)$
- C_{L2W} = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- SL = measured screen Lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.16 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with projection efficiency from the DMD to the screen of 87%.

The conversion constant C_{L2W} is calculated to be 0.00266 W/lm based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculations for typical projection application:

C_{L2W} = 0.00266 W/lm

SL = 450 lm

$Q_{ELECTRICAL}$ = 0.16 W

$T_{CERAMIC}$ = 55.0°C

Q_{ARRAY} = 0.16 W + (0.00266 W/lm × 450 lm) = 1.36 W

T_{ARRAY} = 55.0°C + (1.36 W × 6°C/W) = 63.2°C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time), whereas 0/100 would indicate that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Copyright © 2016–2018, Texas Instruments Incorporated

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Copyright © 2016–2018, Texas Instruments Incorporated

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_%×Blue_Scale_Value)

where

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 2.

Copyright © 2016–2018, Texas Instruments Incorporated

Table 2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the Landed Duty Cycle is any applied image processing. Within the DLP Controller DLPC3437, the two functions which affect Landed Duty Cycle are Gamma and IntelliBright™.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC3430/DLPC3435 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 19.

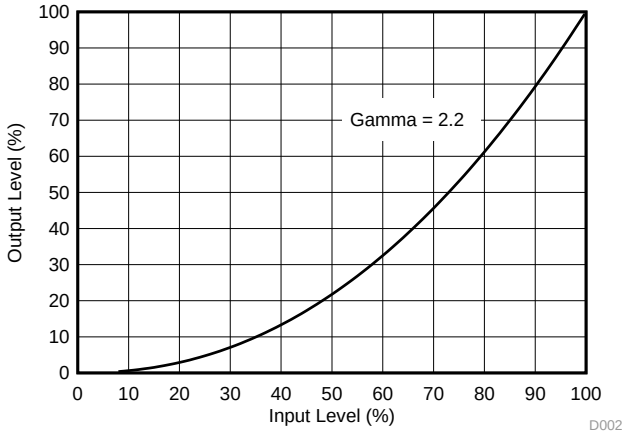


Figure 19. Example of Gamma = 2.2

Copyright © 2016–2018, Texas Instruments Incorporated

From Figure 19, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3437 controller.

Copyright © 2016–2018, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the dual DLPC3437 controllers. The new high tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness constrained applications. Applications of interest include projection embedded in display devices like battery powered mobile accessory full HD projectors, battery powered smart full HD projectors, digital signage, interactive surface projection, low latency gaming displays, interactive displays, and wearable displays.

DMD power-up and power-down sequencing is strictly controlled by the DLPA3000. Refer to *Power Supply Recommendations* for power-up and power-down specifications. To ensure reliable operation, the DLP3310 DMD must always be used with two DLPC3437 display controllers and a DLPA3000 PMIC/LED driver.

Copyright © 2016–2018, Texas Instruments Incorporated

8.2 Typical Application

A common application when using a DLP3310 DMD and two DLPC3437s is for creating a pico-projector that can be used as an accessory to a smartphone, tablet or a laptop. The two DLPC3437s in the pico-projector receive images from the XC7Z020-1CLG484I4493 FPGA, which receives images from a multimedia front end within the product as shown in Figure 20.

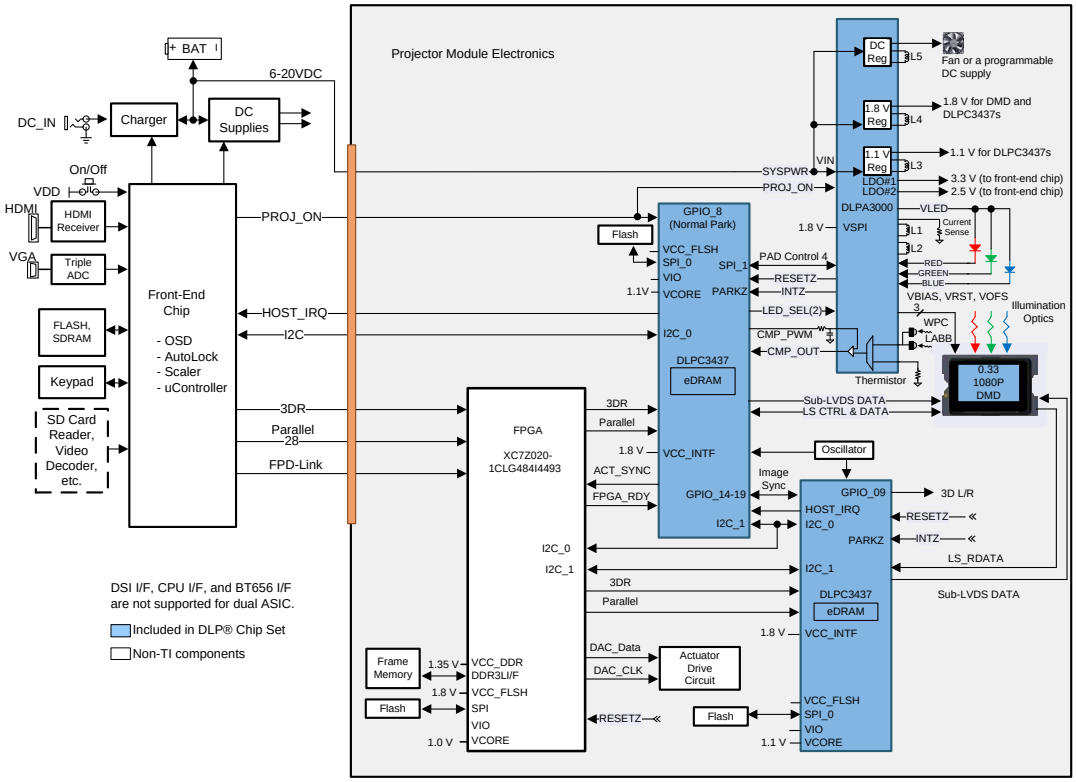


Figure 20. Typical Application Diagram

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of a DLP3310 DMD, two DLPC3437 controllers, a XC7Z020-1CLG484I4493 FPGA, and a DLPA3000 PMIC/LED driver. The XC7Z020-1CLG484I4493 FPGA and DLPC3437 controllers do the digital image processing, the DLPA3000 provides the needed analog functions for the projector, and the DLP3310 DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips are needed. At a minimum a Flash part is needed to store the software and firmware to control the XC7Z020-1CLG484I4493 FPGA, and each of the DLPC3437 controllers.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

For connecting the XC7Z020-1CLG484I4493 FPGA to the multimedia front end for receiving images, either a 24-bit parallel interface can be used, or the dual FPD-Link interface can be used. An I^2C interface should be connected from the multimedia front end for sending commands to one of the DLPC3437 controllers for configuring the chipset for different features.

Copyright © 2016–2018, Texas Instruments Incorporated

Typical Application (continued)

8.2.2 Detailed Design Procedure

For connecting together the XC7Z020-1CLG484I4493 FPGA, the two DLPC3437 controllers, the DLPA3000, and the DLP3310 DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in Figure 21. For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

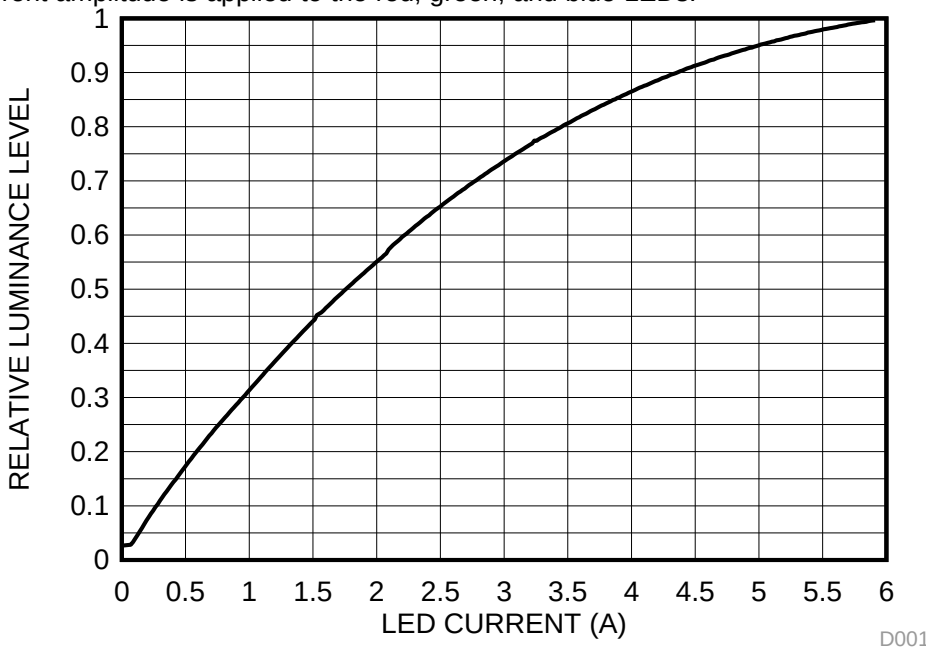


Figure 21. Luminance vs Current

Copyright © 2016–2018, Texas Instruments Incorporated

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA3000 devices.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 23. V_{SS} must also be connected.

9.1 Power Supply Power-Up Procedure

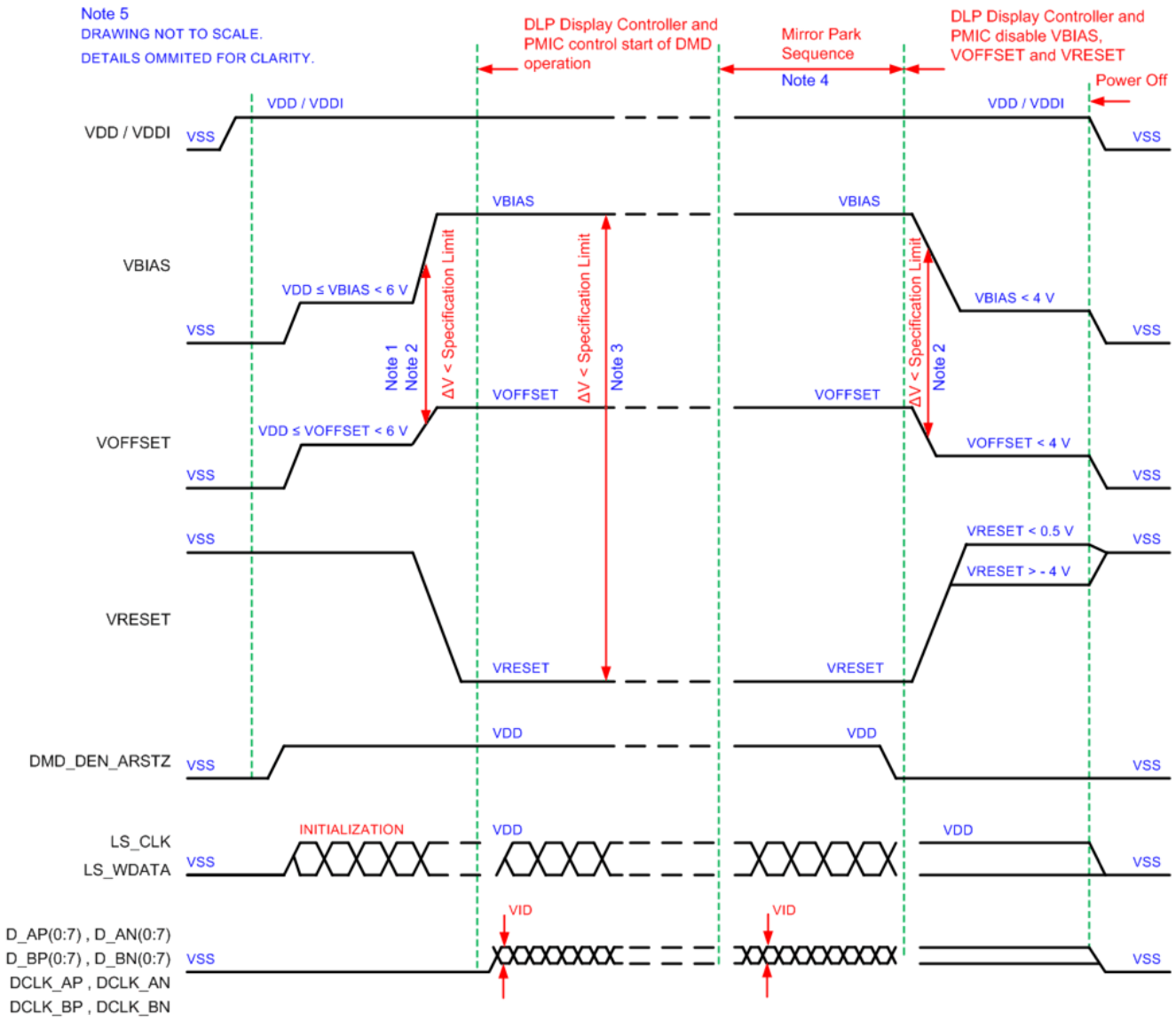
- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions*. Refer to Table 3 and the *Layout Example* for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after V_{DD} and V_{DDI} have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in *Recommended Operating Conditions* (Refer to Note 2 for Figure 22).
- During power-down, the DMD's LPSDR input pins must be less than V_{DDI}, the specified limit shown in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in Figure 22.

Copyright © 2016–2018, Texas Instruments Incorporated

9.3 Power Supply Sequencing Requirements



(1) Refer to Table 3 and Figure 23 for critical power-up sequence delay requirements.

(2) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down. Refer to Table 3 and Figure 23 for power-up delay requirements.

(3) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than specified limit shown in *Recommended Operating Conditions*.

(4) When system power is interrupted, the DLPA3000 initiates hardware power-down that disables V_{BIAS}, V_{RESET} and V_{OFFSET} after the Micromirror Park Sequence.

(5) Drawing is not to scale and details are omitted for clarity.

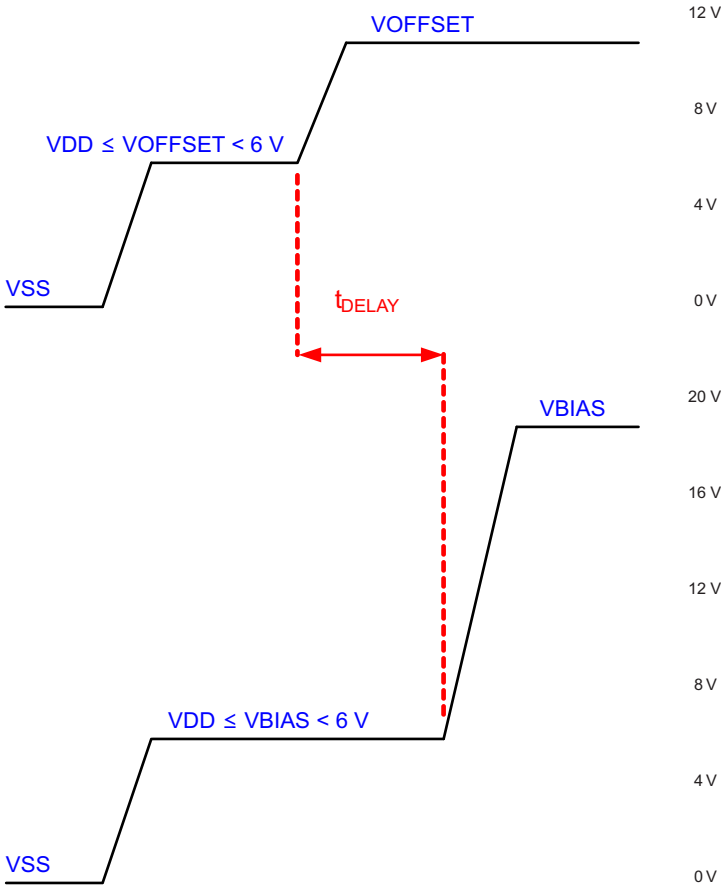
Figure 22. Power Supply Sequencing Requirements (Power Up and Power Down)

Copyright © 2016–2018, Texas Instruments Incorporated

Power Supply Sequencing Requirements (continued)

Table 3. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from V_{OFFSET} power up to V_{BIAS} power up	2		ms
V_{OFFSET}	Supply voltage level at beginning of power–up sequence delay (see Figure 23)		6	V
V_{BIAS}	Supply voltage level at end of power–up sequence delay (see Figure 23)		6	V



Refer to Table 3 for V_{OFFSET} and V_{BIAS} supply voltage levels during power-up sequence delay.

Figure 23. Power-Up Sequence Delay Requirement

Copyright © 2016–2018, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

The DLP3310 DMD is connected to a PCB or a Flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, etc. see the DLPC3437 controller datasheet. For a detailed layout example refer to the layout design files. Some layout guidelines for routing to the DLP3310 DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to Figure 24.
- Minimum of two 220-nF (35 V) capacitors - one close to V_{BIAS} pin. Capacitors C10 and C14 in Figure 24.
- Minimum of two 220-nF (35 V) capacitors - one close to each V_{RST} pin. Capacitors C11 and C13 in Figure 24.
- Minimum of two 220-nF (35 V) capacitors - one close to each V_{OFS} pin. Capacitors C4 and C12 in Figure 24.
- Minimum of four 220-nF (10 V) capacitors - two close to each side of the DMD. Capacitors C1, C3, C2, and C5 in Figure 24.

10.2 Layout Example

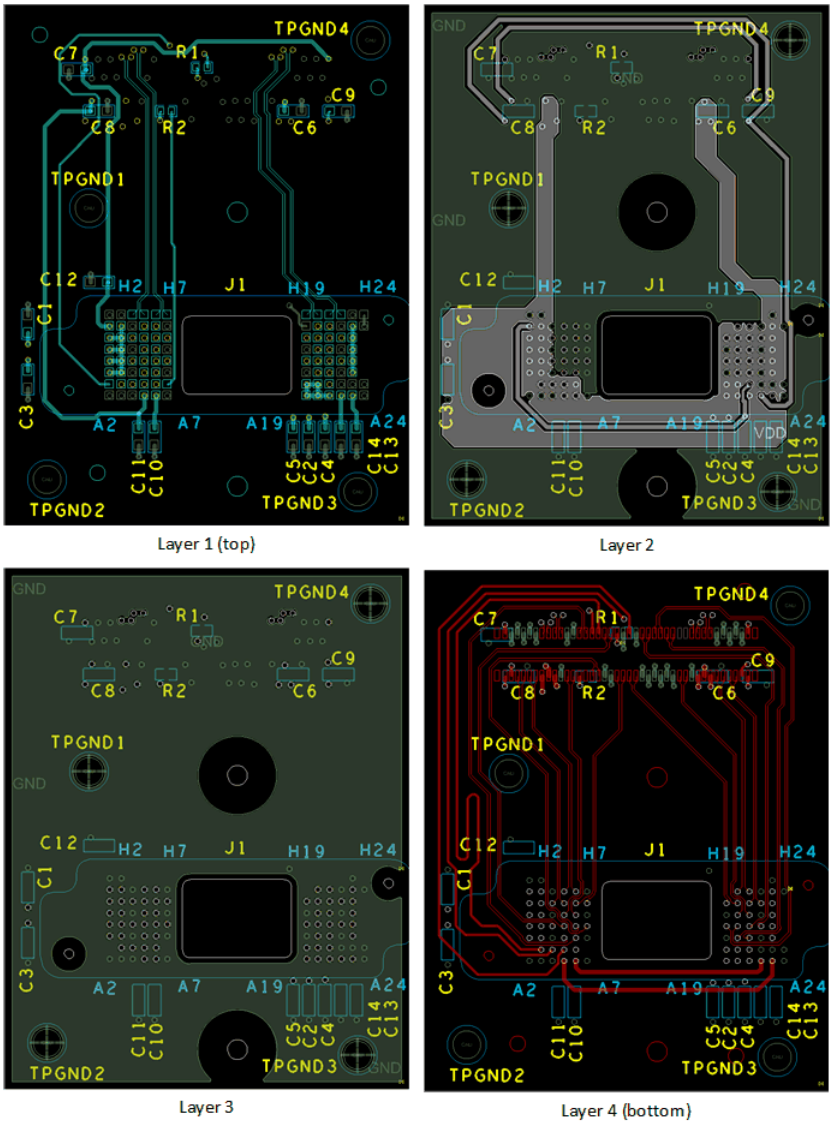


Figure 24. Power Supply Connections

Copyright © 2016–2018, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

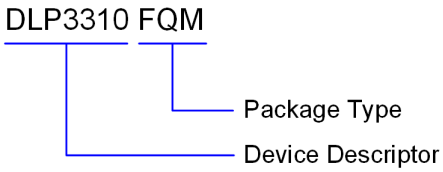


Figure 25. Part Number Description

11.1.2 Device Markings

The device marking includes the legible character string GHJJJJK DLP3310FQM. GHJJJJK is the lot trace code. DLP3310FQM is the device marking.

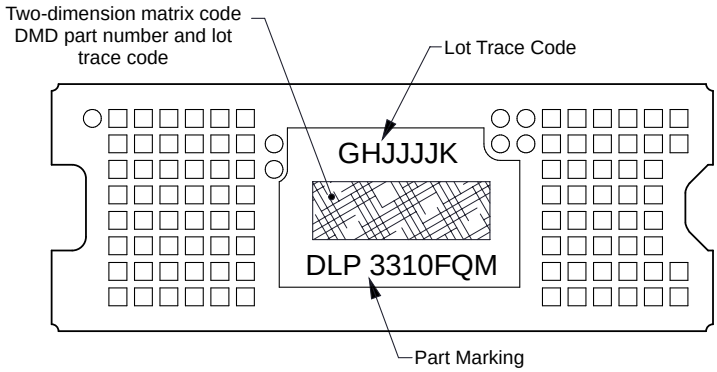


Figure 26. DMD Marking

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP3310	Click here	Click here	Click here	Click here	Click here
DLPC3437	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

Copyright © 2016–2018, Texas Instruments Incorporated

11.4 Trademarks

IntelliBright, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2016–2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3310FQM	ACTIVE	CLGA	FQM	92	100	RoHS & Green	Call TI	Level-1-NC-NC			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

© COPYRIGHT 2016 TEXAS INSTRUMENTS
UN-PUBLISHED, ALL RIGHTS RESERVED.

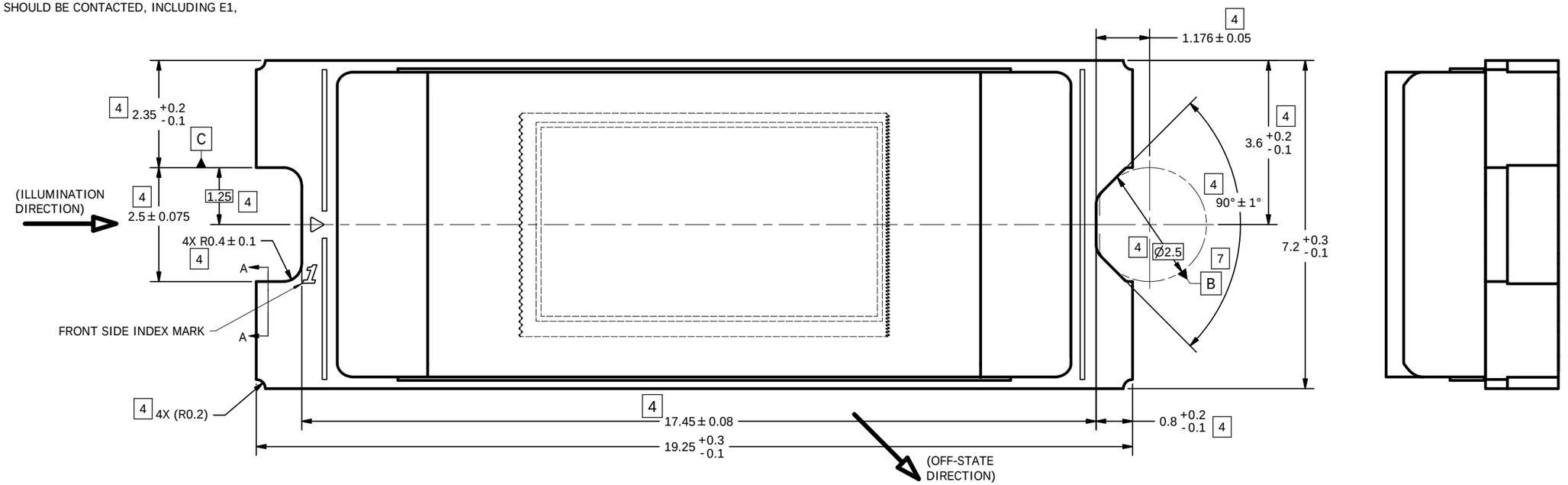
DWG NO. 2512400 SH 1

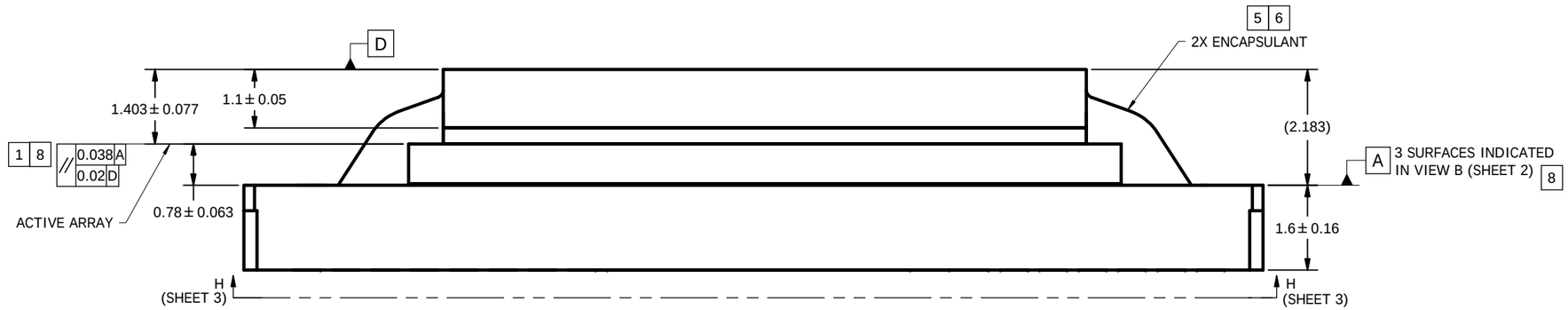
REVISIONS

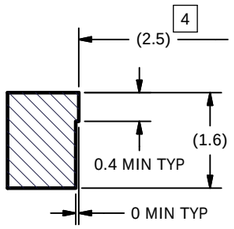
REV	DESCRIPTION	DATE	BY
A	ECO 2156795: INITIAL RELEASE	3/8/2016	BMH
B	ECO 2157307: UPDATE SUBSTRATE THICKNESS TOLERANCE & SYMBOLIZATION PAD SIZE/SHAPE	4/1/2016	BMH
C	ECO 2159285: CORRECT SUBSTRATE BACK SIDE MARKING IN VIEW H-H (SH. 3) FROM "465" TO "888"	7/7/2016	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.







SECTION A-A
(ROTATED 90°)
SCALE 20 : 1

	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	B. HASKETT	3/8/2016
ENGINEER	B. HASKETT	3/8/2016
QA/CE	P. KONRAD	3/8/2016
CM	S. SUSI	3/10/2016
	M. DORAK	3/8/2016
APPROVED	E. CARPENTER	3/10/2016

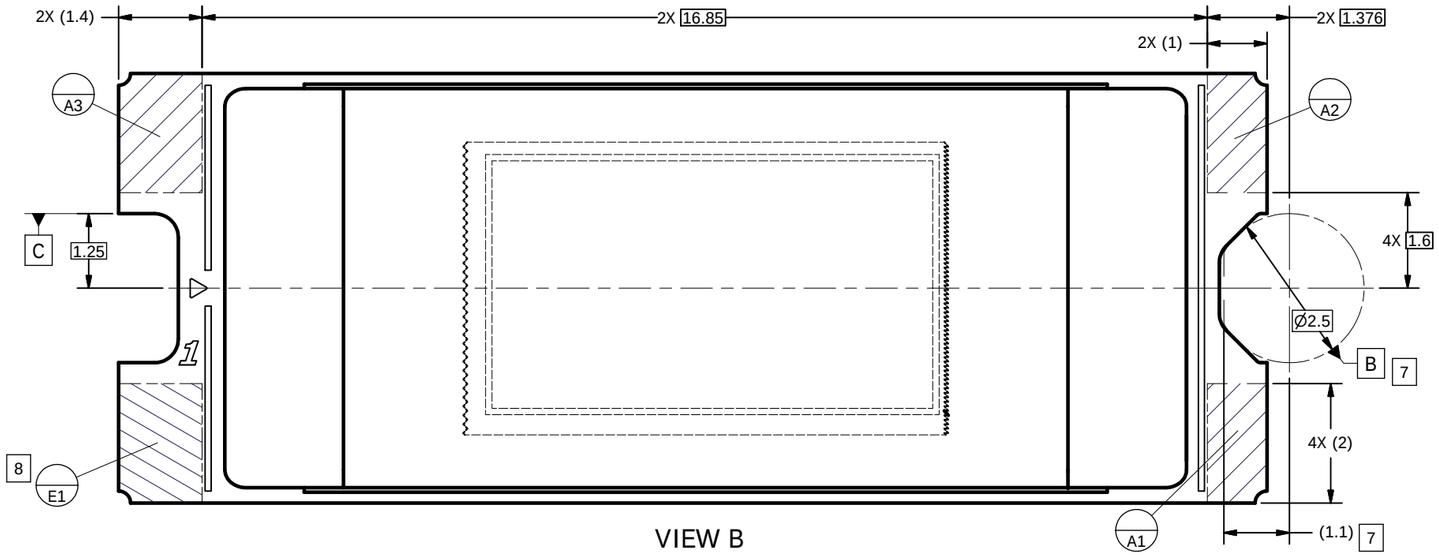
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .33 1080p SERIES 315 (FQM PACKAGE)

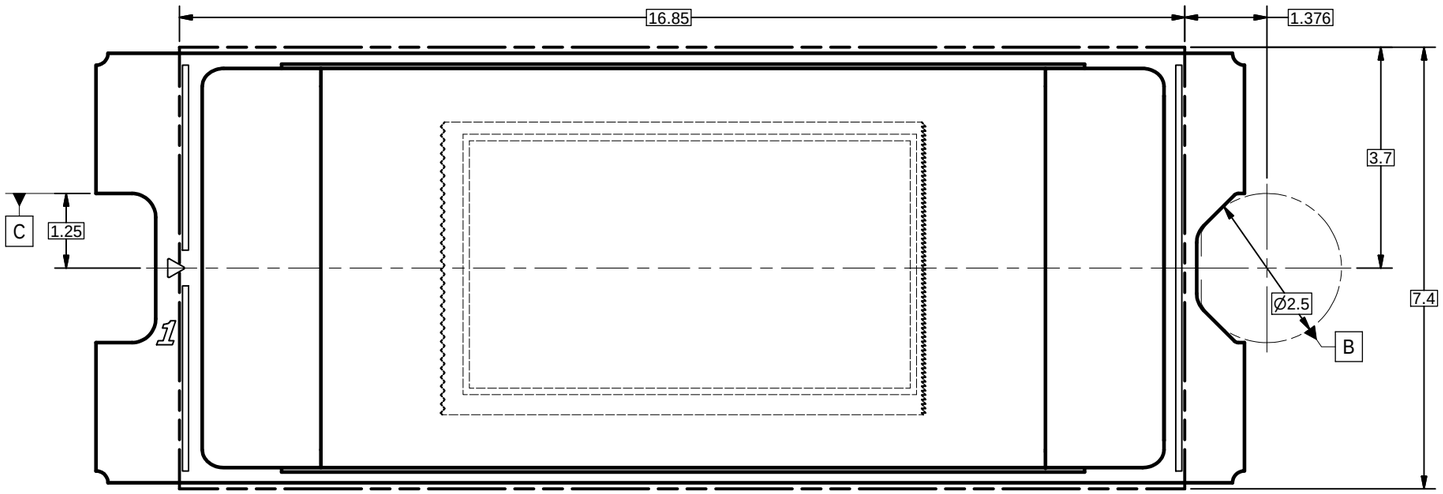
SIZE	DWG NO	REV
D	2512400	C

SCALE 20:1 SHEET 1 OF 3

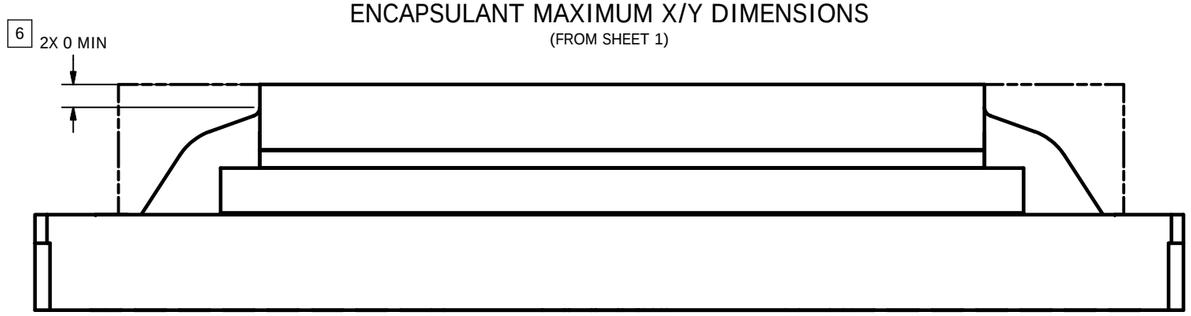
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



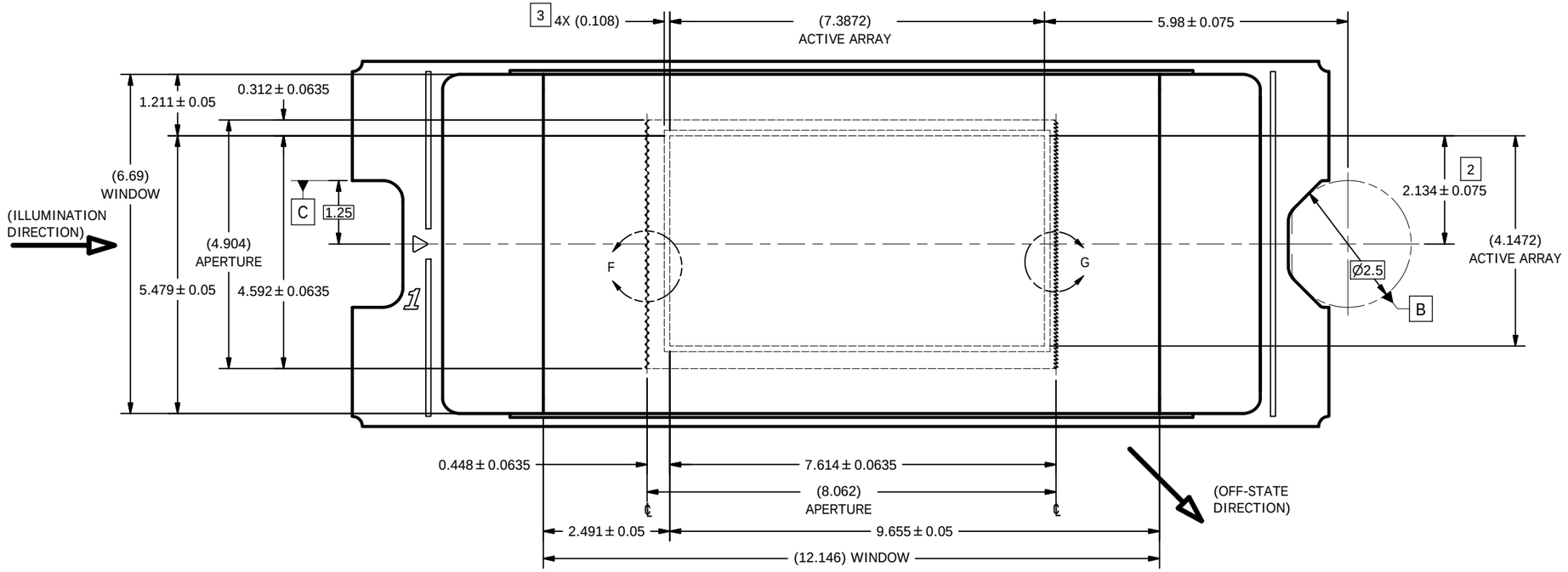
VIEW C 5
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



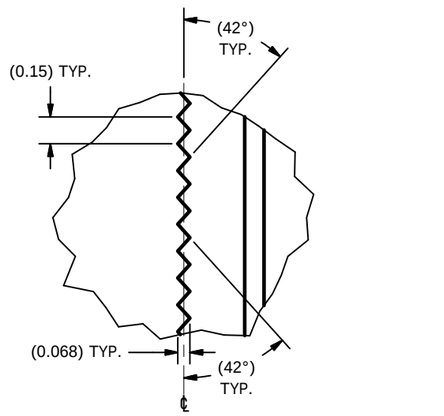
VIEW D
ENCAPSULANT MAXIMUM HEIGHT

Texas Instruments, Dallas Texas	DRAWN B. HASKETT	DATE 3/8/2016	SIZE D		DWG NO 2512400	REV C
			SCALE		SHEET 2 OF 3	

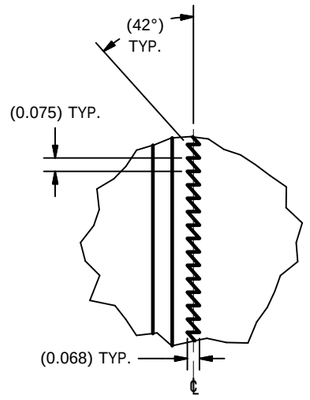
INV11-2006a



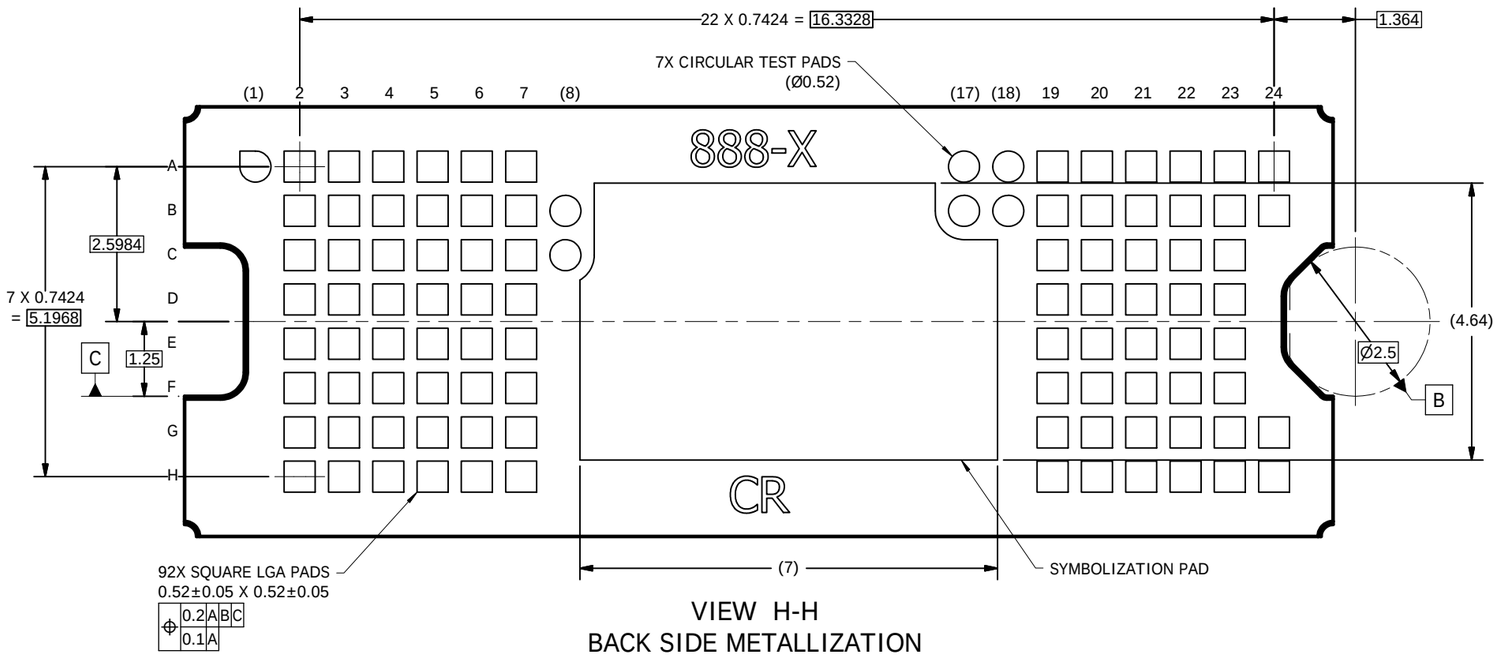
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
SCALE 60 : 1



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 3/8/2016	SIZE D	DWG NO 2512400	REV C
			SCALE	SHEET 3 OF 3	

INV11-2006a

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated